

TOSHIBA BIPOLAR LINEAR INTEGRATED CIRCUIT SILICON MONOLITHIC

TA75062P, TA75062S, TA75062F**DUAL OPERATIONAL AMPLIFIER**

The TA75062P, TA75062S and TA75062F are J-FET input low-power operational amplifiers with low input bias and offset current and fast slew rate.

The TA75062P is pin compatible with the TA75458P and 1458. The TA75062S is single-in-line package.

It is possible to exchange the position of 9 pin for 1 pin because of pin connection being symmetric.

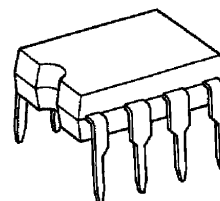
The TA75062F is mini-flat package.

The TA75062P series are excellent choice for active filters, integrators, buffers and sample-and-hold circuits.

FEATURES

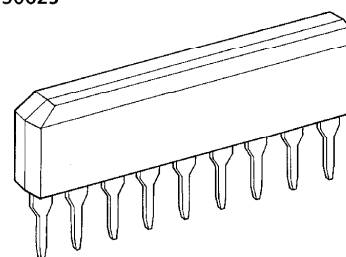
- Low Supply Current : 500 μ A MAX.
- Low Input Bias Current : 400pA MAX.
- Low Input Offset Current : 200pA MAX.
- High Slew Rate : 3.5V / μ s
- Wide Supply Voltage Range : $\pm 2 \sim \pm 18$ V
- Internal Frequency Compensation
- Output Short Circuit Protection

TA75062P



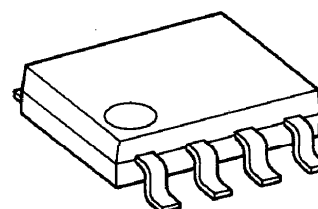
DIP8-P-300-2.54A

TA75062S



SIP9-P-2.54A

TA75062F



SOP8-P-225-1.27

Weight

DIP8-P-300-2.54	: 0.5g (Typ.)
SIP9-P-2.54A	: 0.9g (Typ.)
SOP8-P-225-1.27	: 0.1g (Typ.)

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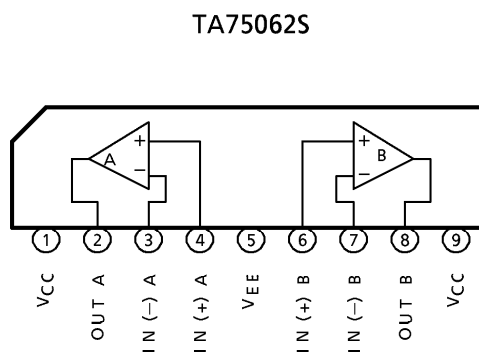
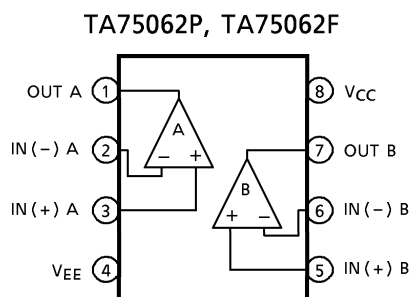
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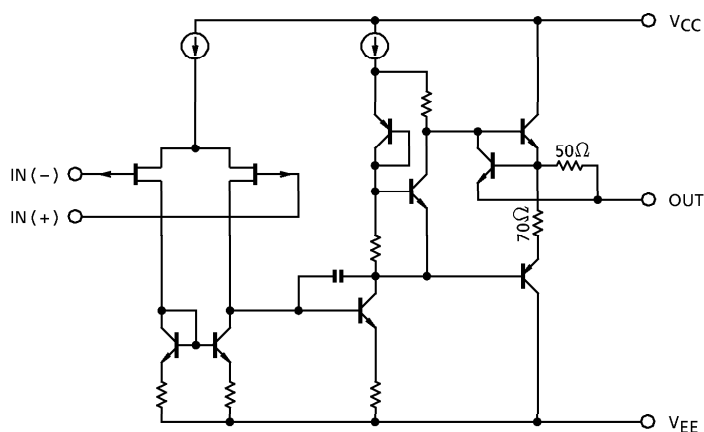
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● The information contained herein is subject to change without notice.

PIN CONNECTION (TOP VIEW)



EQUIVALENT CIRCUIT



MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Supply Voltage		V_{CC}	18	V
		V_{EE}	- 18	
Differential Input Voltage		DV_{IN}	± 30	V
Input Voltage		V_{IN}	± 15	V
Power Dissipation	TA75062P	P_D	500	mW
	TA75062S			
	TA75062F		240	
Operating Temperature		T_{opr}	- 40~85	°C
Storage Temperature		T_{stg}	- 55~125	°C

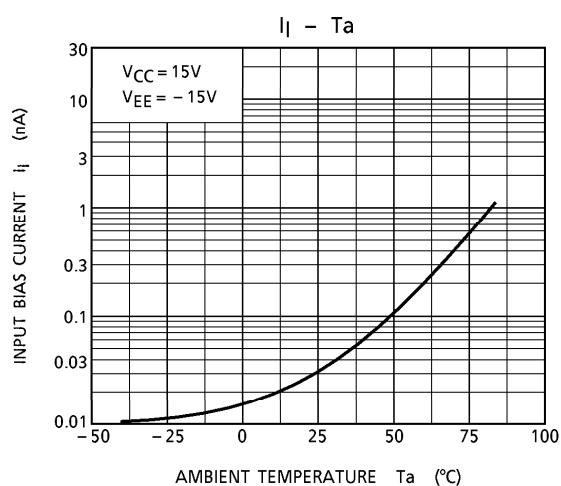
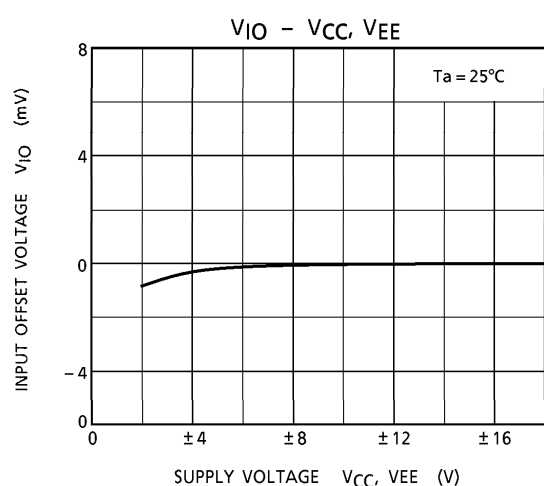
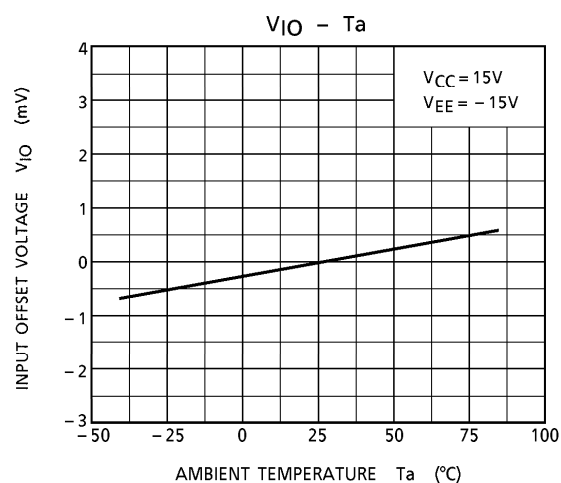
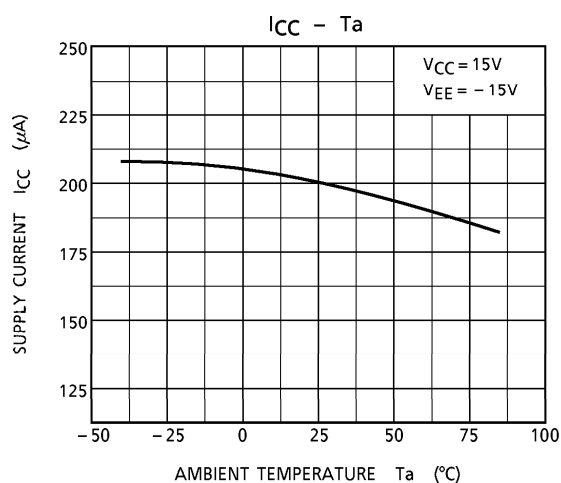
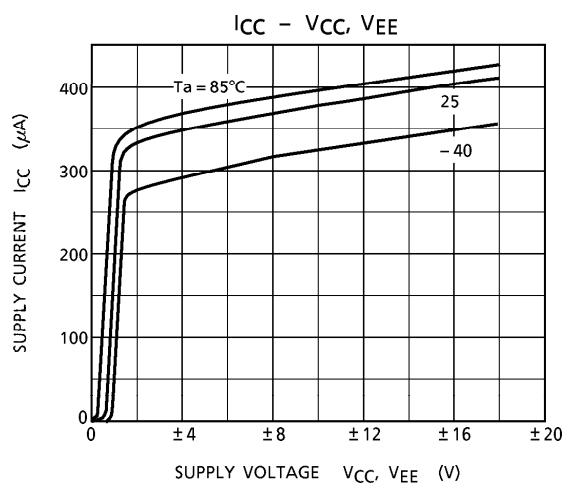
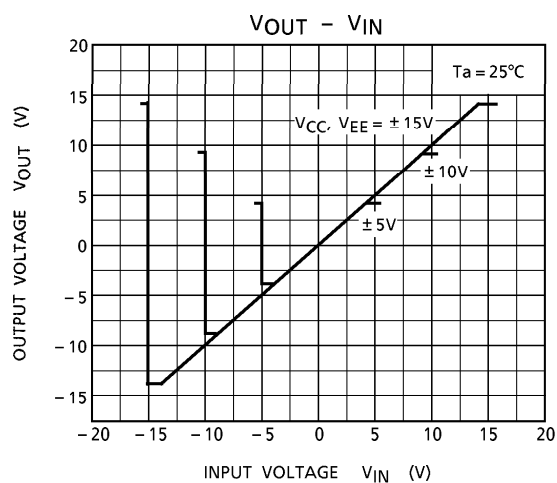
ELECTRICAL CHARACTERISTICS ($V_{CC} = 15V$, $V_{EE} = -15V$, $T_a = 25^\circ C$)

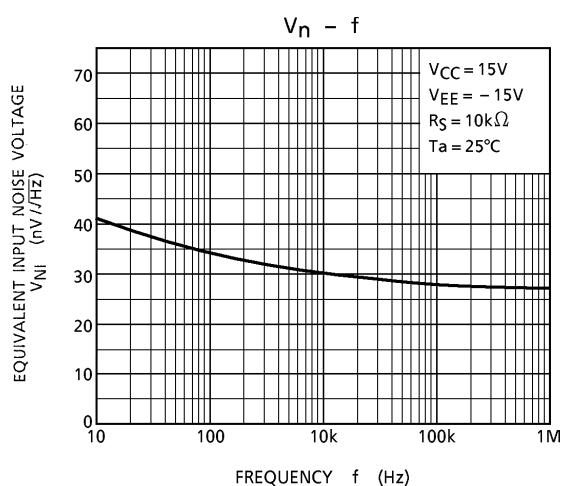
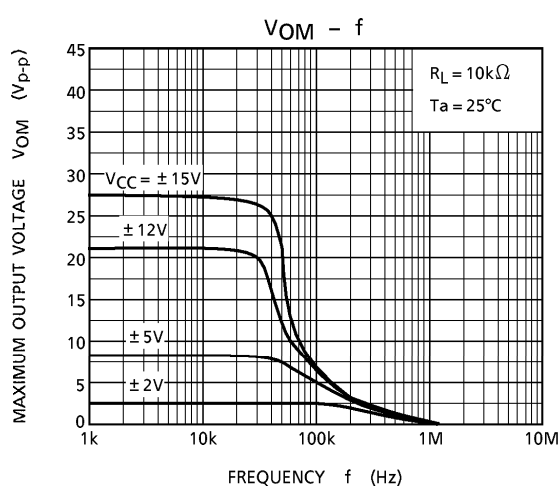
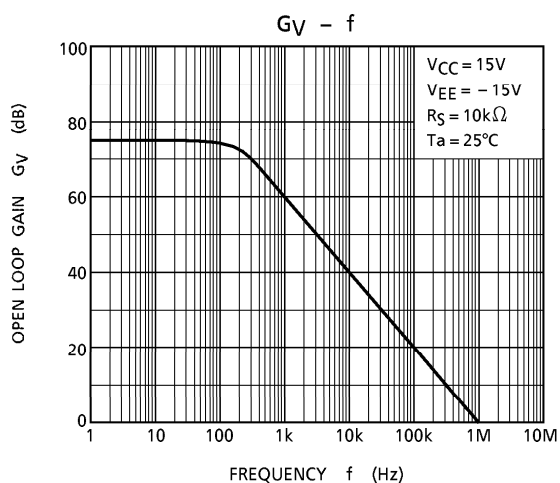
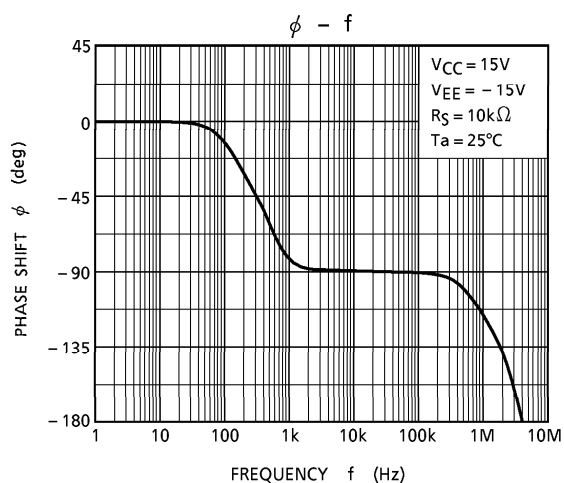
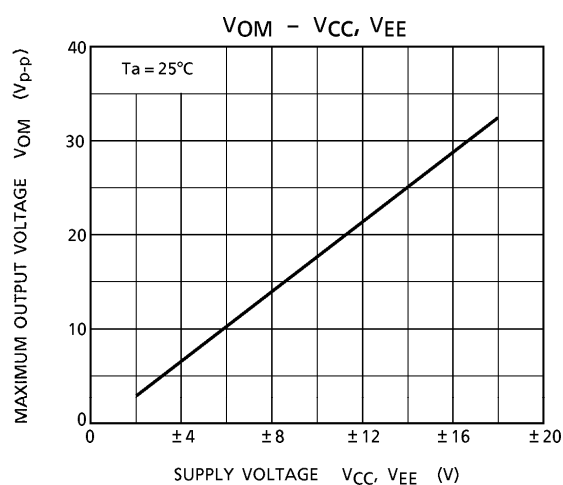
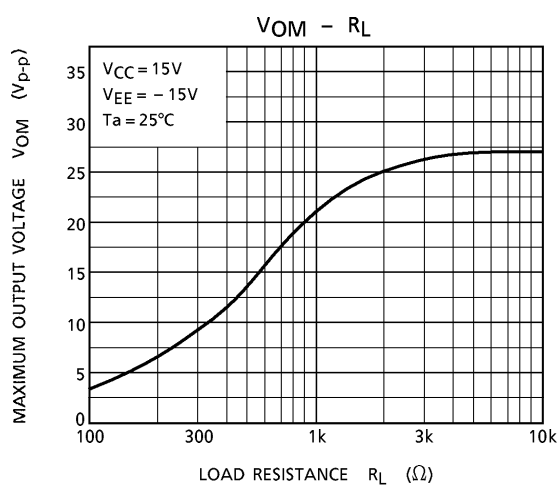
CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Offset Voltage	V_{IO}	—	$R_g \leq 10k\Omega$	—	3	15	mV
TC Of Input Offset Voltage	TCV_{IO}	—	—	—	10	—	$\mu V / ^\circ C$
Input Offset Current	I_{IO}	—	—	—	5	200	pA
Input Bias Current	I_I	—	—	—	30	400	pA
Common Mode Input Voltage	CMV_{IN}	—	—	± 11.5	± 12	—	V
Maximum Output Voltage	V_{OM}	—	$R_L = 10k\Omega$	20	27	—	V_{p-p}
Voltage Gain (Open Loop)	G_V	—	$V_{OUT} = \pm 10V$, $R_L = 10k\Omega$	3	6	—	V / mV
Unity Gain Cross Frequency	f_T	—	Open Loop, $R_L = 10k\Omega$	—	1	—	MHz
Input Resistance	R_{IN}	—	—	—	10^{12}	—	Ω
Common Mode Input Signal Rejection Ratio	CMRR	—	$R_g \leq 10k\Omega$	70	76	—	dB
Supply Voltage Rejection Ratio	SVRR	—	$R_g \leq 10k\Omega$	70	76	—	dB
Supply Current	I_{CC} , I_{EE}	—	Non load	—	400	500	μA
Cross Talk		—	—	—	-120	—	dB

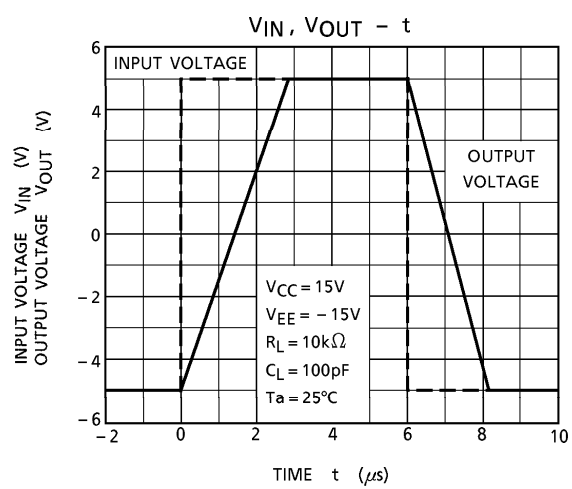
OPERATING CHARACTERISTICS ($V_{CC} = 15V$, $V_{EE} = -15V$, $T_a = 25^\circ C$)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Slew Rate	SR	—	$V_{IN} = 10V_{p-p}$, $R_L = 10k\Omega$ $C_L = 100pF$	—	3.5	—	V / μs
Equivalent Input Noise Voltage	V_n	—	$R_S = 100\Omega$, $f = 1kHz$	—	42	—	nV / \sqrt{Hz}

CHARACTERISTICS

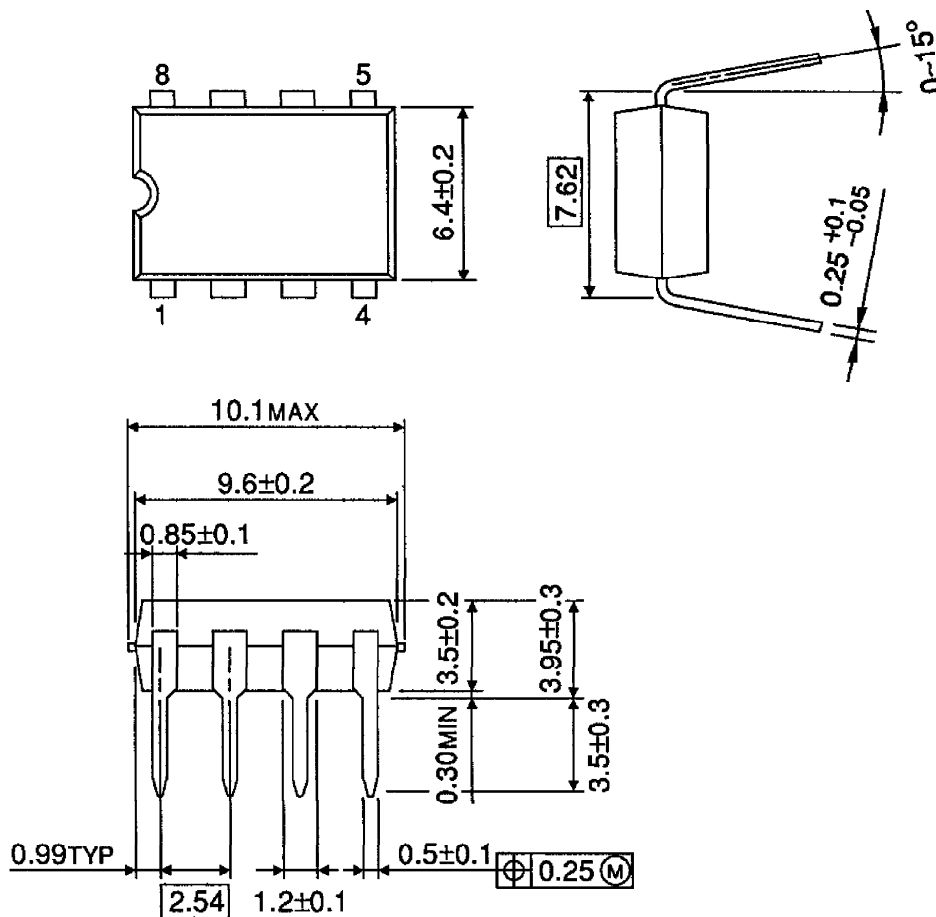






OUTLINE DRAWING
DIP8-P-300-2.54A

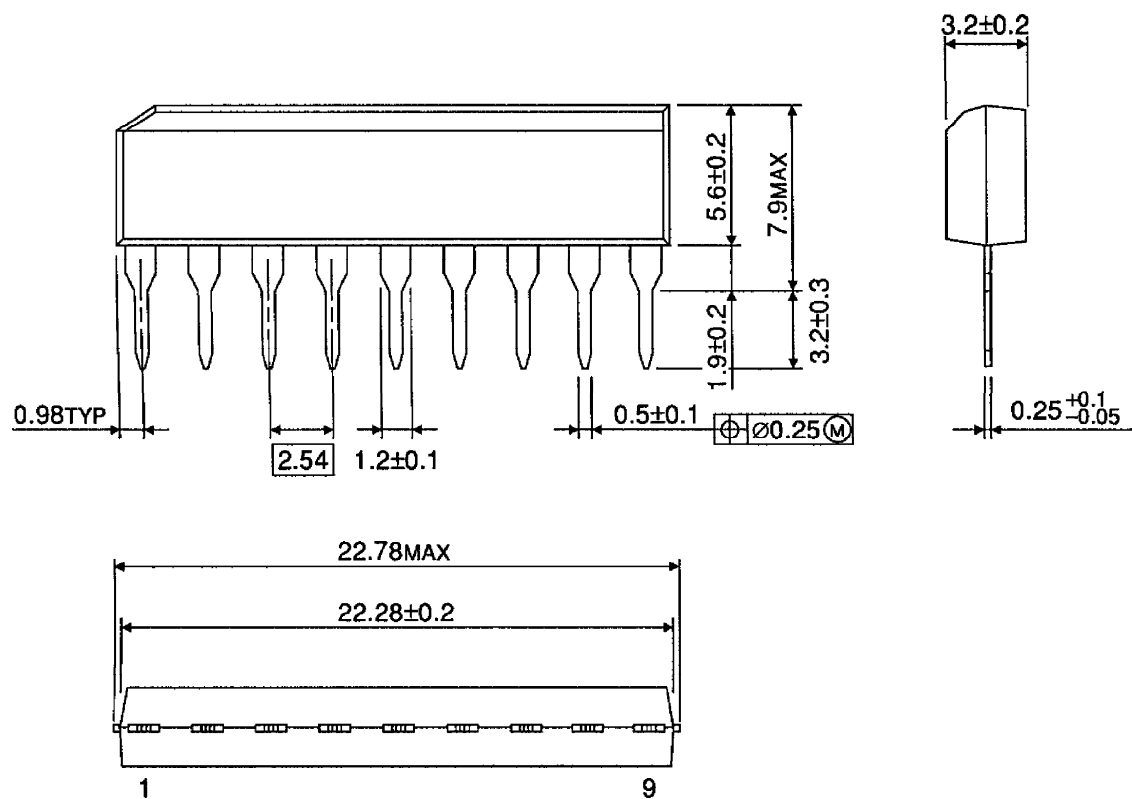
Unit : mm



Weight : 0.5g (Typ.)

OUTLINE DRAWING
SIP9-P-2.54A

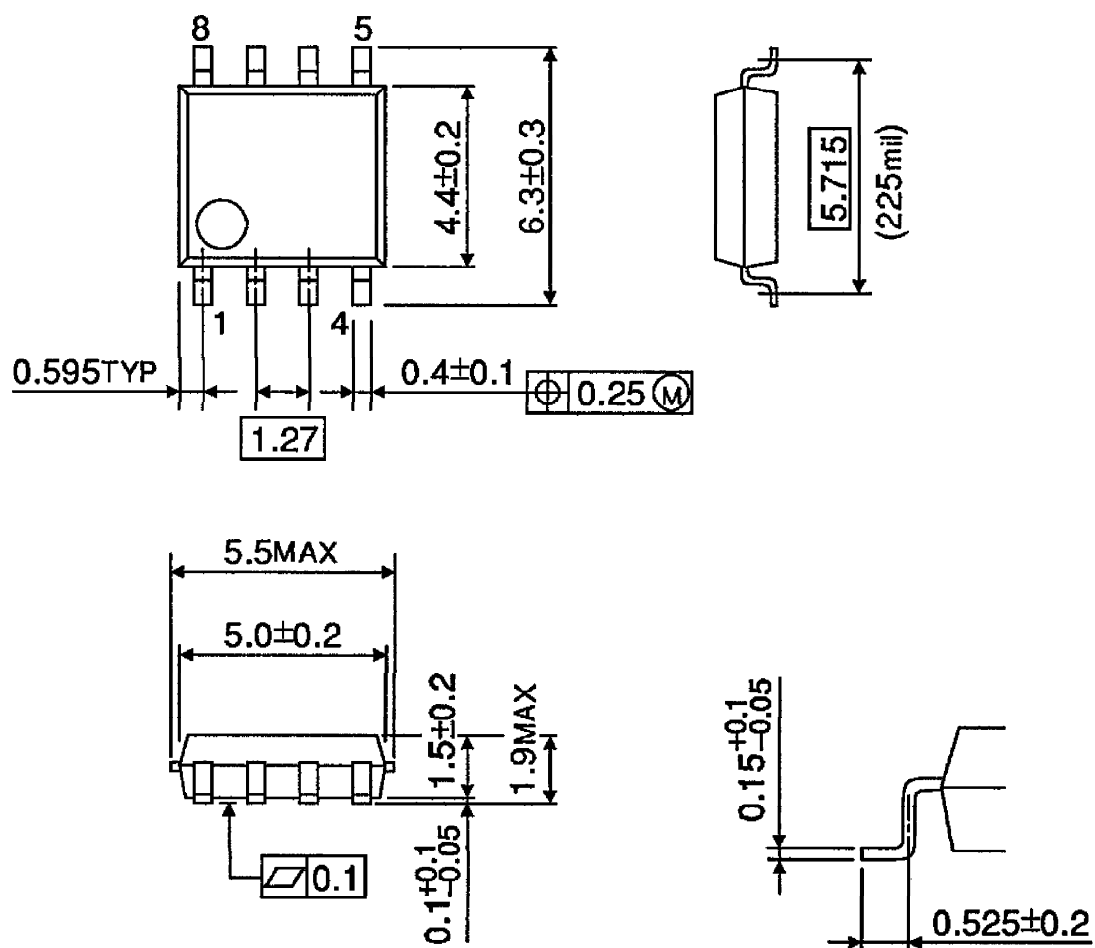
Unit : mm



Weight : 0.9g (Typ.)

OUTLINE DRAWING
SOP8-P-225-1.27

Unit : mm



Weight : 0.1g (Typ.)