

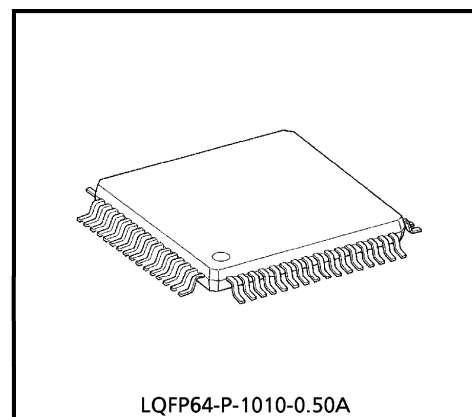
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VIDEO CAMERA CYLINDER MOTOR CONTROLLERS AND CAPSTAN MOTOR CONTROLLERS

The TB6519AF is a single-chip IC for video camera cylinder motor controllers and capstan motor controllers. The cylinder section is a soft-switching pre-driver based on a 3-phase full-wave sensorless driver and 180° trapezoidal wave commutation control. The capstan section is a soft-switching pre-driver based on 3-phase full-wave drive and pseudo-sine wave commutation control.

FEATURES

- Output current : 10 mA (MIN.) (At $V_{CC} = 3.5\text{ V}$)
- Operating voltage : $V_{CC} = 2.8\sim 5.5\text{ V}$
- Motor voltage : $V_M = 3.0\sim 12\text{ V}$

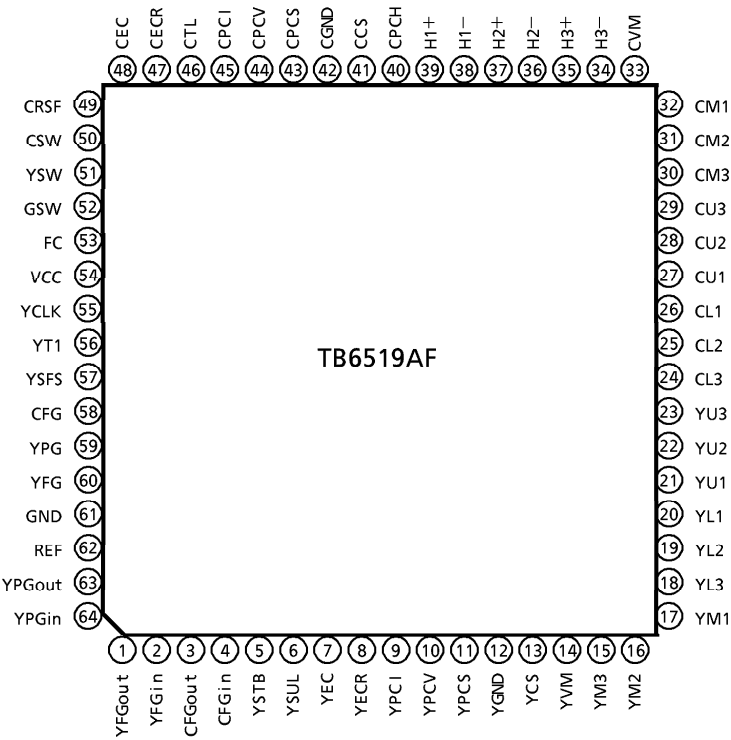


Weight : 0.34 g (Typ.)

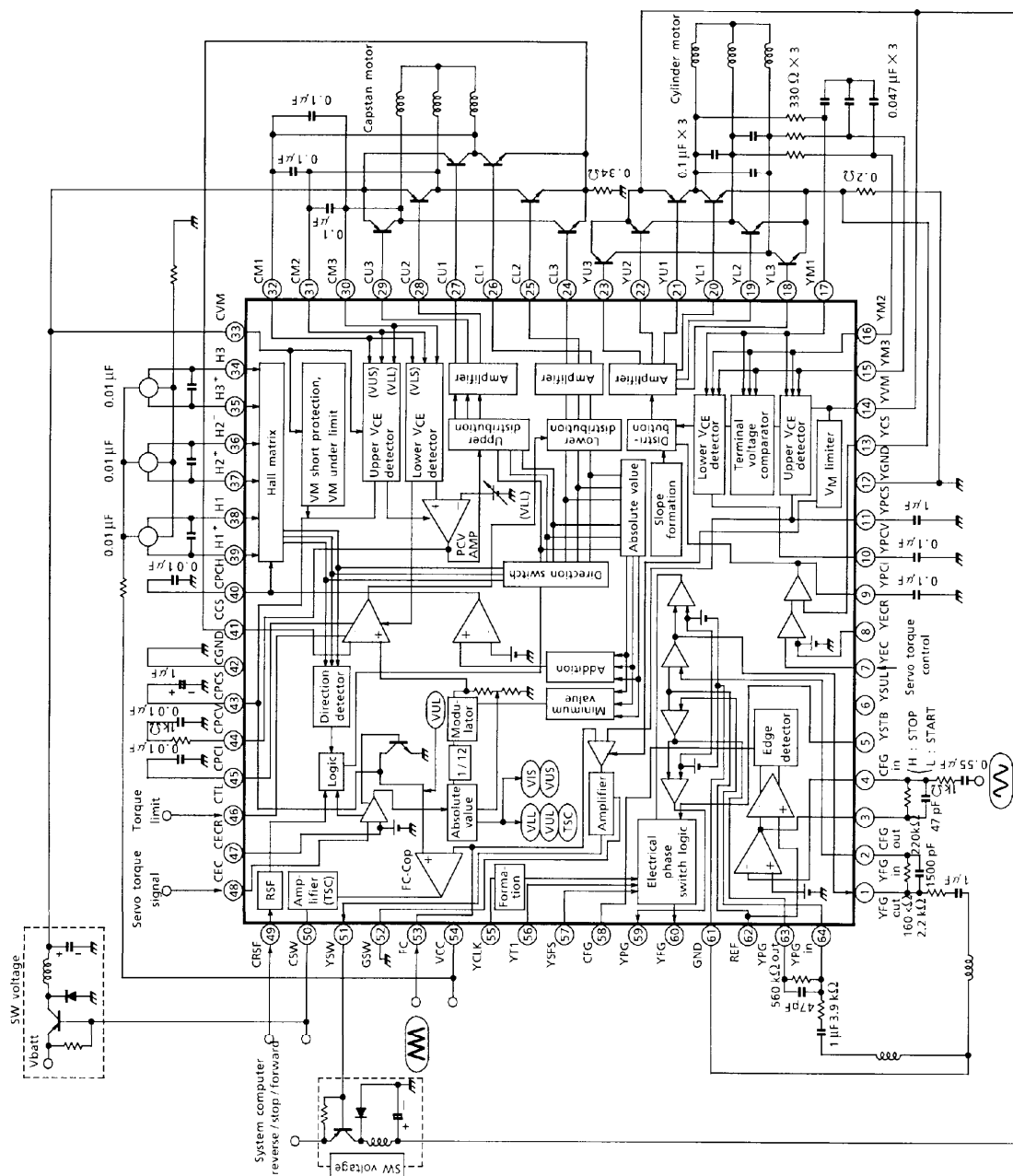
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PIN CONNECTION



BLOCK DIAGRAM



TB6519AF—3

PIN FUNCTION

PIN No.	SYMBOL	FUNCTION DESCRIPTION	PIN No.	SYMBOL	FUNCTION DESCRIPTION
1	YFGout	Cylinder part FG amplifier output terminal	34	H3 -	Capstan motor hall element input terminal
2	YFGin	Cylinder part FG input terminal	35	H3 +	⌀
3	CFGout	Capstan part FG amplifier output terminal	36	H2 -	⌀
4	CFGin	Capstan part FG input terminal	37	H2 +	⌀
5	YSTB	Cylinder part stand-by switch input terminal	38	H1 -	Capstan motor hall element input terminal
6	YSUL	Cylinder part sloop voltage terminal	39	H1 +	⌀
7	YEC	Cylinder part torque control input terminal	40	CPCH	Capstan part hall amplifier phase compensation
8	YECR	Cylinder part torque control reference input terminal	41	CCS	Capstan part current detection input terminal
9	YPCI	Cylinder part current feedback phase compensation	42	CGND	Capstan part ground terminal
10	YPCV	Cylinder part voltage feedback phase compensation	43	CPCS	Capstan part switching voltage control output
11	YPCS	Cylinder part switching voltage control output terminal	44	CPCV	Capstan part voltage feedback phase compensation
12	YGND	Cylinder part ground terminal	45	CPCI	Capstan part current feedback phase compensation
13	YCS	Cylinder part current detection input terminal	46	CTL	Capstan part torque limit
14	YVM	Cylinder motor power voltage terminal	47	CECR	Capstan part torque control reference voltage
15	YM3	Cylinder motor coil terminal	48	CEC	Capstan part torque control input terminal
16	YM2	⌀	49	CRSF	Capstan part direction control input terminal
17	YM1	⌀	50	CSW	Capstan part switching pre-driver output terminal
18	YL3	Cylinder motor lower side pre-drive output terminal	51	YSW	Cylinder part switching pre-driver output terminal
19	YL2	⌀	52	GSW	Switching voltage part ground terminal
20	YL1	⌀	53	FC	Switching comparator triangular-wave Input terminal
21	YU1	Cylinder motor upper side pre-drive output terminal	54	VCC	Capstan part ground terminal
22	YU2	⌀	55	YCLK	Cylinder part clock input terminal
23	YU3	⌀	56	YT1	Cylinder part test mode switch input terminal
24	CL3	Capstan motor low side pre-driver output terminal	57	YSFS	Cylinder part start-up frequency switch input
25	CL2	⌀	58	CFG	Capstan part FG wave output terminal
26	CL1	⌀	59	YPG	Cylinder part PG wave output terminal
27	CU1	Capstan motor upper side pre-driver output terminal	60	YFG	Cylinder part FG wave output terminal
28	CU2	⌀	61	GND	FG and PG part ground terminal
29	CU3	⌀	62	REF	FG and PG part reference voltage terminal
30	CM3	Capstan motor coil terminal	63	YPGout	Cylinder part PG amplifier output terminal
31	CM2	⌀	64	YPGin	Cylinder part PG input terminal
32	CM1	⌀			
33	CVM	Capstan motor mains power terminal			

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V _{CC}	6	V
Motor Supply Voltage (Note 1)	V _M	14	V
Supply I/O Voltage (Note 2)	V _{SWB}	14	V
Output Terminal Voltage (Note 3)	V _N	14	V
Input Terminal Voltage (Note 4)	V _I	-0.3~V _{CC} + 0.3	V
Power Dissipation	P _D	0.95 (Note 5)	W
Operating Temperature	T _{opr}	-20~75	°C
Storage Temperature	T _{stg}	-55~125	°C

(Note 1) Pin No. = 14, 33

(Note 2) Pin No. = 50, 51

(Note 3) Pin No. = 15, 16, 17, 21, 22, 23, 27, 28, 29, 30, 31, 32

(Note 4) Pin No. = 2, 4, 5, 7, 8, 13, 41, 46, 47, 48, 49, 53, 55, 56, 57, 62, 64

(Note 5) Element

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, Ta = 25°C, V_{CC} = 3.5 V)

Cylinder part

No.	CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
1	Supply Current (1)	I _{CC} (1)	1	Shared use of the cylinder area and capstan area during operations	—	17.9	30	mA
2	Supply Current (2)	I _{CC} (2)	1	During STB, during STOP (CAP)	—	10.6	20	mA
3	ECR Voltage	V _{ECR}	1		2.14	2.24	2.54	V
4	Torque Control Input Current	Y _{IEC}	1	YEC = 0 V	-5	-0.5	—	μA
5	Torque Control Input Offset Voltage	ΔEC	2		-100	-15	100	mV
6	I/O Gain	Y _{Gio}	2		0.13	0.15	0.17	
7	Maximum Output Voltage	Y _{CSmax}	2	R _{YCS} = 0.27 Ω	145	160	183	mV
8	Lower Side Output Voltage (1)	V _L (1)	3	YCS = 54 mV	0.2	0.39	0.6	V
9	Lower Side Output Voltage (2)	V _L (2)	3	YECR = 2.24 V, YEC = 0 V	0.45	0.66	0.85	V
10	Upper Side Drive Current	I _U	4		—	—	-10	mA
11	Lower Side Drive Current	I _L	4		10	—	—	mA
12	PCS Operating Point (1)	V _{PCS} (1)	5	YEC = YECR = 2.24 V V _{PCS} = 1.75 V	0.36	0.47	0.58	V

Cylinder part

No.	CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
13	PCS Operating Point (2)	V _{PCS} (2)	5	YEC = 0 V, YECR = 2.24 V V _{PCS} = 1.75 V	0.60	0.79	0.98	V
14	PCS Gain	YG _{PCS}	5		4.5	6.5	8.5	
15	SW Reg Drive Current (1)	I _{SW} (1)	5	VM1 = 6 V, YEC = YECR = 2.24 V	3	4.5	—	mA
16	SW Reg Drive Current (2)	I _{SW} (2)	5	VM1 = 6 V YEC = 0 V, YECR = 2.24 V	11	16.6	—	mA
17	SW Reg Comparator Offset Voltage	ΔV _{FC}	5		− 5	15	25	mV
18	FG Amplifier Gain	G _{FG}	6	V _{p-p} = 1.5 mV, f = 1 kHz	45	—	—	dB
19	YFG High Level	YFG (H)	7	I _{YFG} = − 100 μA	2.0	3.4	—	V
20	YFG Low Level	YFG (L)	7	I _{YFG} = 100 μA	—	0.1	1.5	V
21	PG Amplifier Open Loop Gain	G _{PG}	—		—	70	—	dB
22	PG Amplifier Offset Voltage	ΔP _{Gin}	7		0.45	0.5	0.6	V
23	YPG High Level	YPG (H)	7	I _{YPG} = − 10 μA	2.0	3.0	—	V
24	YPG Low Level	YPG (L)	7	I _{YPG} = 100 μA	—	0.03	1.0	V
25	Stand-By Voltage	STB _{on}	8		2.15	—	—	V
26	Stand-By Release Voltage	STB _{off}	8		—	—	1.0	V
27	Stand-By Input Current	I _{STB}	8	V _{STB} = 0 V	− 100	− 35	—	μA
28	Start-Up Phase Switch Frequency 7.5 Hz Setting Input	SFS (L)	9		—	—	1.05	V
29	Start-Up Phase Switch Frequency 15 Hz Setting Input	SFS (H)	9		2.45	—	—	V
30	YVM Under Limit	YVML	5		1.87	2.5	3.13	V
31	YVM Short Protection	YVMS	5		0.26	0.76	1.00	V
32	Current Leak When Mains Power Off	I _{ML}	10	YVM = 6 V	—	3	10	μA
33	Output Idle Voltage	YCS _{idle}	2	R _{YCS} = 0.27 Ω	—	0	5	mV

Capstan area

No.	CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
34	Torque Control Input Current	CEC	11	CEC = CECR = 1.75 V	− 2	− 1	—	μA
35	Torque Control Reference Voltage	CE _{CR}	11		1.55	1.73	1.95	V
36	Torque Control Input Voltage	CE _C	12		0.5	—	3.0	V
37	Output Maximum Voltage	CCS _{max}	12	R _{CCS} = 0.34 Ω	0.19	0.23	—	V
38	Torque Control I/O Gain	CG _{io}	12		0.21	0.24	0.27	

Capstan area

No.	CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
39	Output Idle Voltage	CCSidle	12		—	0	4	mV
40	Torque Control Input Offset	CECofs	12		− 100	15	100	mV
41	Torque Control Dead Zone	CECdz	12		30	77	130	mV
42	Low Side V_{CE} Voltage (1)	CVLL (1)	13	CCS = 60 mV	0.22	0.28	0.50	V
43	Low Side V_{CE} Voltage (2)	CVLL (2)	13	CEC = 0 V, CTL = 1.0 V	0.40	0.50	0.80	V
44	Hall Element Permissible Input Voltage	Hin	14		1.2	—	2.0	V
45	Hall Element Input Conversion Offset	Hofs	15		− 8	− 1	8	mV
46	TL-CS Offset	TLoFs	16	CTL = 20 mV	6	9.5	14	mV
47	Forward Rotation Control Voltage	Vf	17		—	—	0.87	V
48	Stop Control Voltage	Vs	17		1.27	—	2.23	V
49	Reverse Rotation Control Voltage	Vr	17		2.90	—	—	V
50	Ripple Cancel Rates	R	18	CCS = 60 mV	8	13	18	%
51	Upper Side Drive MAX Current	CI _U	19		10	24	—	mA
52	Low Side Drive MAX Current	CI _L	19		—	− 16	− 10	mA
53	SW Power Voltage Input Offset	CSWoFs	21		− 20	11	20	mV
54	SW Power Voltage Control Output Gain	CGpCS	20		6	8	10	
55	SW Power Voltage Control Output Voltage (1)	VUD (1)	20	CEC = CECR, CPCS = 1.7 V	0.3	0.40	0.65	V
56	SW Power Voltage Control Output Voltage (2)	VUD (2)	20	CEC = 0 V, CTL = 0.2 V CPCS = 1.7 V	0.47	0.62	1.10	V
57	SW Power Voltage Output MAX Current	CI _{SWB}	20	CEC = 0 V, CTL = 0.2 V	15	22	—	mA
58	FG Amplifier Standard Voltage	CFG _{ref}	11		1.7	2.0	2.3	V
59	FG Amplifier Loop Gain	CG _{FG}	22	External 1 k Ω , 220 k Ω Input 3 mV _{p-p} , 1 kHz	45	50	—	dB
60	FG Amplifier Output Voltage High Level	CFG _H	22		3	3.5	—	V
61	FG Amplifier Output Voltage Low Level	CFG _L	22		—	0.01	0.5	V
62	V _M Under Limit	CV _{ML}	23		1.13	1.52	1.88	V
63	V _M Short Protection	CV _{MS}	23		0.26	0.45	1.00	V

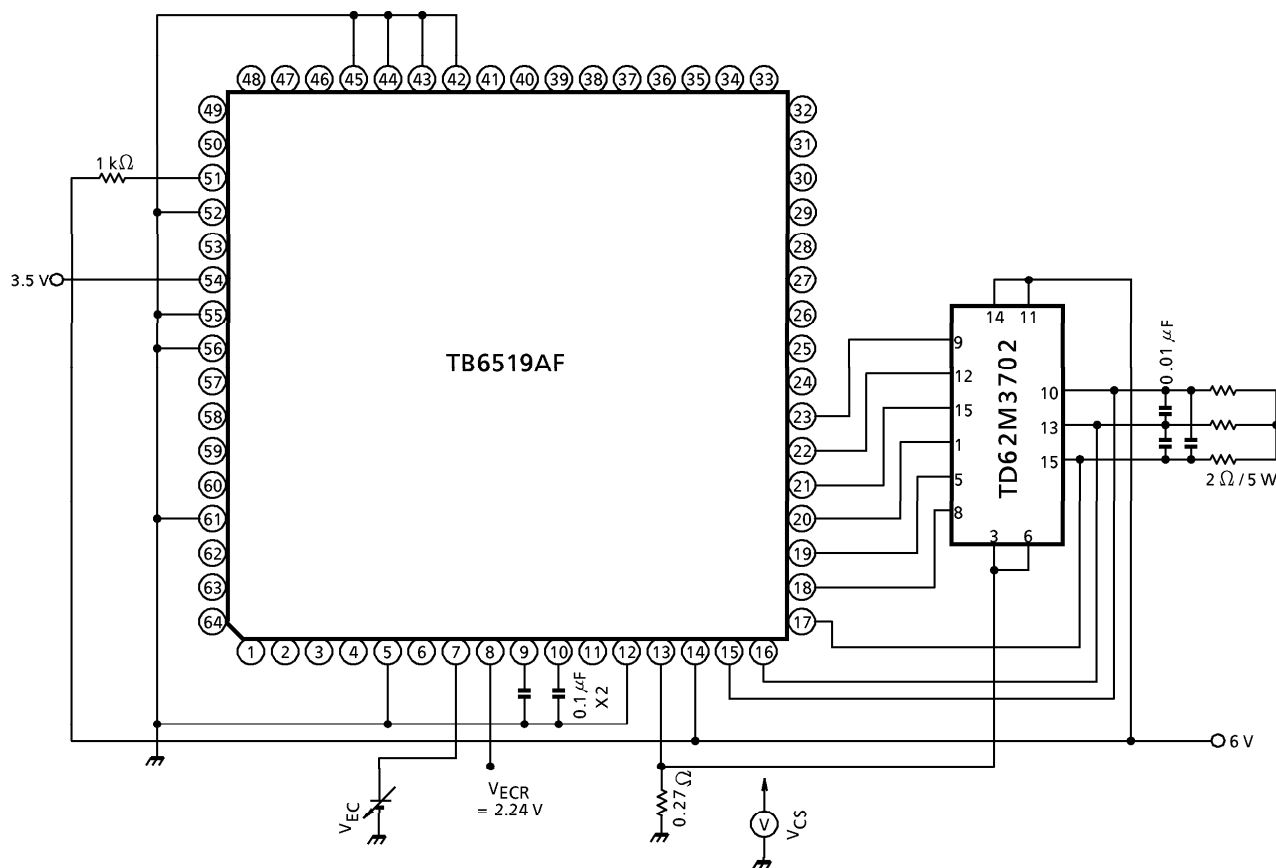
Set YSTB = 0 V, YEC = 2.24 V, YECR = 0 V and CRSF = 0 V and then measure the current flowing into the V_{CC} terminal.

Set YSTB = 3.5 V, YEC = YECR = 2.24 V and CRSF = OPEN and then measure the current flowing into the V_{CC} terminal.

Measure the potential of pin ⑧.

Measure the current flowing into pin ⑦ when YEC = 0 V and YECR = 2.24 V.

TEST CIRCUIT 2. ΔEC , YG_{io}, YCS_{max}, YCS_{idle}

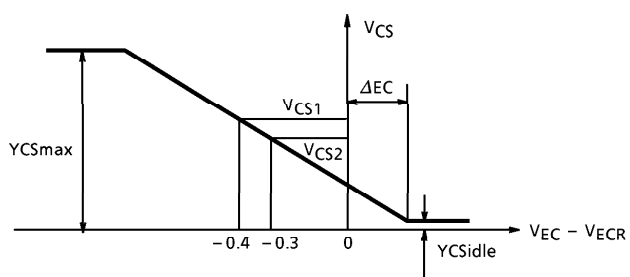


No. 5 ΔEC, No. 6 YGio, No. 7 YCSmax, No. 33 YCSidle

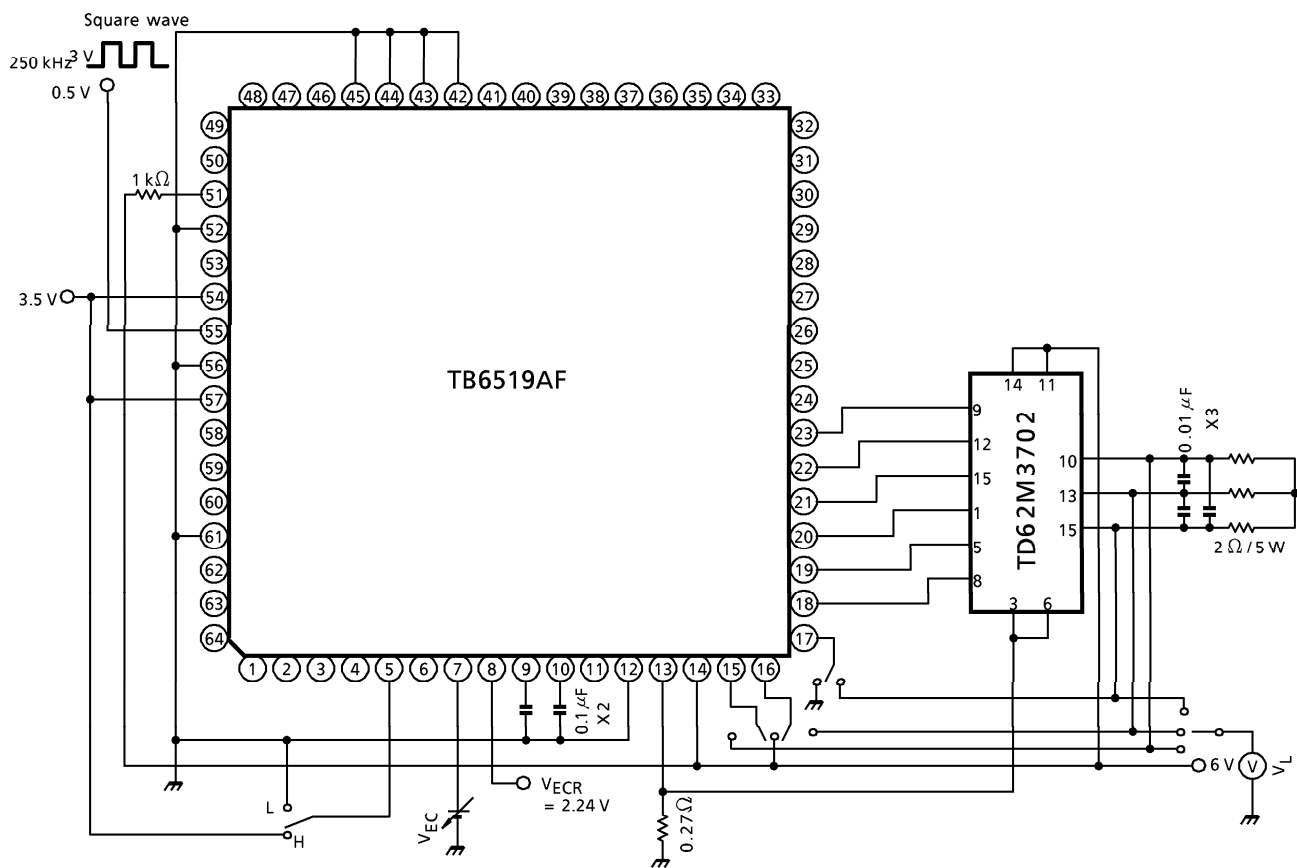
Set YECR = 2.24 V, change YEC from 0 V to 3 V and then measure the potential of pin ⑬.

$$\Delta EC = V_{EC} - V_{ECR} \quad (V_{CS} \approx 0 \text{ V})$$

$$Y_{\text{Gio}} = \frac{V_{\text{CS1}} - V_{\text{CS2}}}{0.1 \text{ V}}$$



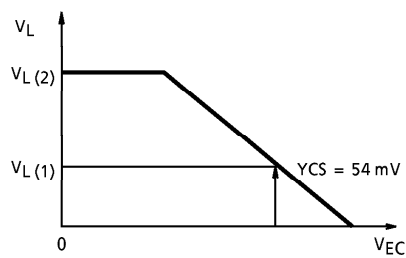
TEST CIRCUIT 3. $V_L(1)$, $V_L(2)$



No. 8 $V_L(1)$, No. 9 $V_L(2)$

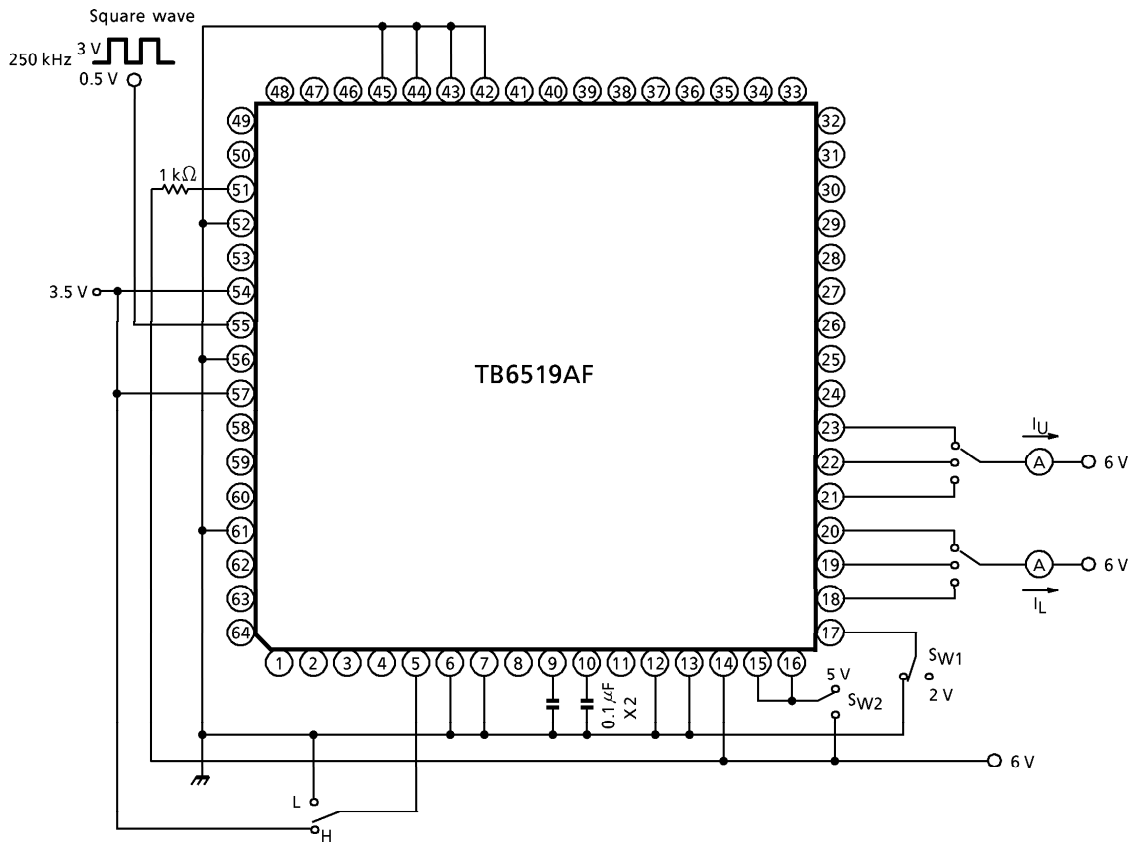
Change the YSTB terminal from H to L with YMI = 0 V, YM2 = 6 V and YM3 = 6 V and then enter the following clock counts into the YCLK terminal in order to set the drive angle.

Connect the YM1, YM2 and YM3 terminals to PWTR after setting the drive angle and then carry out the measurement.



CLOCK	80	150	270
Terminal	YM3	YM1	YM2

TEST CIRCUIT 4. I_U, I_L

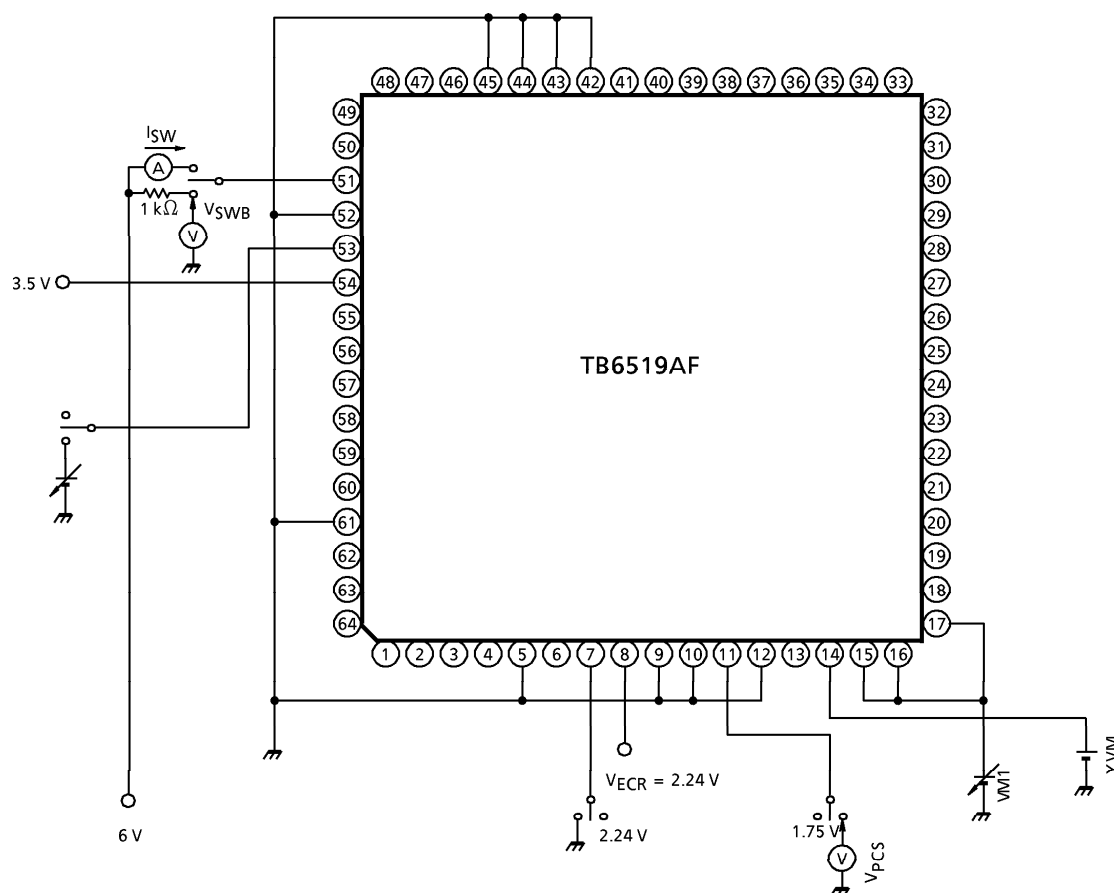


No. 10 I_U , No. 11 I_L

Change the YSTB terminal from H to L and then enter the following clock counts into the YCLK terminal in order to set the drive angle.

CLOCK	50		150		280	
Terminal	YU1	YL3	YU2	YL1	YU3	YL2
S_{W1}	0V	2V	0V	2V	0V	2V
S_{W2}	5V	6V	5V	6V	5V	6V

TEST CIRCUIT 5. $V_{PCS}(1)$, $V_{PCS}(2)$, $Y_{G_{PCS}}$, $I_{SW}(1)$, $I_{SW}(2)$, ΔV_{FC} , Y_{VML} , Y_{VMS}



No. 12 $V_{PCS}(1)$

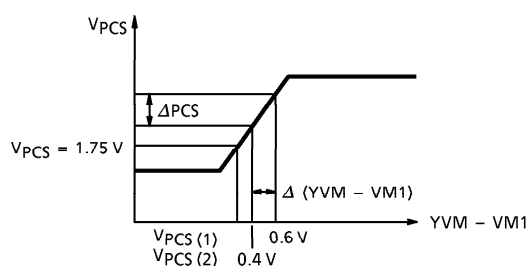
Set $Y_{VM} = 6V$ and $Y_{EC} = 2.24V$ and then measure the $VM1$ for which $V_{PCS} = 1.75V$.

No. 13 $V_{PCS}(2)$

Set $Y_{VM} = 6V$ and $Y_{EC} = 0V$ and then measure the $VM1$ for which $V_{PCS} = 1.75V$.

No. 14 $Y_{G_{PCS}}$

Set $Y_{VM} = 6V$ and $Y_{EC} = 2.24V$ and then acquire $Y_{G_{PCS}}$ from the amount of V_{PCS} voltage change when $(Y_{VM} - VM1)$ is changed from $0.4V$ to $0.6V$.



$$Y_{G_{PCS}} = \frac{\Delta PCS}{\Delta (Y_{VM} - VM1)}$$

No. 15 $I_{SW}(1)$

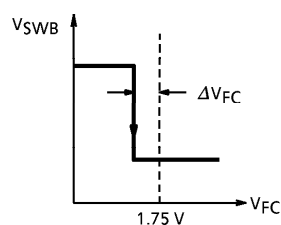
Set $FC = 3\text{ V}$ and $YEC = 2.24\text{ V}$ and then measure the current flowing into the YSW terminal.
($YVM = VM1 = 6\text{ V}$)

No. 16 $I_{SW}(2)$

Set $FC = 3\text{ V}$ and $YEC = 0\text{ V}$ and then measure the current flowing into the YSW terminal.
($YVM = VM1 = 6\text{ V}$)

No. 17 ΔV_{FC}

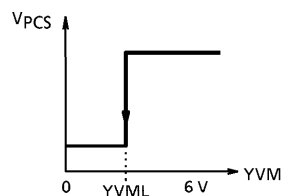
Set $YPCS = 1.75\text{ V}$, change FC from 0 V and then measure the difference in V_{FC} and V_{PCS} when V_{SWB} changes from H to L.



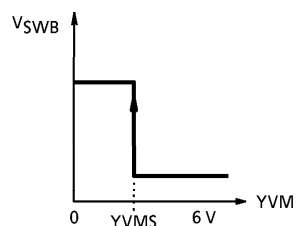
$$\Delta V_{FC} = V_{PCS} - V_{FC}$$

No. 30 $YVML$

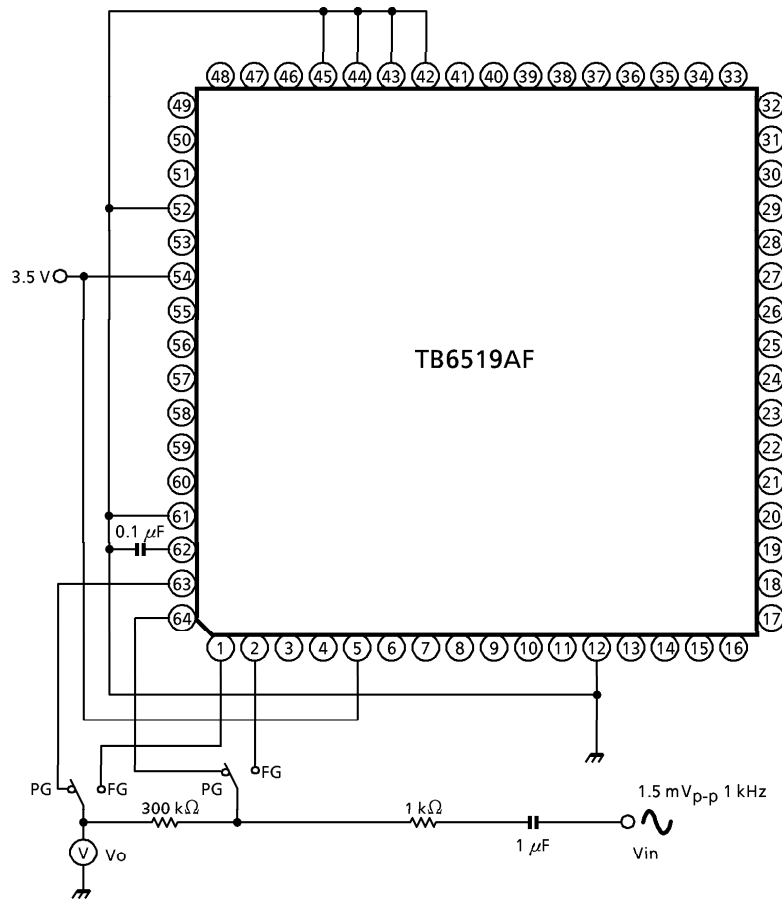
Set $FC = 3\text{ V}$, $YEC = 2.24\text{ V}$ and $VM1 = YVM - 1\text{ V}$, change YVM from 6 V and then set $YVML$ when V_{PCS} changes from H to L.

No. 31 $YVMS$

Set $FC = 3\text{ V}$, $YEC = 0\text{ V}$ and $VM1 = 6\text{ V}$, change YVM from 6 V and then set $YVMS$ when V_{SWB} changes from H to L.



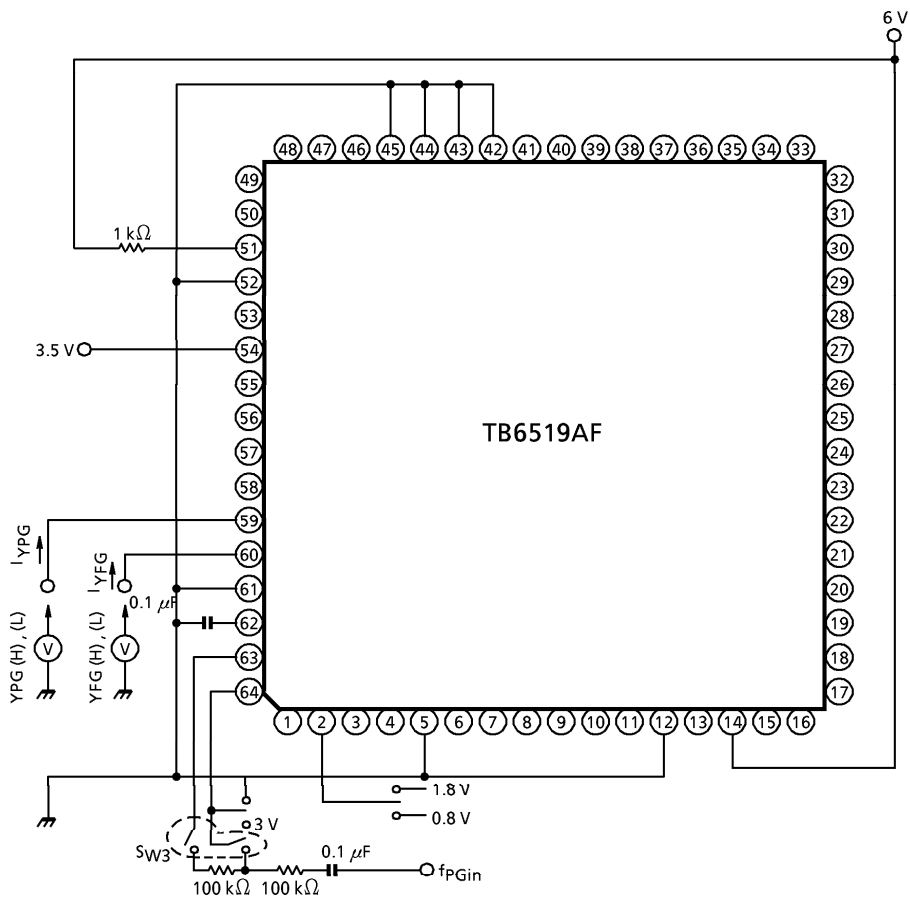
TEST CIRCUIT 6. G_{FG} , G_{PG}



No. 18 G_{FG}

Set the SW to FG, measure V_o when $V_{in} = 1.5 \text{ mV}_{p-p}$ at 1 kHz and acquire $G_{FG} = 20 \log (V_o / V_{in})$.

TEST CIRCUIT 7. YFG (H), YFG (L), Δ PGin, YPG (H), YPG (L)



No. 19 YFG (H)

Measure the potential of YFG when a current of $I_{YFG} = -100 \mu A$ is flowing after 1.8 V has been applied to YFGin and YFG has been set at H.

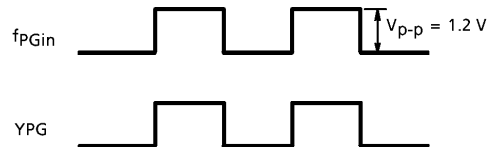
No. 20 YFG (L)

Measure the potential of YFG when a current of $I_{YFG} = 100 \mu A$ is flowing after 0.8 V has been applied to YFGin and YFG has been set at L.

No. 22 Δ PGin

Set SW3 on, input a 10 kHz square wave from f_{PGin} , set the f_{PGin} V_{p-p} to 1.2 V (Δ PGin = 0.6 V) and confirm that the pin 59 is operating.

Also, set V_{p-p} to 0.9 V (Δ PGin = 0.45 V) and confirm that the YPG terminal is not operating.

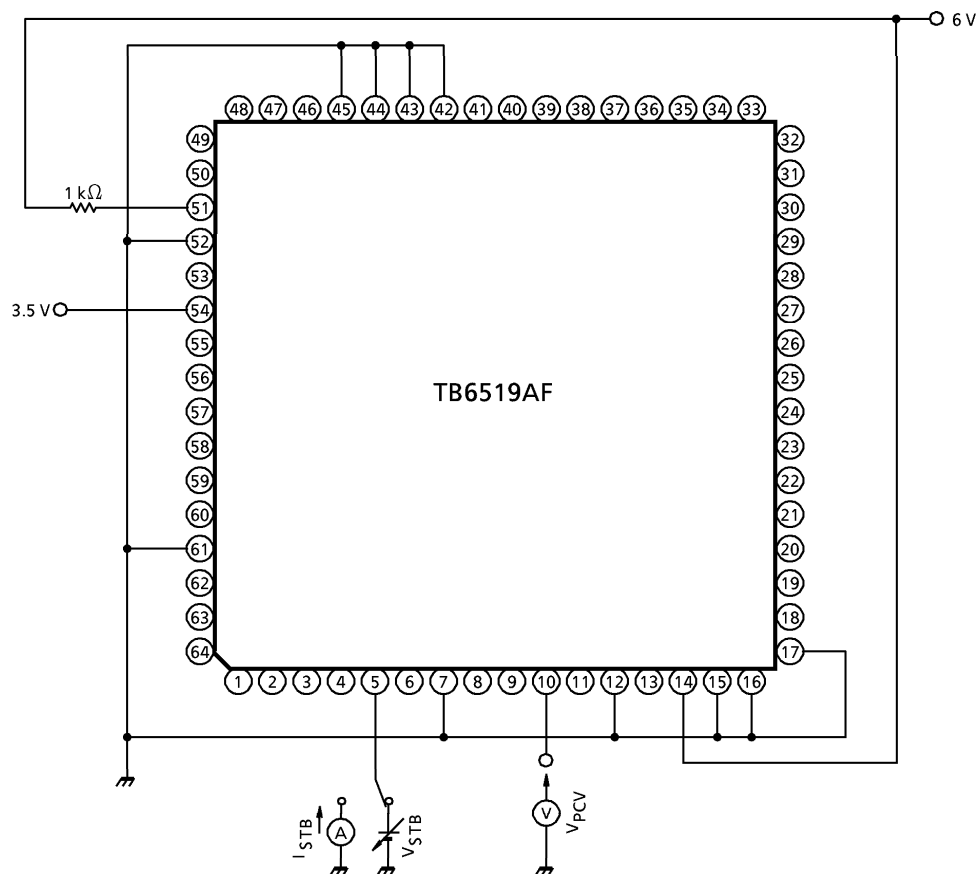


No. 23 YPG (H)

Measure the potential of YPG when a current of $I_{YPG} = -100 \mu A$ is flowing after 3 V has been applied to YPGin and YPG has been set at H.

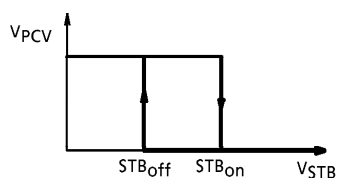
No. 24 YPG (L)

Measure the potential of YPG when a current of $I_{YPG} = 100 \mu A$ is flowing after 0 V has been applied to YPGin and YPG has been set at L.

TEST CIRCUIT 8. STB_{on} , STB_{off} , I_{STB} No. 25 STB_{on} , No. 26 STB_{off}

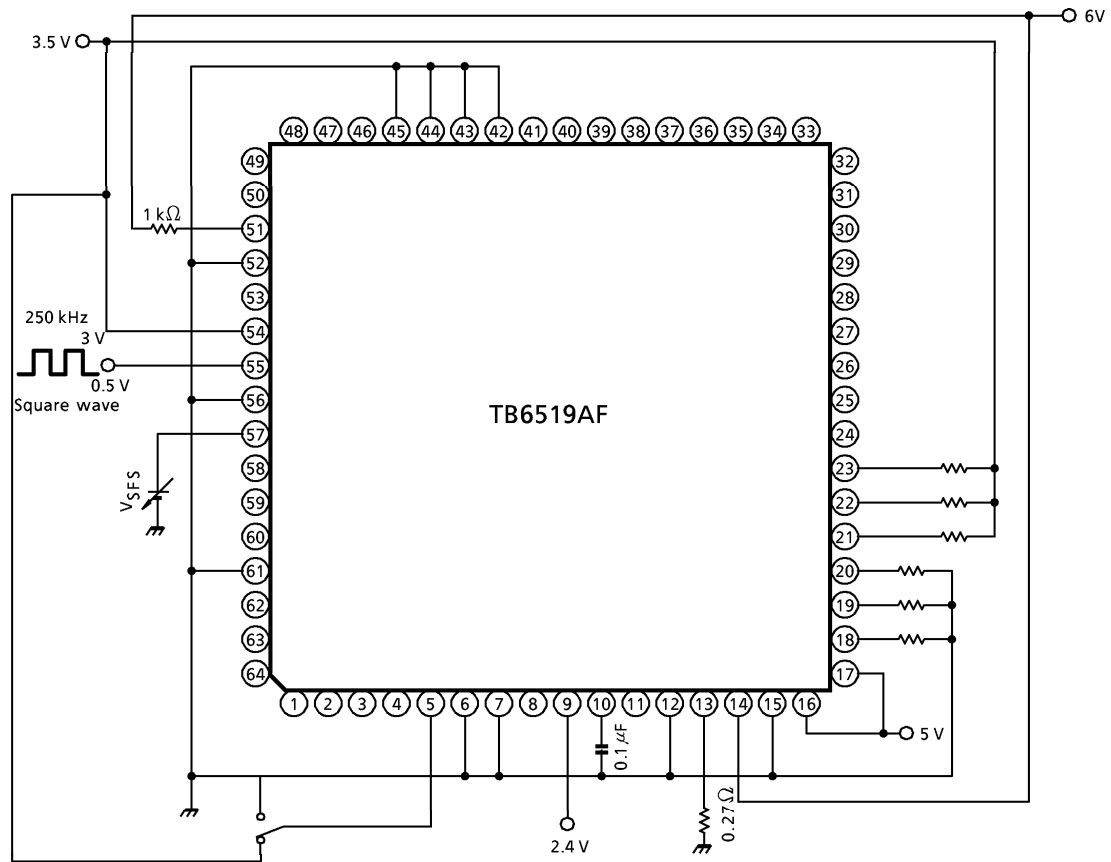
Change V_{STB} from 0 V to 3.5 V, and then from 3.5 V to 0 V, and measure V_{PCV} .

V_{STB} becomes STB_{on} when V_{PCV} changes from H to L, and becomes STB_{off} when V_{PCV} changes from L to H.

No. 27 I_{STB}

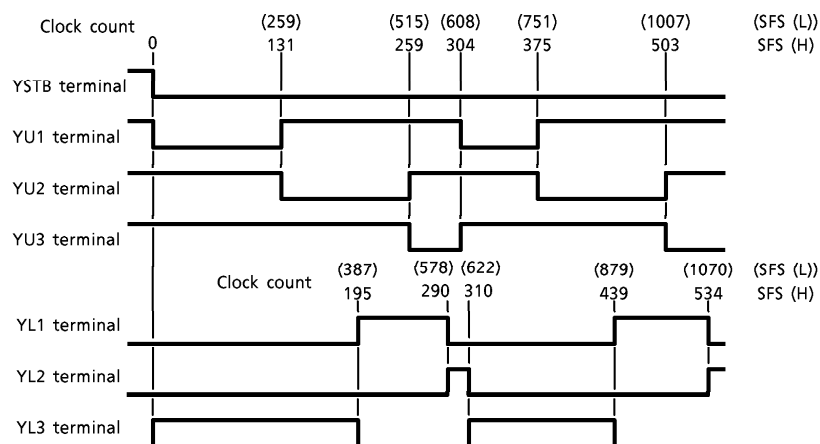
Measure I_{STB} when $V_{STB} = 0$ V.

TEST CIRCUIT 9. SFS (L), SFS (H)

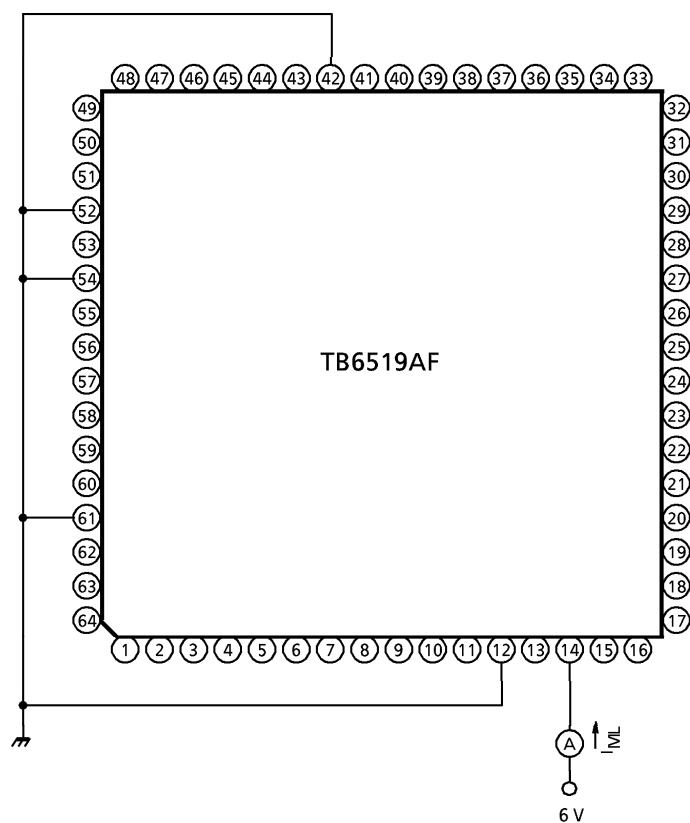


No. 28 SFS (L), No. 29 SFS (H)

Change V_{SFS} from 0 V to 3.5 V and measure the potential of YU1~3 and YL1~3.



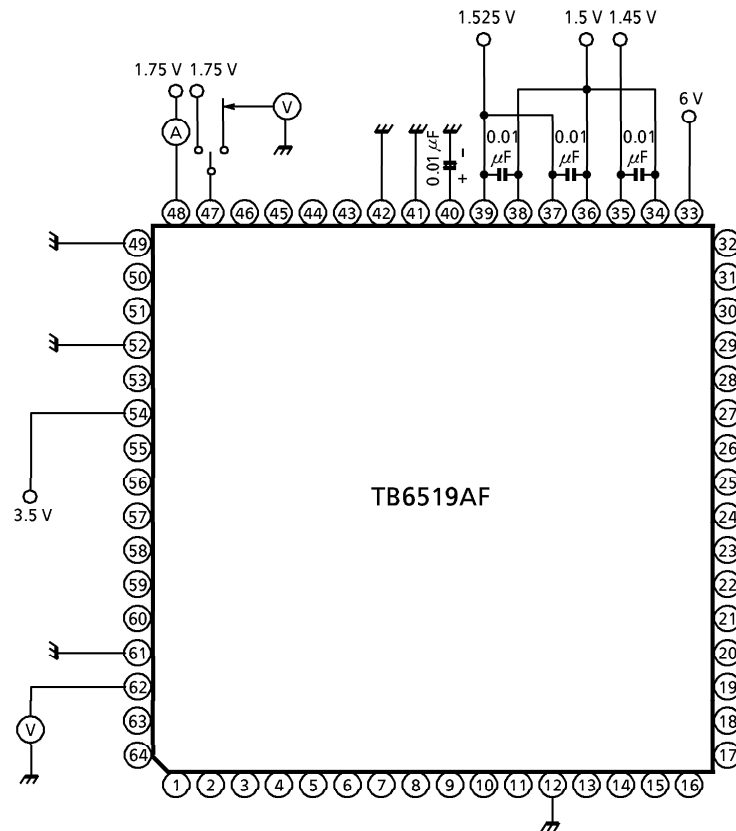
TEST CIRCUIT 10. I_{ML}



No. 32 I_{ML}

Measure the current that flows into pin ⑭ when $YVM = 6V$.

TEST CIRCUIT 11. Cl_{EC} , CE_{CR} , CFG_{ref}



No. 34 Cl_{EC}

Measure the current that flows into the CEC terminal with $CEC = 1.75\text{ V}$ and $CECR = 1.75\text{ V}$.

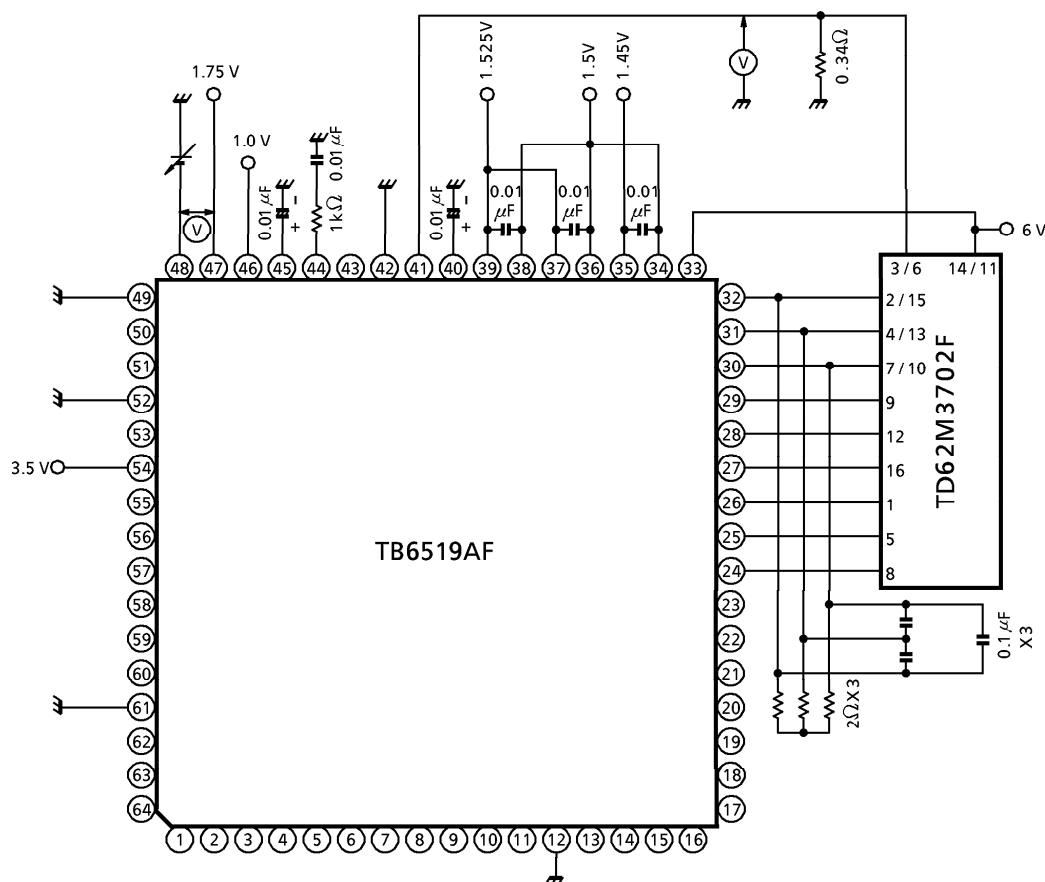
No. 35 CE_{CR}

Measure the voltage of the CECR terminal.

No. 58 CFG_{ref}

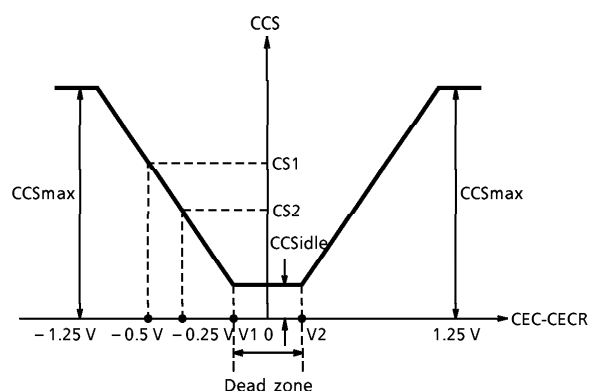
Measure the voltage of the REF terminal.

TEST CIRCUIT 12. CECm, CCSmaxm, CGiom, CCSidlem, CECofsm, CECdz



No. 36 No. 37 No. 38 No. 39 No. 40 No. 41

Set CTL = 1.0 V and CECR = 1.75 V, change CEC from 0 V to 3.5 V, measure the potential of the CCS terminal and confirm the V characteristics.



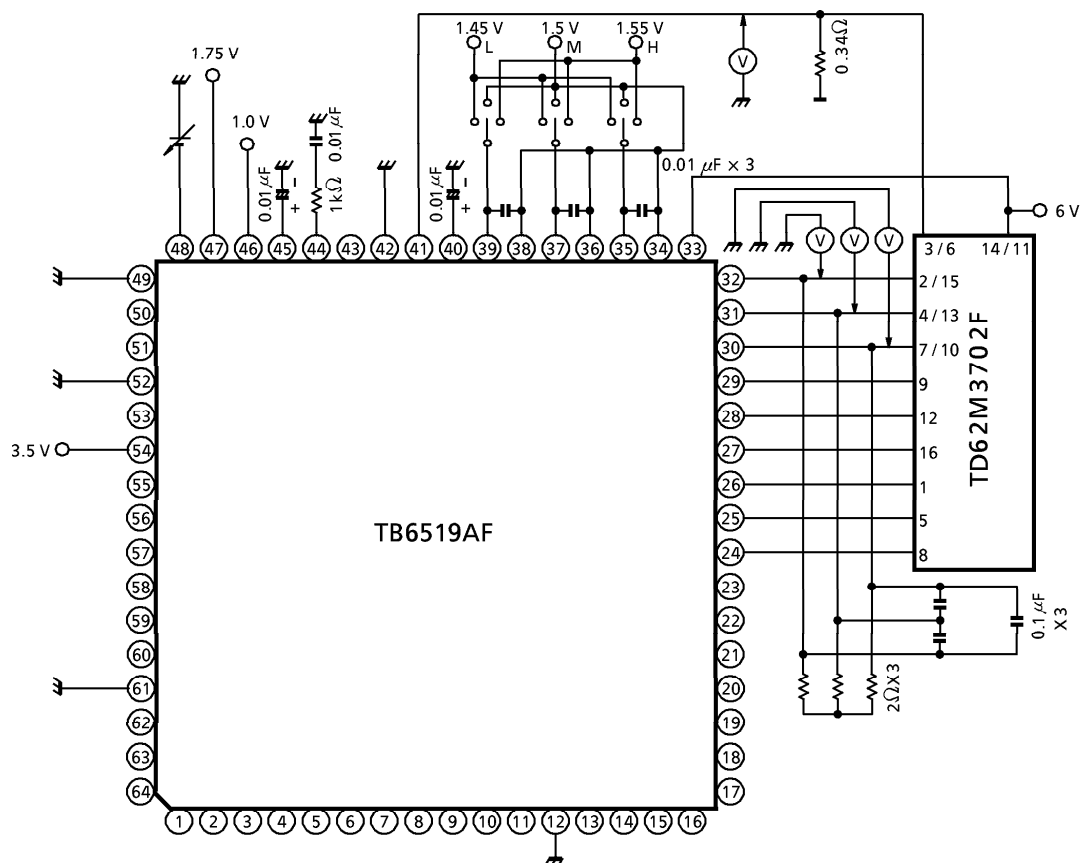
$$CGio = \frac{CS1 - CS2}{0.25 V}$$

CCSidle : The CS potential within the dead zone

$$CECofs = \frac{V1 + V2}{2}$$

$$CECdz = V2 - V1$$

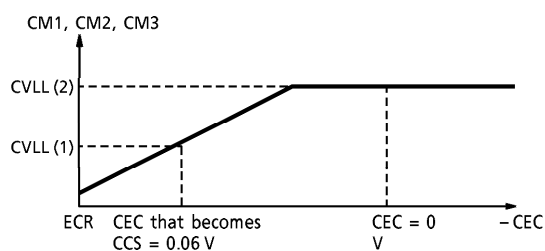
TEST CIRCUIT 13. CVLL (1), CVLL (2)



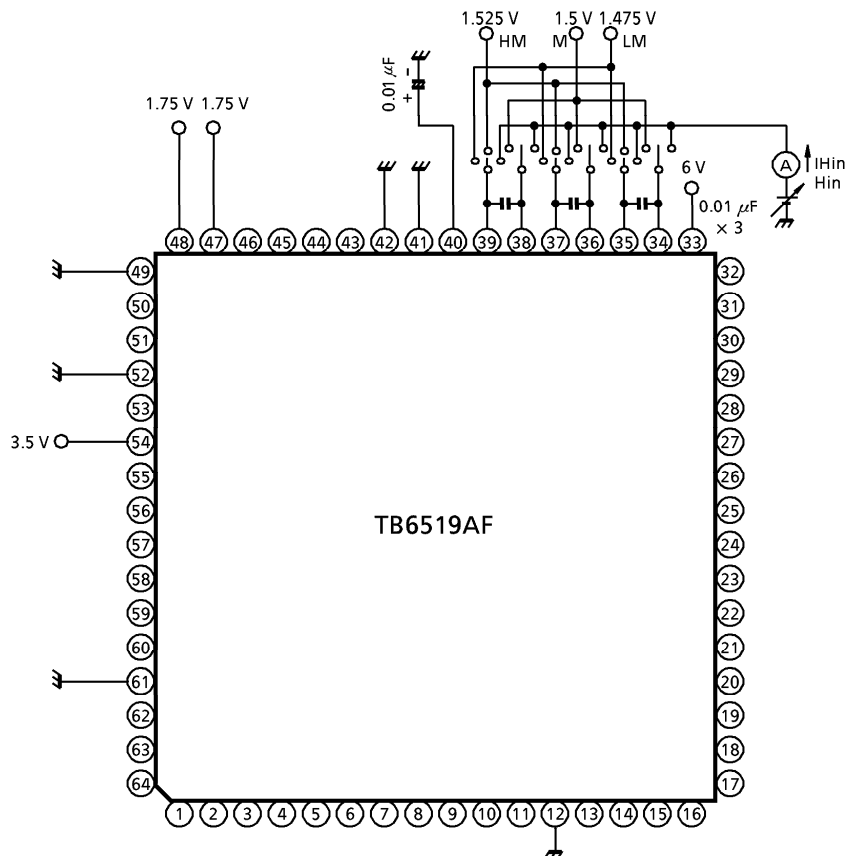
No. 42 CVLL (1), No. 43 CVLL (2)

Perform the settings laid out in the table below and measure the potential of the CM1, CM2 and CM3 terminals when the CEC voltage is adjusted to $CCS = 0.06\text{ V}$ and when $CEC = 0\text{ V}$.

	H1 +	H2 +	H3 +	TEST TERMINAL
Setting 1	H	L	M	CM1
Setting 2	M	H	L	CM2
Setting 3	L	M	H	CM3



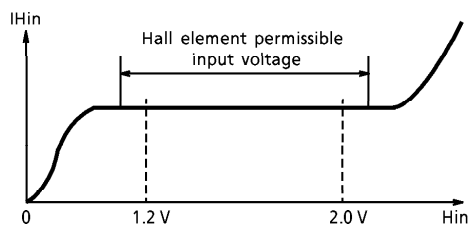
TEST CIRCUIT 14. H_{in}



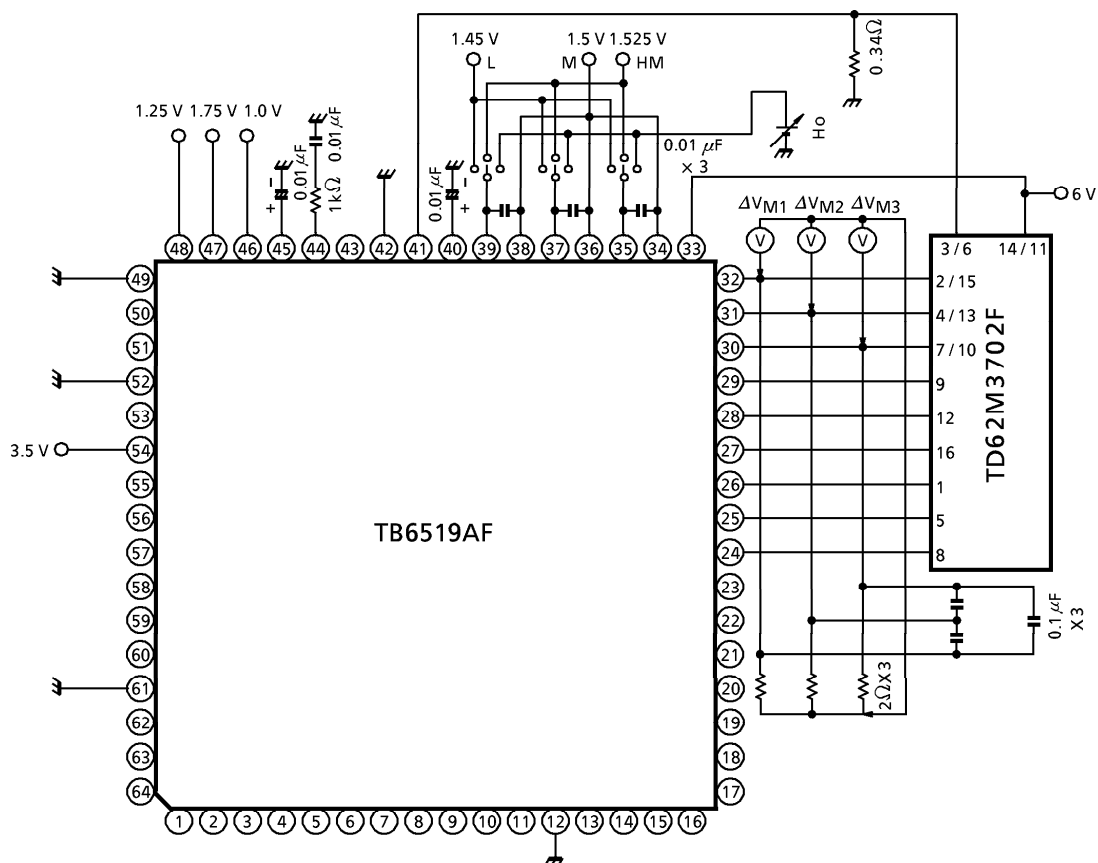
No. 44 Hin

Perform the settings laid out in the table below and then measure the voltage range of the I_{Hin} that does change rapidly in accordance with changes in the H_{in}.

	H1 +	H1 -	H2 +	H2 -	H3 +	H3 -
Setting 1	Hin	Hin	HM	M	LM	M
Setting 2	LM	M	Hin	Hin	HM	M
Setting 3	HM	M	LM	M	Hin	Hin



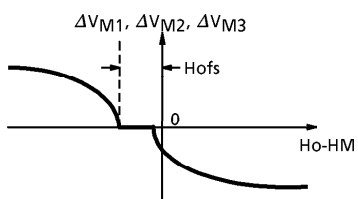
TEST CIRCUIT 15. Hofs



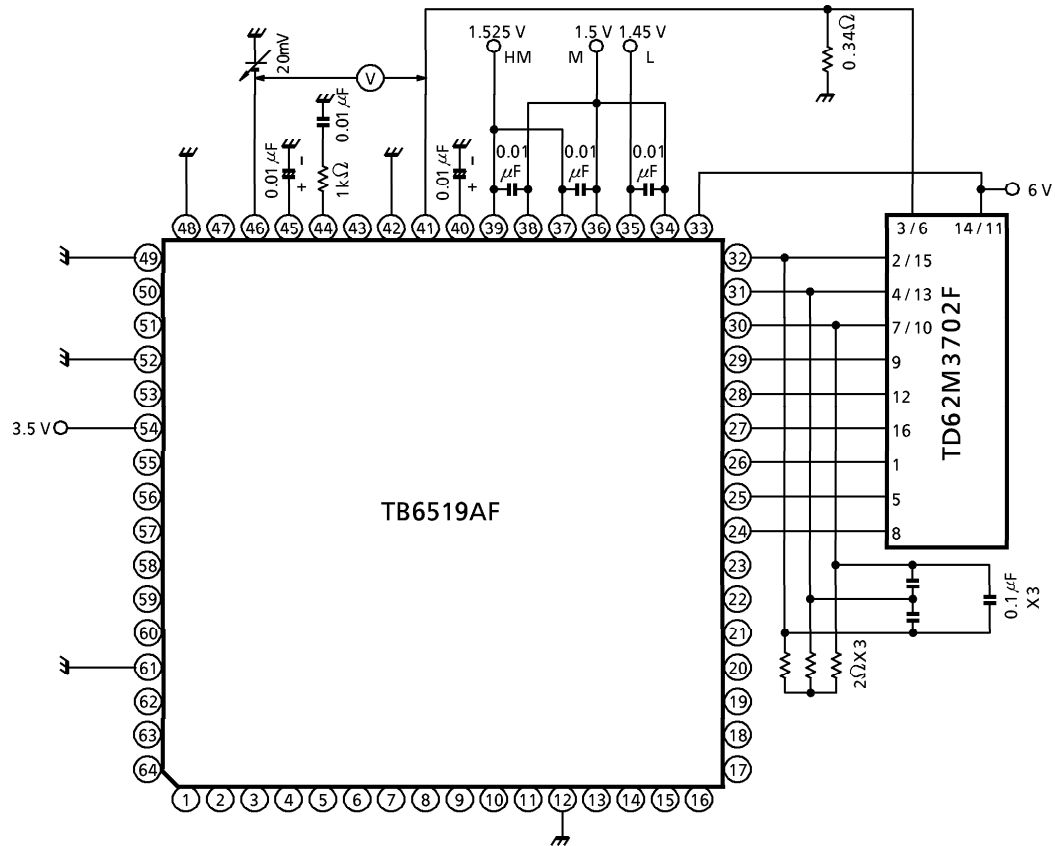
No. 45 Hofs

Perform the settings laid out in the table below and then measure the hall element input conversion offset.

	H1 +	H2 +	H3 +	OFFSET MEASUREMENT
Setting 1	Ho	HM	L	$\Delta V_{M1} = 0$ difference between H1 + and H2 +
Setting 2	L	Ho	HM	$\Delta V_{M2} = 0$ difference between H2 + and H3 +
Setting 3	HM	L	Ho	$\Delta V_{M3} = 0$ difference between H3 + and H1 +

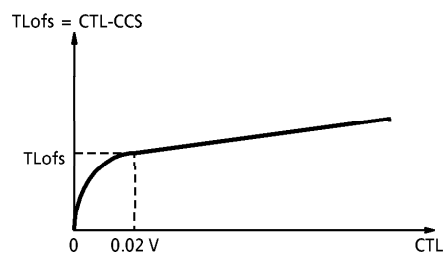


TEST CIRCUIT 16. TLofs



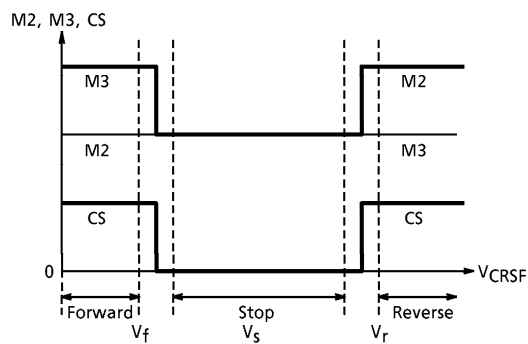
No. 46 TLofs

Measure the potential differential (CTL-CCS) of the CTL and CCS terminals when CTL = 0.02 V.



No. 47 Vf, No. 48 Vs, No. 49 Vr

Change CRSF from 0V to 3.5 V, acquire the characteristics indicated in the following diagram and measure the threshold voltage.

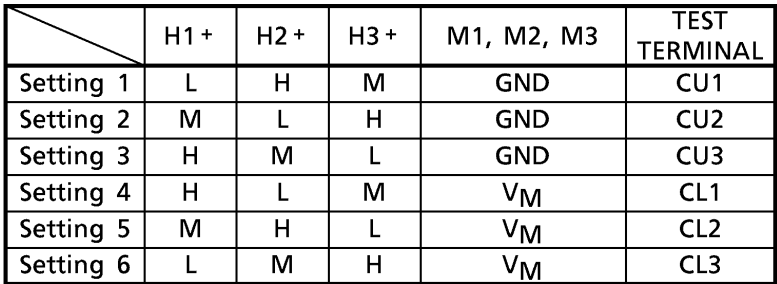


Adjust the CEC voltage so that CCS becomes 0.06 V with $H1^+ = 1.525$ V and $H2^+ = 1.525$ V, and then measure CCS (CS_L) when $H1^+ = 1.525$ V and $H2^+ = 1.525$ V and CCS (CS_H) when $H1^+ = 1.55$ V and $H2^+ = 1.5$ V.

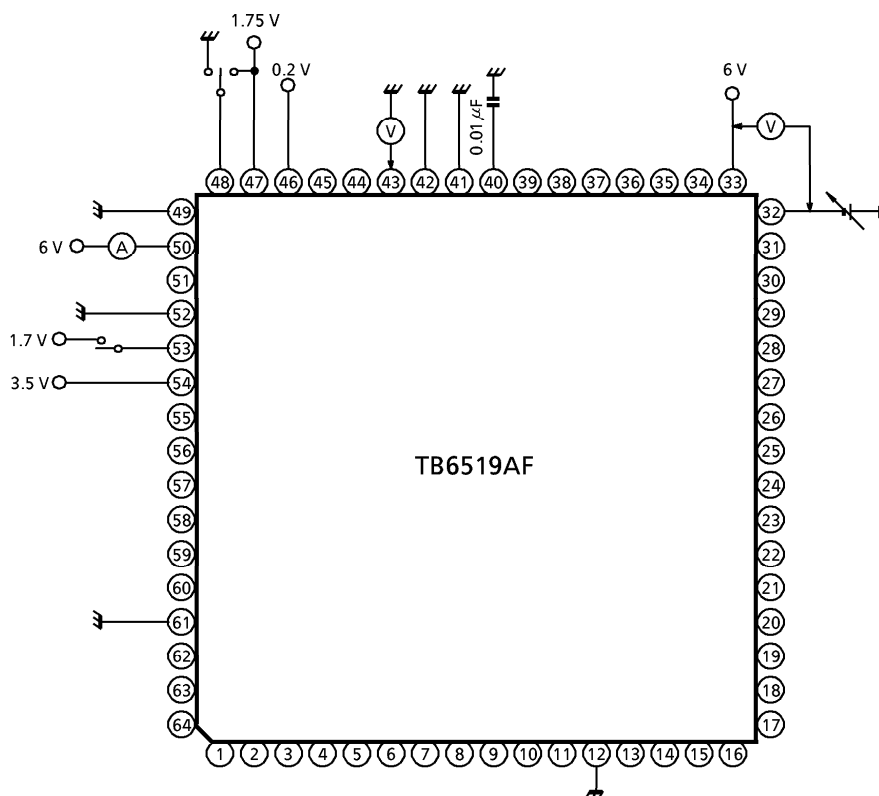
1999-03-17 27/33

No. 51 Cl_U , No. 52 Cl_L

1999-03-17 28/33



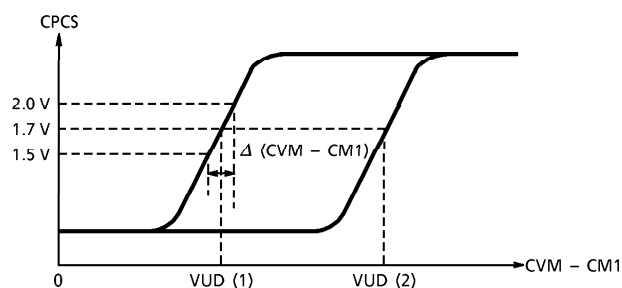
TEST CIRCUIT 20. CG_PCS, VUD (1), VUD (2), Cl_{SWB}



No. 54 CG_PCS, No. 55 VUD (1), No. 56 VUD (2)

Set CEC = 0 V, change CM1 from 6 V to 5 V and measure the potential difference (CVM – CM1) of the CVM terminal and the CM1 terminal when the potential of the CPCS terminal becomes 1.7 V.

Set CEC = CECR = 1.75 V, perform the same measurements as outlined below and acquire the characteristics indicated in the diagram below.

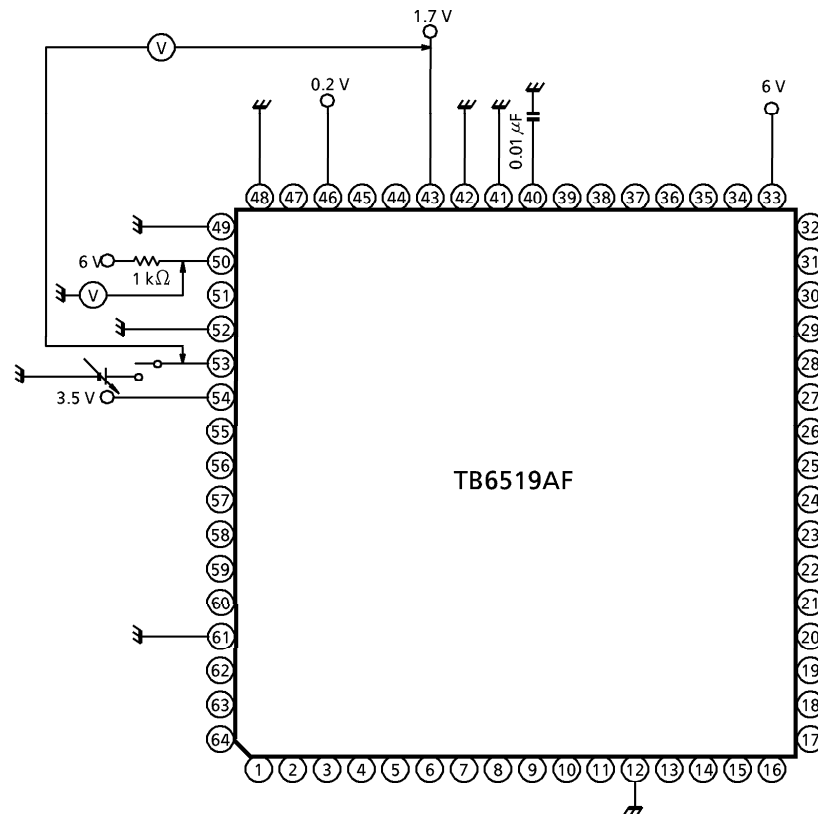


$$CG_{PCS} = \frac{2.0 \text{ V} - 1.5 \text{ V}}{\Delta (CVM - CM1)}$$

No. 57 Cl_{SWB}

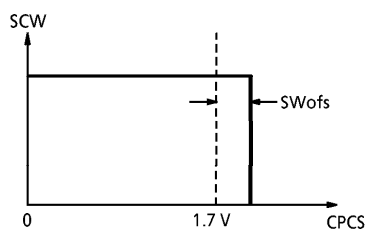
Set FC = 1.7 V, CEC = 0 V and CM1 = 6 V and measure the current that flows into the SCW terminal.

TEST CIRCUIT 21. CSWofs

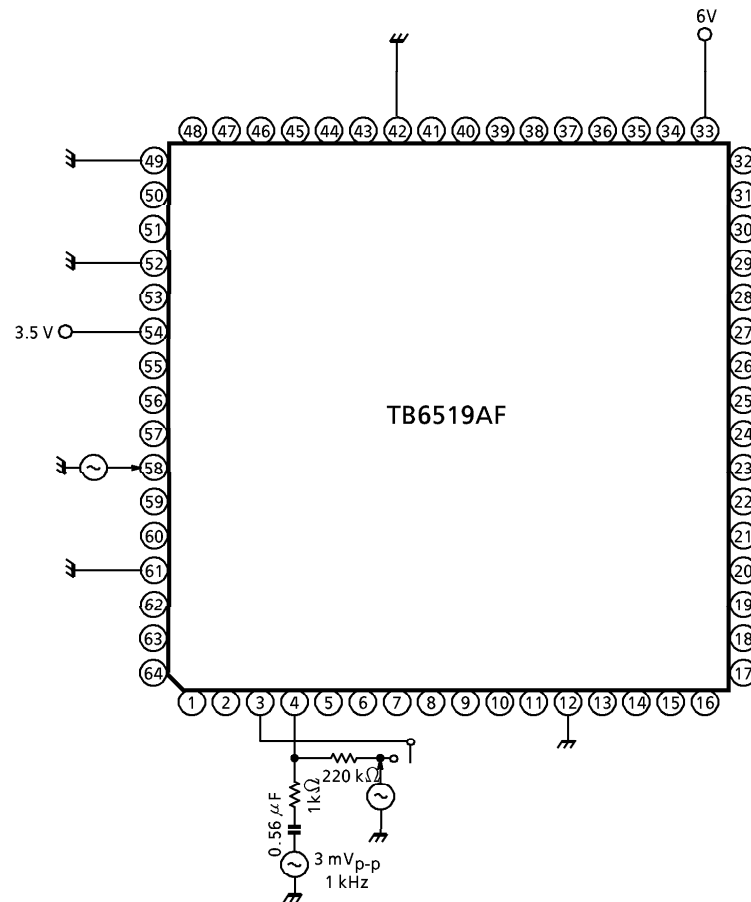


No. 53 CSWofs

Set SPCS = 1.7 V, change FC from 0 V to 3.5 V and measure the potential difference (FC – CPCS) of the FC terminal and the CPCS terminal when SCW changes from high to low.



TEST CIRCUIT 22. CG_{FG} , CG_{FH} , CG_{FL}

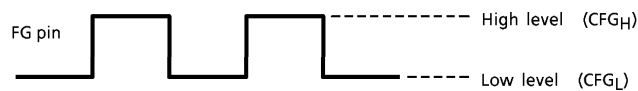


No. 59 CG_{FG} No. 60 CG_{FH} No. 61 CG_{FL}

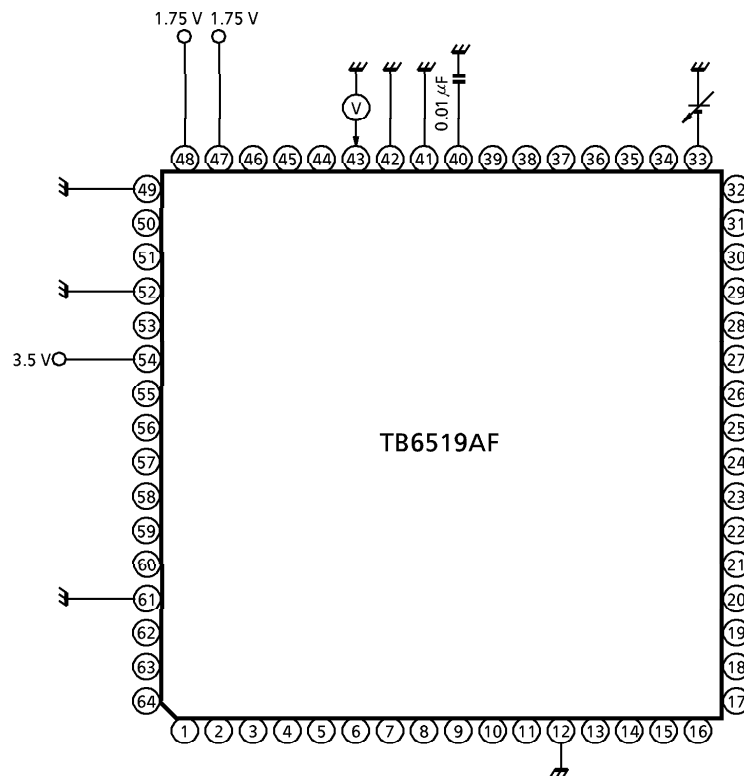
Set $CG_{out} = V_o$ and measure V_o when $V_{in} = 3 \text{ mV}_{p-p}$ at 1 kHz.

Then acquire : $CG_{FG} = 20 \log \frac{V_o}{V_{in}}$

Also, acquire the characteristics indicated in the diagram below and then measure the high level potential and low level potential of the CFG terminal's output wave form.

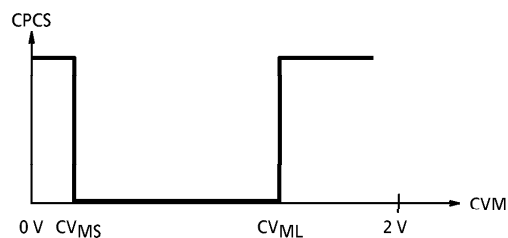


TEST CIRCUIT 23. CV_{ML} , CV_{MS}



No. 62 CV_{ML} No. 63 CV_{MS}

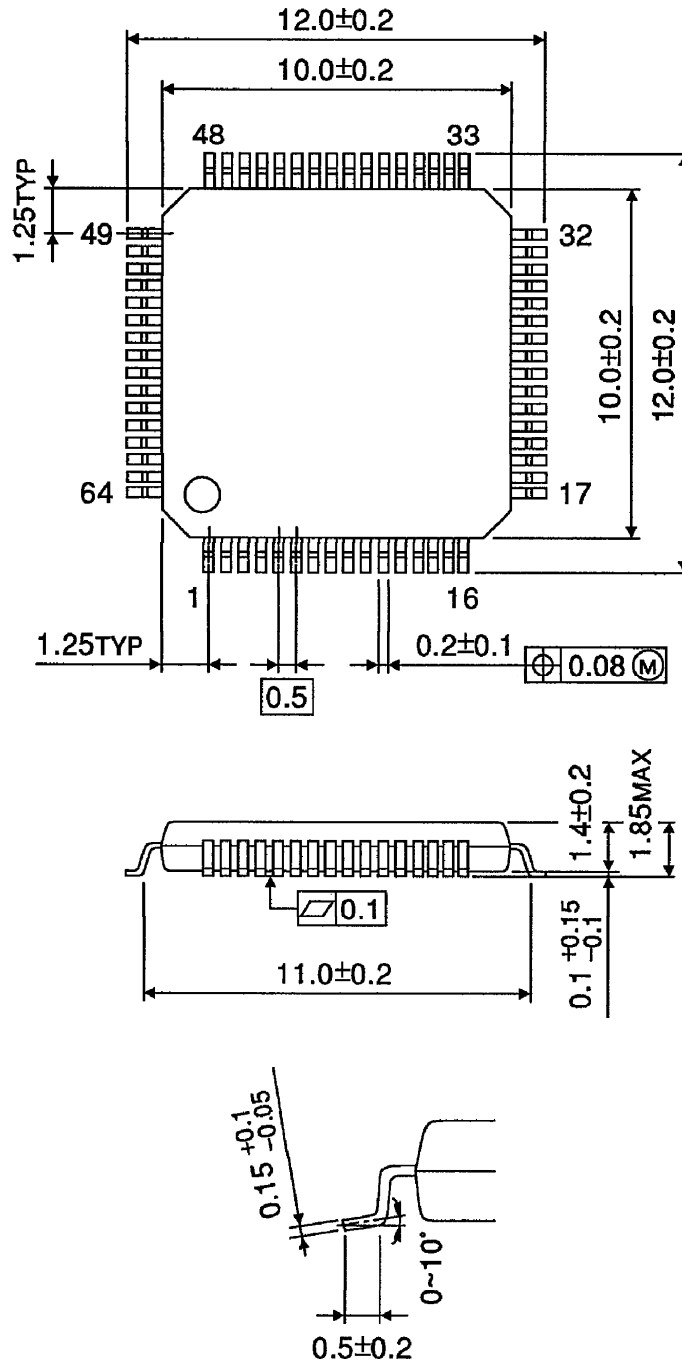
Change CVM from 2 V to 0 V, acquire the characteristics indicated in the following diagram and measure the threshold voltage.



OUTLINE DRAWING

LQFP64-P-1010-0.50A

Unit : mm



Weight : 0.34 g (Typ.)