

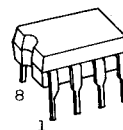
TC40107BP DUAL 2-INPUT NAND BUFFER/DRIVER

TC40107BP is a dual 2-input NAND gate, of which output is of open-drain structure by use of N-channel MOS FET. Being capable of driving a large current, it can be directly connected to a relay, a lamp, a light-emitting diode (LED), etc. Wired OR can be also made.

($I_{OL}=74\text{mA(Typ.)}$ at $V_{DD}=10\text{V}$ and $V_{OL}=0.5\text{V}$)

The package is a compact DIP 8-pin unit, which is easily mounted.

Since its output current is large, if the capacitor of an output line exceeds 500pF, a resistor of 25 Ω or more should be used in series with the capacitor.

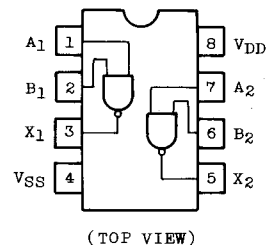


DIP 8 (3D8A-P)

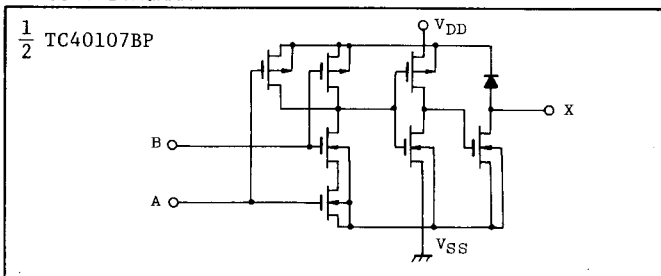
MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	$V_{SS}-0.5 \sim V_{SS}+20$	V
Input Voltage	V_{IN}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
Output Voltage	V_{OUT}	$V_{SS}-0.5 \sim V_{DD}+0.5$	V
DC Input Current	I_{IN}	± 10	mA
Max. GND Current	I_{SS}	125	mA
Power Dissipation	P_d	300	mW
Operating Temperature Range	T_A	$-40 \sim 85$	$^{\circ}\text{C}$
Storage Temperature Range	T_{stg}	$-65 \sim 150$	$^{\circ}\text{C}$
Lead Temp./Time	T_{sol}	$260^{\circ}\text{C} \cdot 10 \text{ sec}$	

PIN ASSIGNMENT



CIRCUIT DIAGRAM



TRUTH TABLE

INPUT		OUTPUT
A	B	X
L	L	HZ
L	H	HZ
H	L	HZ
H	H	L
HZ : High impedance		

RECOMMENDED OPERATING CONDITIONS ($V_{SS}=0\text{V}$)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V_{DD}	3	—	18	V
Input Voltage	V_{IN}	0	—	V_{DD}	V
Load Capacitance	C_L	—	—	500	pF

STATIC ELECTRICAL CHARACTERISTICS ($V_{SS}=0V$)

CHARACTERISTIC		SYM-BOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
					MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
Low-Level Output Voltage		V_{OL}	$ I_{OUT} < 1\mu A$ $V_{IH}=V_{DD}$	5	-	0.05	-	0.00	0.05	-	0.05	V
				10	-	0.05	-	0.00	0.05	-	0.05	
				15	-	0.05	-	0.00	0.05	-	0.05	
Output Low Current		I_{OL}	$V_{OL}=0.4V$	5	20	-	16	32	-	14	-	mA
			$V_{OL}=1.0V$	5	42	-	34	68	-	30	-	
			$V_{OL}=0.5V$	10	46	-	37	74	-	32	-	
			$V_{OL}=1.0V$	10	85	-	68	136	-	60	-	
			$V_{OL}=0.5V$	15	63	-	50	100	-	44	-	
			$V_{IH}=V_{DD}$									
Input High Voltage		V_{IH} *	$V_{OUT}=0.5V, 4.5V$	5	3.5	-	3.5	2.75	-	3.5	-	V
			$V_{OUT}=1.0V, 9.0V$	10	7.0	-	7.0	5.5	-	7.0	-	
			$V_{OUT}=1.5V, 13.5V$	15	11.0	-	11.0	8.25	-	11.0	-	
			$ I_{OUT} < 1\mu A$									
Input Low Voltage		V_{IL} *	$V_{OUT}=4.5V$	5	-	1.5	-	2.25	1.5	-	1.5	V
			$V_{OUT}=9.0V$	10	-	3.0	-	4.5	3.0	-	3.0	
			$V_{OUT}=13.5V$	15	-	4.0	-	6.75	4.0	-	4.0	
			$ I_{OUT} < 1\mu A$									
Input Current	"H" Level	I_{IH}	$V_{IH}=18V$	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
	"L" Level	I_{IL}	$V_{IL}=0V$	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	
3-State Output Leakage Current		I_{DH}	$V_{OH}=18V$	18	-	2	-	10^{-4}	2	-	20	
Quiescent Device Current		I_{DD} **	$V_{IN}=V_{DD}, V_{SS}$ Outputs Open	5	-	1	-	0.001	1	-	7.5	
				10	-	2	-	0.001	2	-	15	
				15	-	4	-	0.002	4	-	30	

* Required external pull-up register R (=20k Ω)

** All valid input combinations.

DYNAMIC ELECTRICAL CHARACTERISTICS ($T_a=25^\circ\text{C}$, $V_{SS}=0\text{V}$, $C_L=50\text{pF}$)

CHARACTERISTIC	SYMBOL	TEST CONDITION	$V_{DD}(\text{V})$	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Low to High)	t_{TLH}	$R_L=120\Omega$	5	-	35	100	ns
			10	-	25	70	
			15	-	20	50	
Output Transition Time (High to Low)	t_{THL}	$R_L=120\Omega$	5	-	35	100	ns
			10	-	10	40	
			15	-	7	20	
Propagation Delay Time (Low to High)	t_{pLH}	$R_L=120\Omega$	5	-	60	200	ns
			10	-	35	120	
			15	-	30	100	
Propagation Delay Time (High to Low)	t_{pHL}	$R_L=120\Omega$	5	-	70	200	ns
			10	-	30	90	
			15	-	20	60	
Input Capacitance	C_{IN}			-	5	7.5	pF
Output Capacitance	C_{OUT}			-	30	-	pF

CIRCUIT AND WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

