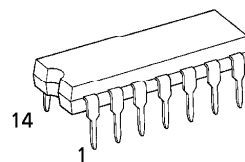


# TC4013BP, TC4013BF, TC4013BFN

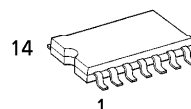
## TC4013B DUAL D-TYPE FLIP-FLOP

TC4013B contains two independent circuits of D type flip-flop. The input level applied to DATA input are transferred to Q and  $\bar{Q}$  output by rising edge of the clock pulse. When SET input is placed at "H", and RESET input is placed at "L", outputs become Q = "H", and  $\bar{Q}$  = "L". When RESET input is placed at "H", and SET input is placed at "L", outputs become Q = "L", and  $\bar{Q}$  = "H". When both of RESET input and SET input are at "H", outputs become Q = "H" and  $\bar{Q}$  = "H".

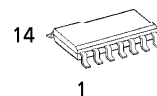
(Note) The JEDEC SOP (FN) is not available in Japan.



P (DIP14-P-300-2.54)  
Weight : 0.96g (Typ.)



F (SOP14-P-300-1.27)  
Weight : 0.18g (Typ.)

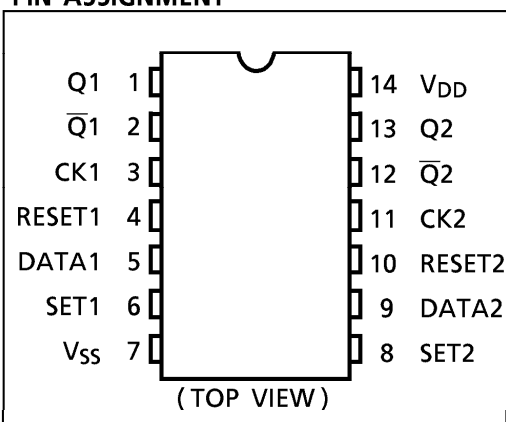


FN (SOL14-P-150-1.27)  
Weight : 0.12g (Typ.)

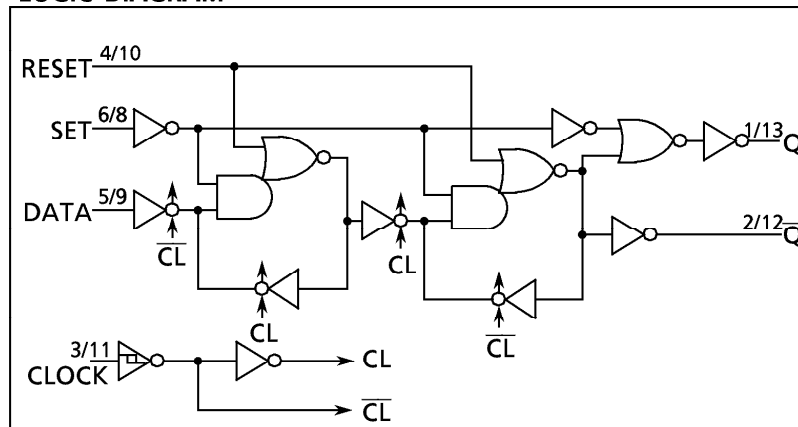
## MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	$V_{DD}$	$V_{SS} - 0.5 \sim V_{SS} + 20$	V
Input Voltage	$V_{IN}$	$V_{SS} - 0.5 \sim V_{DD} + 0.5$	V
Output Voltage	$V_{OUT}$	$V_{SS} - 0.5 \sim V_{DD} + 0.5$	V
DC Input Current	$I_{IN}$	$\pm 10$	mA
Power Dissipation	$P_D$	300 (DIP) / 180 (SOIC)	mW
Operating Temperature Range	$T_{opr}$	$-40 \sim 85$	$^{\circ}\text{C}$
Storage Temperature Range	$T_{stg}$	$-65 \sim 150$	$^{\circ}\text{C}$

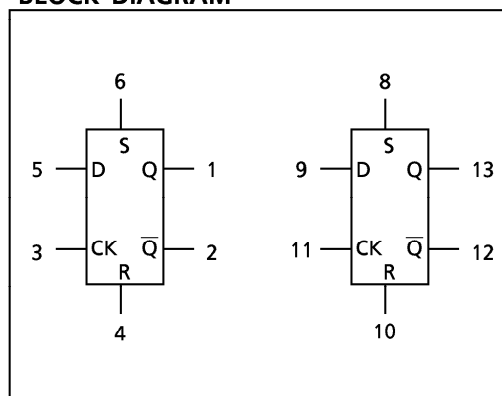
## PIN ASSIGNMENT



## LOGIC DIAGRAM






## BLOCK DIAGRAM



961001EBA2

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TRUTH TABLE

INPUTS				OUTPUTS	
RESET	SET	DATA	CK△	Qn + 1	$\overline{Q}n + 1$
L	H	*	*	H	L
H	L	*	*	L	H
H	H	*	*	H	H
L	L	L		L	H
L	L	H		H	L
L	L	*		$Qn \cdot$	$\overline{Q}n \cdot$

\* : Don't Care

△ : Level Change

· : No Change

961001EBA2'

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● The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.

● The information contained herein is subject to change without notice.

RECOMMENDED OPERATING CONDITIONS ( $V_{SS} = 0V$ )

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
DC Supply Voltage	$V_{DD}$		3	—	18	V
Input Voltage	$V_{IN}$		0	—	$V_{DD}$	V

STATIC ELECTRICAL CHARACTERISTICS ( $V_{SS} = 0V$ )

CHARACTERISTIC	SYM-BOL	TEST CONDITION	$V_{DD}$ (V)	- 40°C		25°C			85°C		UNIT
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Output Voltage	$V_{OH}$	$ I_{OUT}  < 1\mu A$ $V_{IN} = V_{SS}, V_{DD}$	5	4.95	—	4.95	5.00	—	4.95	—	V
			10	9.95	—	9.95	10.00	—	9.95	—	
			15	14.95	—	14.95	15.00	—	14.95	—	
Low-Level Output Voltage	$V_{OL}$	$ I_{OUT}  < 1\mu A$ $V_{IN} = V_{SS}, V_{DD}$	5	—	0.05	—	0.00	0.05	—	0.05	V
			10	—	0.05	—	0.00	0.05	—	0.05	
			15	—	0.05	—	0.00	0.05	—	0.05	
Output High Current	$I_{OH}$	$V_{OH} = 4.6V$	5	-0.61	—	-0.51	-1.0	—	-0.42	—	mA
		$V_{OH} = 2.5V$	5	-2.50	—	-2.10	-4.0	—	-1.70	—	
		$V_{OH} = 9.5V$	10	-1.50	—	-1.30	-2.2	—	-1.10	—	
		$V_{OH} = 13.5V$	15	-4.00	—	-3.40	-9.0	—	-2.80	—	
		$V_{IN} = V_{SS}, V_{DD}$									
Output Low Current	$I_{OL}$	$V_{OL} = 0.4V$	5	0.61	—	0.51	1.2	—	0.42	—	mA
		$V_{OL} = 0.5V$	10	1.50	—	1.30	3.2	—	1.10	—	
		$V_{OL} = 1.5V$	15	4.00	—	3.40	12.0	—	2.80	—	
		$V_{IN} = V_{SS}, V_{DD}$									
Input High Voltage	$V_{IH}$	$V_{OUT} = 0.5V, 4.5V$	5	3.5	—	3.5	2.75	—	3.50	—	V
		$V_{OUT} = 1.0V, 9.0V$	10	7.0	—	7.0	5.50	—	7.00	—	
		$V_{OUT} = 1.5V, 13.5V$	15	11.0	—	11.0	8.25	—	11.00	—	
		$ I_{OUT}  < 1\mu A$									
Input Low Voltage	$V_{IL}$	$V_{OUT} = 0.5V, 4.5V$	5	—	1.5	—	2.25	1.5	—	1.5	V
		$V_{OUT} = 1.0V, 9.0V$	10	—	3.0	—	4.50	3.0	—	3.0	
		$V_{OUT} = 1.5V, 13.5V$	15	—	4.0	—	6.75	4.0	—	4.0	
		$ I_{OUT}  < 1\mu A$									
Input Current	"H" Level	$I_{IH}$	$V_{IH} = 18V$	18	—	0.1	—	$10^{-5}$	0.1	—	μA
	"L" Level	$I_{IL}$	$V_{IL} = 0V$	18	—	-0.1	—	$-10^{-5}$	-0.1	—	
Quiescent Supply Current	$I_{DD}$	$V_{IN} = V_{SS}, V_{DD} *$	5	—	1	—	0.002	1	—	30	μA
			10	—	2	—	0.004	2	—	60	
			15	—	4	—	0.008	4	—	120	

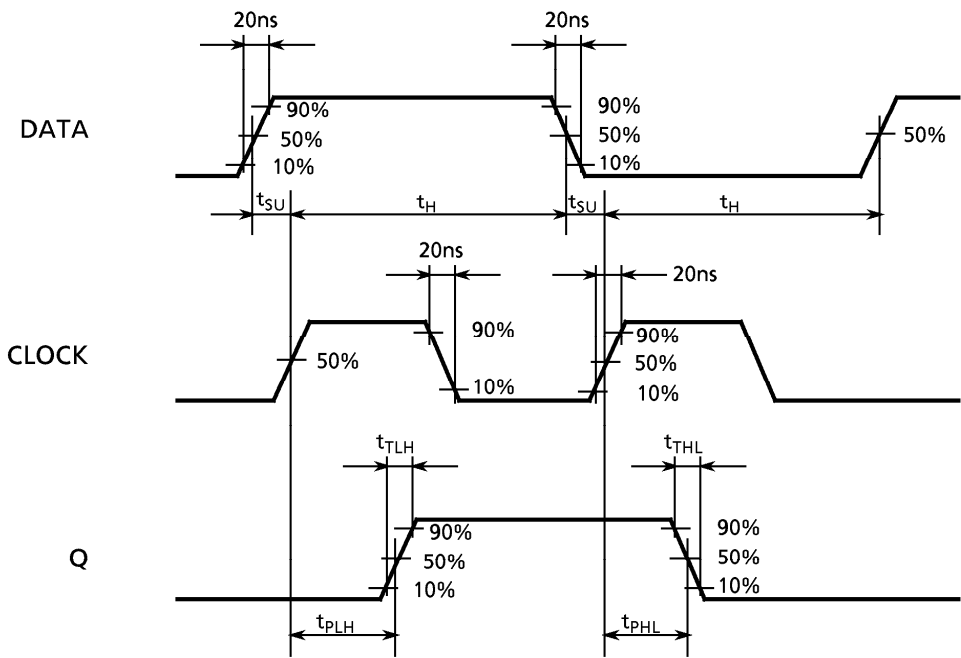
\* All valid input combinations.

## DYNAMIC ELECTRICAL CHARACTERISTICS (Ta = 25°C, Vss = 0V, CL = 50pF)

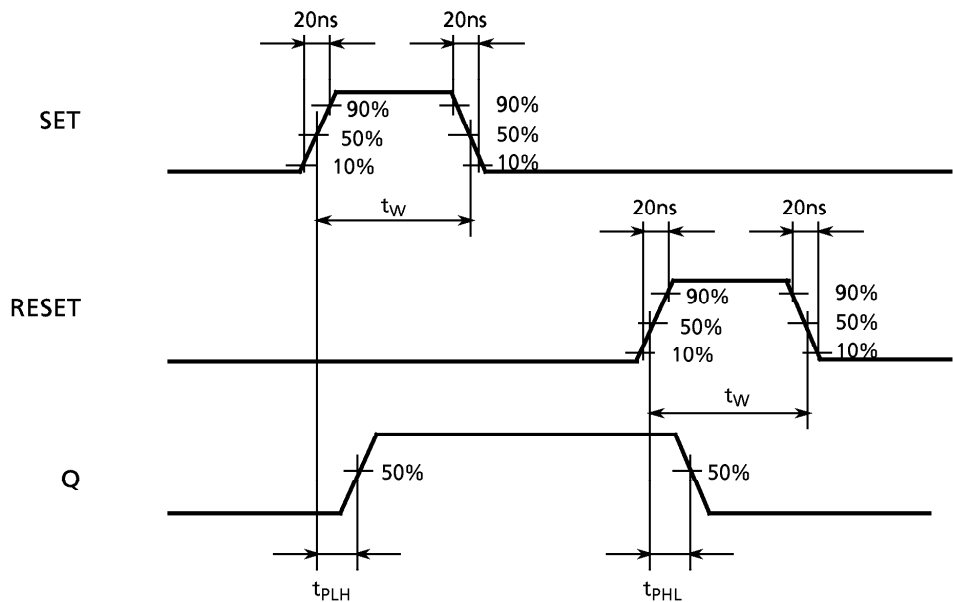
CHARACTERISTIC	SYMBOL	TEST CONDITION	V <sub>DD</sub> (V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Low to High)	t <sub>TLH</sub>		5 10 15	— — —	70 35 30	200 100 80	ns
Output Transition Time (High to Low)	t <sub>THL</sub>		5 10 15	— — —	70 35 30	200 100 80	
Propagation Delay Time (CK - Q, $\overline{Q}$ )	t <sub>pLH</sub> t <sub>pHL</sub>		5 10 15	— — —	130 65 50	300 130 90	
Propagation Delay Time (SET, RESET - Q, $\overline{Q}$ )	t <sub>pLH</sub>		5 10 15	— — —	110 50 40	300 130 90	
Propagation Delay Time (SET, RESET - Q, $\overline{Q}$ )	t <sub>pHL</sub>		5 10 15	— — —	110 50 40	300 130 90	
Max. Clock Frequency	f <sub>CL</sub>		5 10 15	3.5 8.0 12.0	8 16 20	— — —	MHz
Max. Clock Input Rise Time Max. Clock Input Fall Time	t <sub>rCL</sub> t <sub>fCL</sub>		5 10 15	No Limit			μs
Min. Pulse Width (SET, RESET)	t <sub>w</sub>		5 10 15	— — —	60 30 25	180 80 50	ns
Min. Clock Pulse Width	t <sub>w</sub>		5 10 15	— — —	60 30 25	140 60 40	
Min. Set-up Time (DATA - CK)	t <sub>su</sub>		5 10 15	— — —	— — —	40 20 15	
Min. Hold Time (DATA - CK)	t <sub>H</sub>		5 10 15	— — —	20 10 6	40 20 15	ns
Min. Removal Time (SET, RESET - CK)	t <sub>rem</sub>		5 10 15	— — —	— — —	40 20 15	
Input Capacitance	C <sub>IN</sub>			—	5	7.5	pF

WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

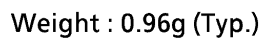
WAVEFORM 1



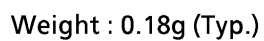
WAVEFORM 2



## Unit in mm



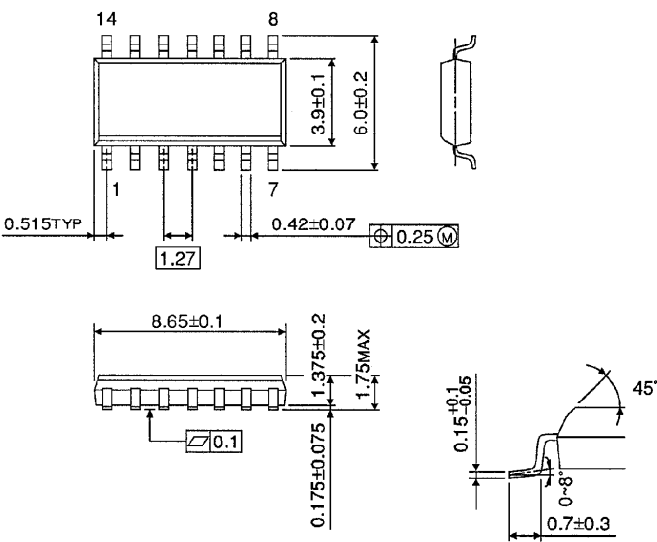
## Unit in mm



SOP 14PIN (150mil BODY) OUTLINE DRAWING (SOL14-P-150-1.27)

Unit in mm

(Note) This package is not available in Japan.



Weight : 0.12g (Typ.)