

SYNCHRONOUS PROGRAMMABLE 4-BIT COUNTER

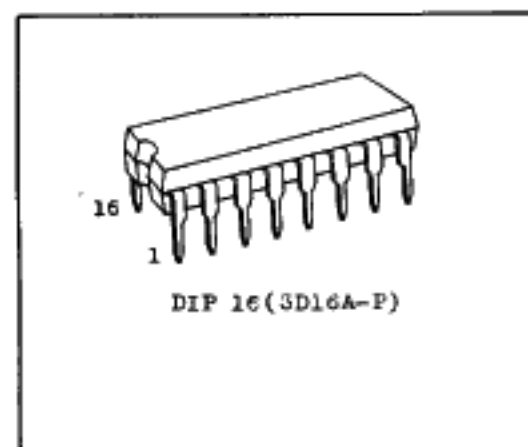
TC40160BP DECADE WITH ASYNCHRONOUS CLEAR

TC40161BP BINARY WITH ASYNCHRONOUS CLEAR

TC40162BP DECADE WITH SYNCHRONOUS CLEAR

TC40163BP BINARY WITH SYNCHRONOUS CLEAR

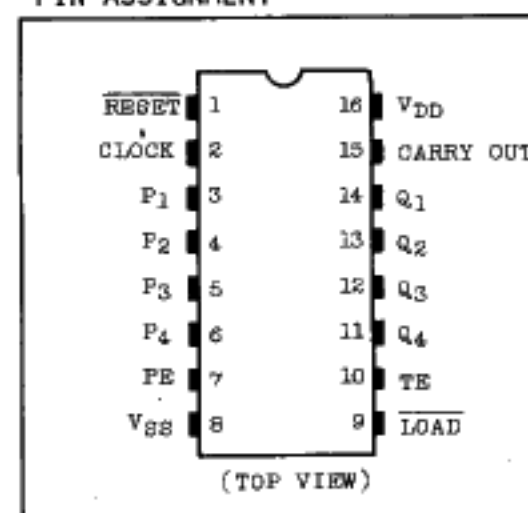
The TC40160BP, TC40161BP, TC40162BP, and TC40163BP are synchronously programmable 4-bit counters. The TC40160BP and TC40161BP are decimal counter and 4-bit binary counter respectively having asynchronous clear function which directly clears all the flip-flop outputs. The TC40162BP and TC40163BP are decimal counter and 4-bit binary counter respectively which are synchronous at the rising edges of clocks. CLEAR and LOAD of these counters are active at the "L" level. Further, these counters are functionally compatible with the 74160, 74161, 74162, and 74163 of TTL.



MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V _{DD}	V _{SS} -0.5 ~ V _{SS} +20	V
Input Voltage	V _{IN}	V _{SS} -0.5 ~ V _{DD} +0.5	V
Output Voltage	V _{OUT}	V _{SS} -0.5 ~ V _{DD} +0.5	V
DC Input Current	I _{IN}	±10	mA
Power Dissipation	P _D	300	mW
Operating Temperature Range	T _A	-40 ~ 85	°C
Storage Temperature Range	T _{stg}	-65 ~ 150	°C
Lead Temp./Time	T _{sol}	260°C · 10 sec	

PIN ASSIGNMENT



TRUTH TABLE

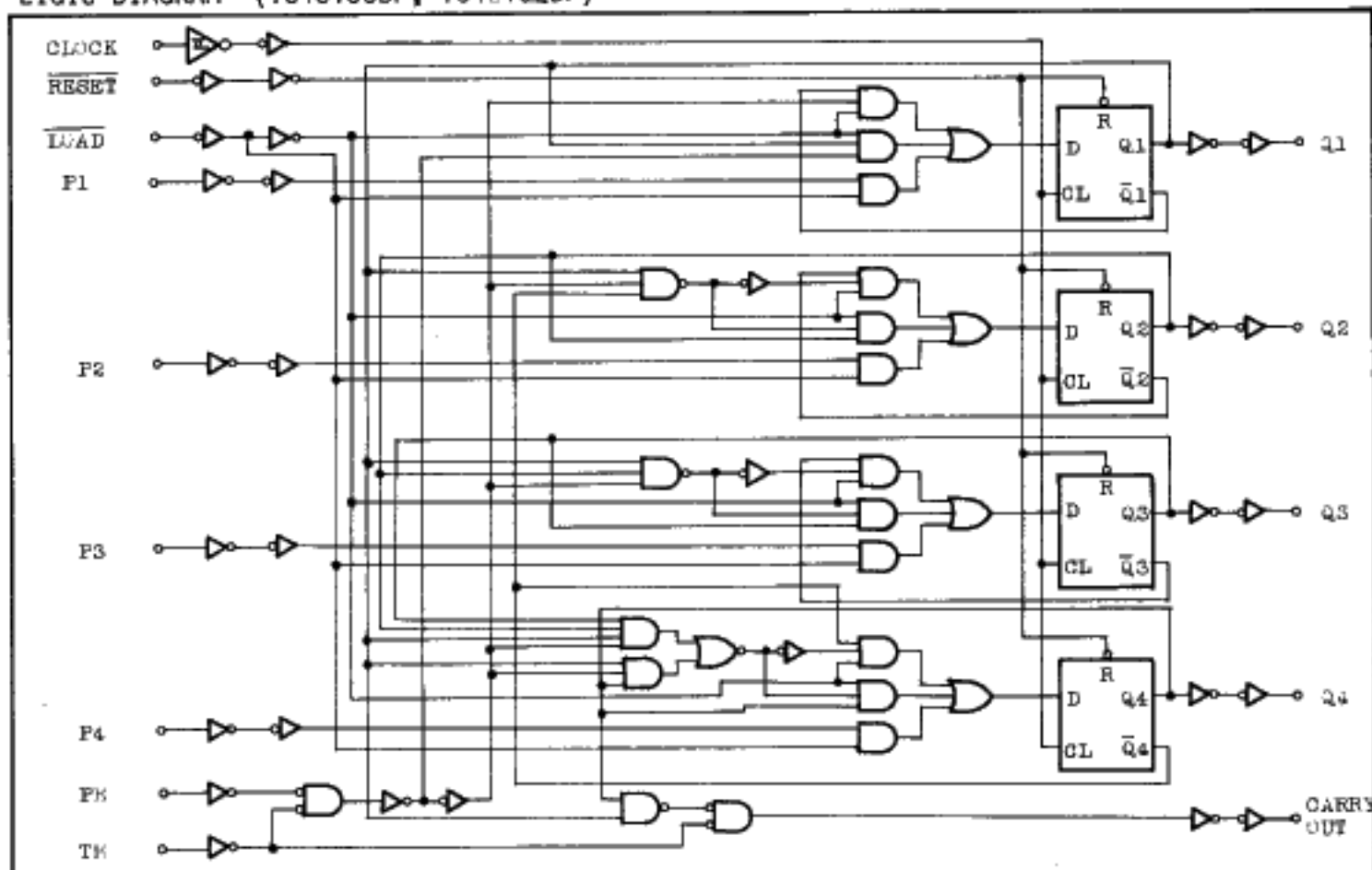
INPUT									OUTPUT			
CLOCK	RESET	LOAD	PE	TE	P ₁	P ₂	P ₃	P ₄	Q ₁	Q ₂	Q ₃	Q ₄
☆	L	*	*	*	*	*	*	*	L	L	L	L
△ ↓	H	L	*	*	D ₁	D ₂	D ₃	D ₄	D ₁	D ₂	D ₃	D ₄
△ ↓	H	H	L	L	*	*	*	*
△ ↓	H	H	L	H	*	*	*	*
△ ↓	H	H	H	L	*	*	*	*
△ ↓	H	H	H	H	*	*	*	*	COUNT			
△ ↓	H	*	*	*	*	*	*	*

* : Don't care
 △ : Level change
 . : No change
 D : Data "H" or "L"

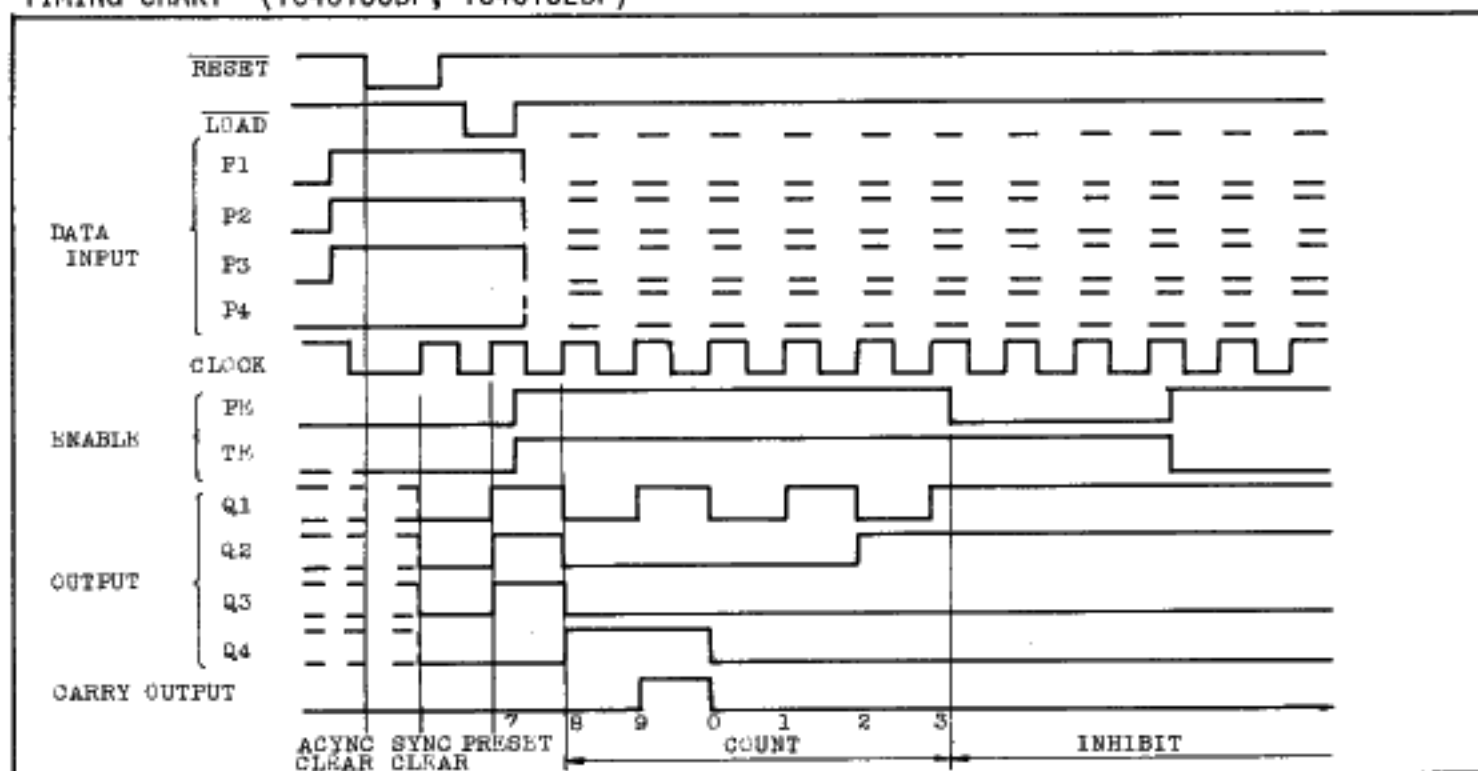
☆ :
 Don't care (TC40160, TC40161)
 Rise edge (TC40162, TC40163)

TC40160BP, TC40161BP, TC40162BP, TC40163BP

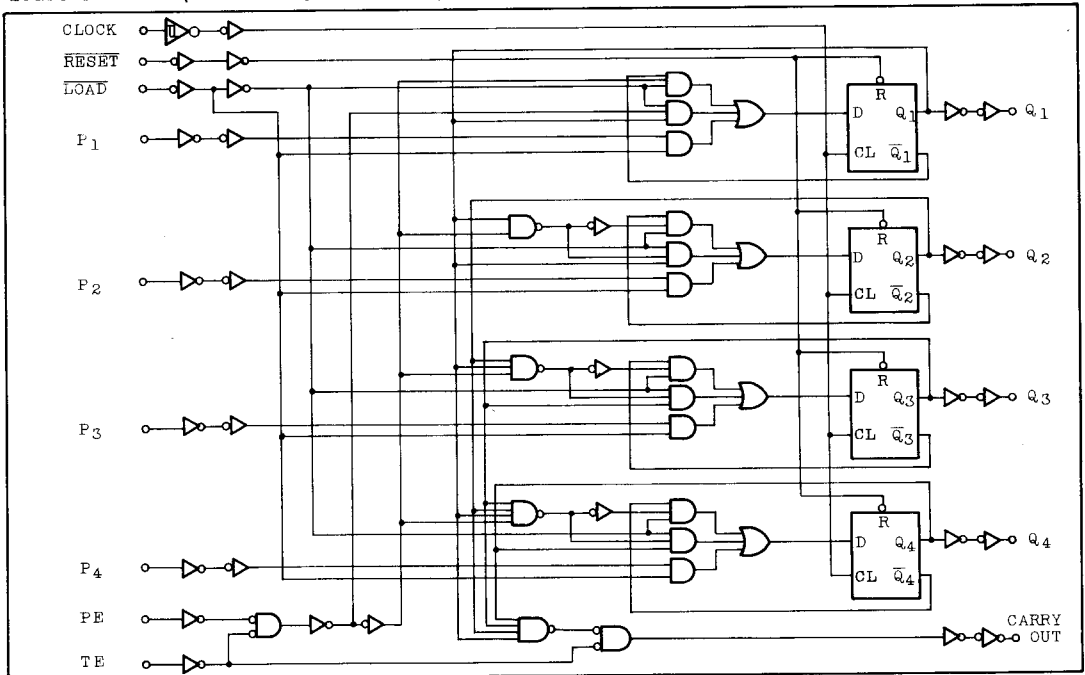
LIGIC DIAGRAM (TC40160BP, TC40162BP)



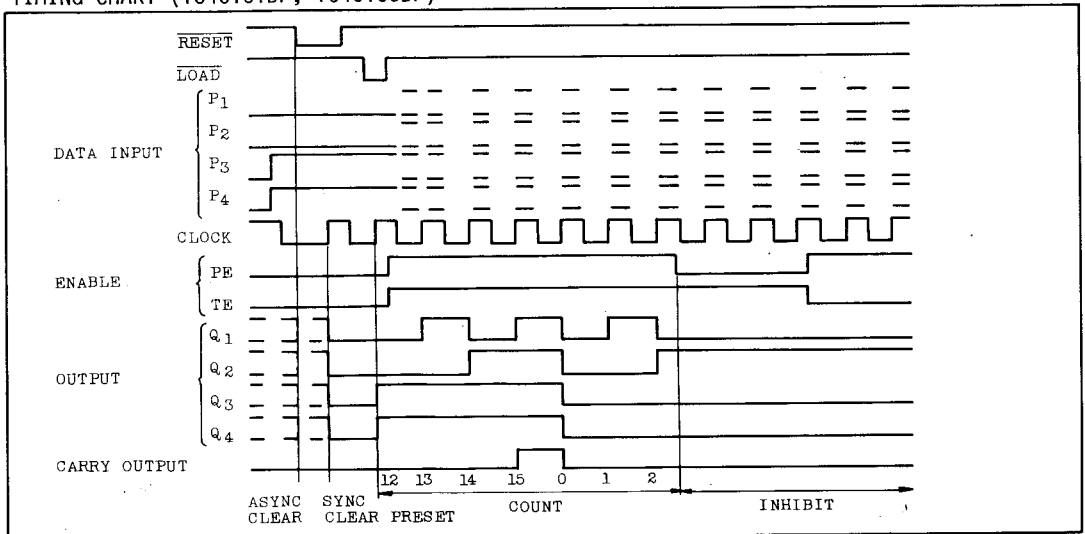
TIMING CHART (TC40160BP, TC40162BP)



LOGIC DIAGRAM (TC40161BP, TC40163BP)



TIMING CHART (TC40161BP, TC40163BP)



TC40160BP, TC40161BP, TC40162BP, TC40163BP

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V _{DD}		3	-	18	V
Input Voltage	V _{IN}		0	-	V _{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYM-BOL	TEST CONDITION	V _{DD} (V)	-40°C		25°C			85°C		UNIT
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Output Voltage	V _{OH}	I _{OUT} < 1μA V _{IN} =V _{SS} , V _{DD}	5	4.95	-	4.95	5.00	-	4.95	-	V
			10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage	V _{OL}	I _{OUT} < 1μA V _{IN} =V _{SS} , V _{DD}	5	-	0.05	-	0.00	0.05	-	0.05	V
			10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current	I _{OH}	V _{OH} =4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
		V _{OH} =2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
		V _{OH} =9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
		V _{OH} =13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
		V _{IN} =V _{SS} , V _{DD}									
Output Low Current	I _{OL}	V _{OL} =0.4V	5	0.61	-	0.51	1.5	-	0.42	-	mA
		V _{OL} =0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
		V _{OL} =1.5V	15	4.0	-	3.4	15.0	-	2.8	-	
		V _{IN} =V _{SS} , V _{DD}									
Input High Voltage	V _{IH}	V _{OUT} =0.5V, 4.5V	5	3.5	-	3.5	2.75	+	3.5	-	V
		V _{OUT} =1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
		V _{OUT} =1.5V, 13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
		I _{OUT} < 1μA									
Input Low Voltage	V _{IL}	V _{OUT} =0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	V
		V _{OUT} =1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
		V _{OUT} =1.5V, 13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
		I _{OUT} < 1μA									
Input Current	"H" Level	I _{IH} V _{IH} =18V	18	-	0.1	-	10 ⁻⁵	0.1	-	1.0	μA
	"L" Level	I _{IL} V _{IL} =0V	18	-	-0.1	-	-10 ⁻⁵	-0.1	-	-1.0	

STATIC ELECTRICAL CHARACTERISTICS ($V_{SS}=0V$)

CHARACTERISTIC	SYM-BOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{DD}	$V_{IN}=V_{SS}, V_{DD}$ *	5	-	5	-	0.005	5	-	150	μA
			10	-	10	-	0.010	10	-	300	
			15	-	20	-	0.015	20	-	600	

* All Valid input combinations.

DYNAMIC ELECTRICAL CHARACTERISTICS ($T_a=25^\circ C$, $V_{SS}=0V$, $C_L=50pF$)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Low to High)	t_{TLH}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
Output Transition Time (High to Low)	t_{THL}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
Propagation Delay Time (CLOCK - Q)	t_{pLH} t_{pHL}		5	-	250	500	ns
			10	-	100	200	
			15	-	70	140	
Propagation Delay Time (CLOCK-CARRY OUT)	t_{pLH} t_{pHL}		5	-	300	600	
			10	-	120	240	
			15	-	80	160	
Propagation Delay Time (TE-CARRY OUT)	t_{pLH} t_{pHL}		5	-	170	340	
			10	-	65	130	
			15	-	45	90	
Propagation Delay Time (\overline{RESET} - Q) 40160, 40161 Only	t_{pHL}		5	-	180	500	
			10	-	75	220	
			15	-	55	160	
Min. Clock Pulse Width	t_w		5	-	130	250	ns
			10	-	45	90	
			15	-	30	60	
Min. Pulse Width (\overline{RESET}) 40160, 40161 Only	t_{WL}		5	-	140	280	
			10	-	55	110	
			15	-	35	70	

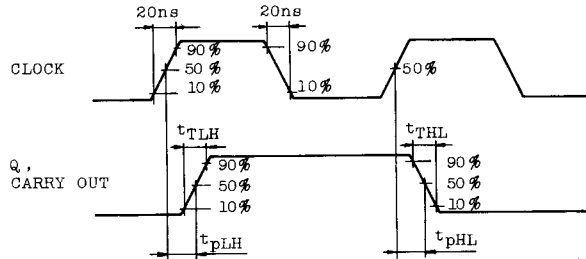
TC40160BP, TC40161BP, TC40162BP, TC40163BP

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, VSS=0V, CL=50pF)

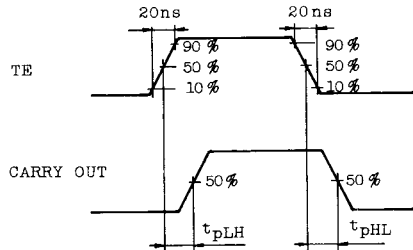
CHARACTERISTIC	SYMBOL	TEST CONDITION	VDD(V)	MIN.	TYP.	MAX.	UNIT
Max. Clock Frequency	fCL		5	2	4	-	MHz
			10	5.5	11	-	
			15	8	16	-	
Max. Clock Input Rise Time.	trCL		5	No Limit			μs
Max. Clock Input Fall Time.	tfCL		10				
			15				
Min. Set-up Time (Pn - CLOCK)	tSU		5	-	55	240	ns
			10	-	20	90	
			15	-	15	60	
Min. Set-up Time (LOAD - CLOCK)	tSU		5	-	75	240	
			10	-	30	90	
			15	-	20	60	
Min. Set-up Time (PE, TE - CLOCK)	tSU		5	-	190	380	
			10	-	70	140	
			15	-	50	100	
Min. Set-up Time (RESET - CLOCK) 40162, 40163 Only	tSU		5	-	50	310	
			10	-	20	110	
			15	-	15	70	
Min. Hold Time (Pn, LOAD, PE, TE- CLOCK)	tH		5	-	-	0	ns
			10	-	-	0	
			15	-	-	5	
Min. Hold Time (RESET - CLOCK) 40162, 40163 Only	tH		5	-	-30	0	
			10	-	-10	0	
			15	-	-5	0	
Min. Removal Time (RESET - COLCK) 40160, 40161 Only	trem		5	-	80	200	ns
			10	-	25	100	
			15	-	15	70	
Input Capacitance	CIN			-	5	7.5	pF

WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

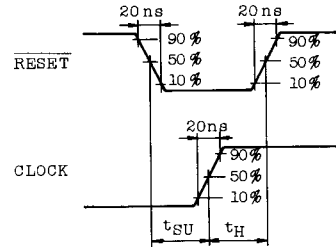
WAVEFORM 1



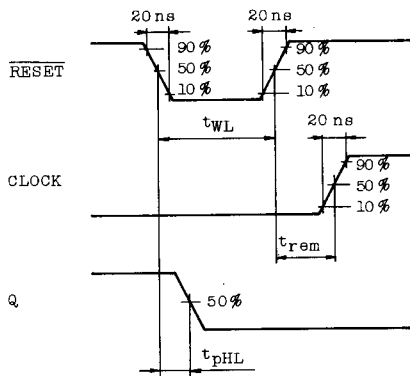
WAVEFORM 2



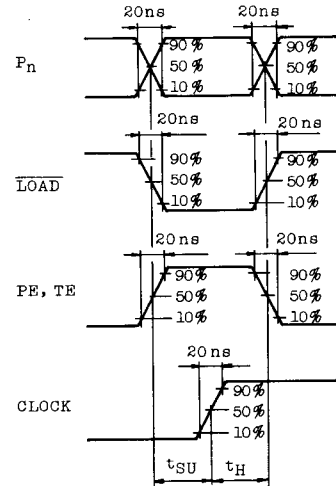
WAVEFORM 3 (40162, 40163)



WAVEFORM 4 (40160, 40161)



WAVEFORM 5



APPLICATION CIRCUIT

1. Cascaded counter packages in the parallel-clocked mode.

