

## HEX D-TYPE FLIP FLOP WITH CLEAR

The TC74ACT174 is an advanced high speed CMOS HEX D-TYPE FLIP FLOP fabricated with silicon gate and double-layer metal wiring C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

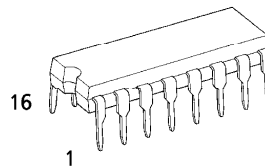
Information signals applied to D inputs are transferred to the Q outputs on the positive going edge of the clock pulse.

When the  $\overline{\text{CLR}}$  input is held low, the Q output are in the low logic level independent of the other inputs.

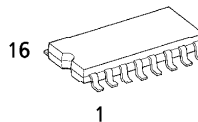
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

## FEATURES :

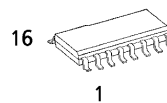
- High Speed..... $f_{\text{MAX}} = 155\text{MHz}(\text{typ.})$   
at  $V_{\text{CC}} = 5\text{V}$
- Low Power Dissipation..... $I_{\text{CC}} = 8\mu\text{A}(\text{Max.})$  at  $T_a = 25^\circ\text{C}$
- Compatible with TTL outputs.... $V_{\text{IL}} = 0.8\text{V}(\text{Max.})$   
 $V_{\text{IH}} = 2.0\text{V}(\text{Min.})$
- Symmetrical Output Impedance.... $|I_{\text{OH}}| = |I_{\text{OL}}| = 24\text{mA}(\text{Min.})$   
Capability of driving  $50\Omega$   
transmission lines.
- Balanced Propagation Delays..... $t_{\text{pLH}} \approx t_{\text{pHL}}$
- Pin and Function Compatible with 74F174



P ( DIP16—P— 300A )  
Weight : 1.00g (TYP.)

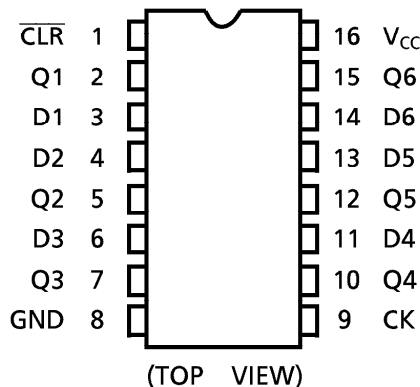


F (SOP16—P—300)  
Weight : 0.18g (TYP.)






FN ( SOL16—P— 150 )  
Weight : 0.13g (TYP.)

## PIN ASSIGNMENT

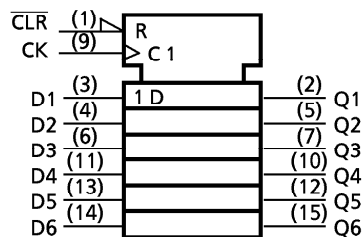


### TRUTH TABLE

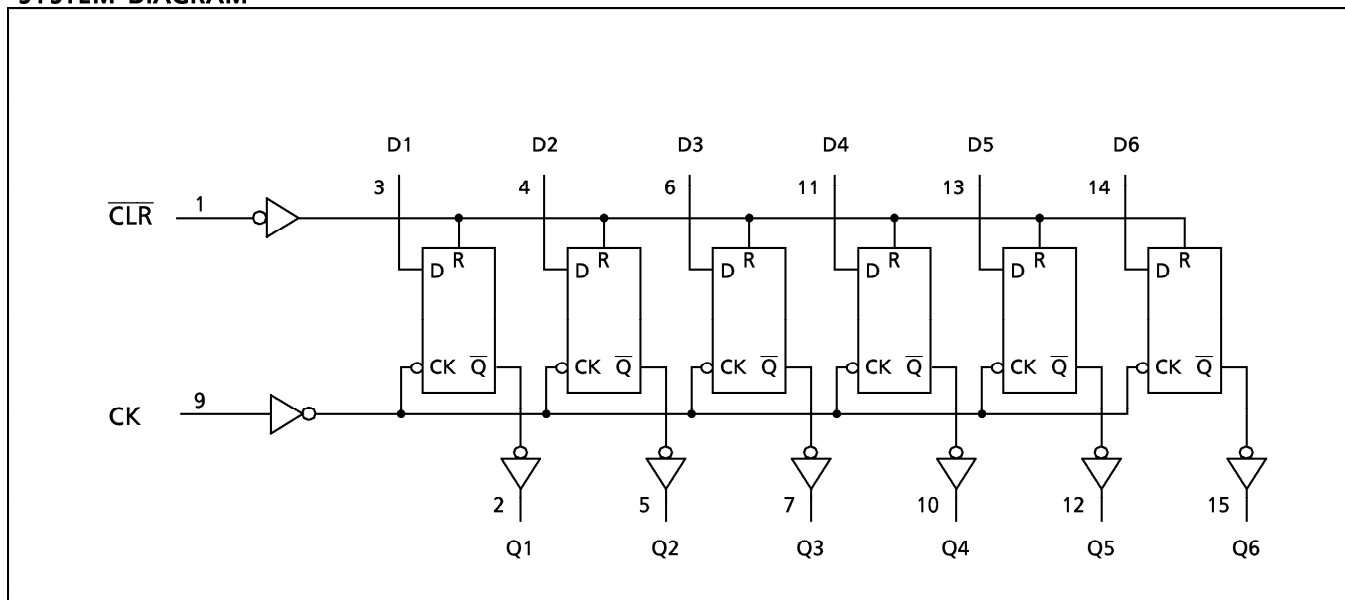
INPUTS			OUTPUTS	FUNCTION
$\overline{\text{CLR}}$	D	CK	Q	
L	X	X	L	CLEAR
H	L		L	—
H	H		H	—
H	X		$Q_n$	NO CHANGE

X : Don't Care

### IEC LOGIC SYMBOL



**SYSTEM DIAGRAM**



**ABSOLUTE MAXIMUM RATINGS**

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	$V_{CC}$	$-0.5 \sim 7.0$	V
DC Input Voltage	$V_{IN}$	$-0.5 \sim V_{CC} + 0.5$	V
DC Output Voltage	$V_{OUT}$	$-0.5 \sim V_{CC} + 0.5$	V
Input Diode Current	$I_{IK}$	$\pm 20$	mA
Output Diode Current	$I_{OK}$	$\pm 50$	mA
DC Output Current	$I_{OUT}$	$\pm 50$	mA
DC $V_{CC}$ /Ground Current	$I_{CC}$	$\pm 150$	mA
Power Dissipation	$P_D$	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	$T_{stg}$	$-65 \sim 150$	$^{\circ}\text{C}$

\*500mW in the range of  $T_a = -40^{\circ}\text{C} \sim 65^{\circ}\text{C}$ . From  $T_a = 65^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  a derating factor of  $-10\text{mW}/^{\circ}\text{C}$  should be applied up to 300mW.

**RECOMMENDED OPERATING CONDITIONS**

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	$V_{CC}$	4.5~5.5	V
Input Voltage	$V_{IN}$	$0 \sim V_{CC}$	V
Output Voltage	$V_{OUT}$	$0 \sim V_{CC}$	V
Operating Temperature	$T_{opr}$	$-40 \sim 85$	$^{\circ}\text{C}$
Input Rise and Fall Time	$dt/dV$	0~10	ns/V

**DC ELECTRICAL CHARACTERISTICS**

PARAMETER	SYMBOL	TEST CONDITION		V <sub>CC</sub> (V)	Ta = 25°C			Ta = -40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V <sub>IH</sub>			4.5 5.5	2.0	—	—	2.0	—	V
Low - Level Input Voltage	V <sub>IL</sub>			4.5 5.5	—	—	0.8	—	0.8	V
High - Level Output Voltage	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -50μA	4.5	4.4	4.5	—	4.4	—	V
			I <sub>OH</sub> = -24mA	4.5	3.94	—	—	3.80	—	
			I <sub>OH</sub> = -75mA*	5.5	—	—	—	3.85	—	
Low - Level Output Voltage	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 50μA	4.5	—	0.0	0.1	—	0.1	V
			I <sub>OL</sub> = 24mA	4.5	—	—	0.36	—	0.44	
			I <sub>OL</sub> = 75mA*	5.5	—	—	—	—	1.65	
Input Leakage Current	I <sub>IN</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		5.5	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		5.5	—	—	8.0	—	80.0	
	I <sub>C</sub>	PER INPUT : V <sub>IN</sub> = 3.4V OTHER INPUT : V <sub>CC</sub> or GND		5.5	—	—	1.35	—	1.5	mA

\* : This spec indicates the capability of driving 50Ω transmission lines.  
One output should be tested at a time for a 10ms maximum duration.

**TIMING REQUIREMENTS ( Input t<sub>r</sub> = t<sub>f</sub> = 3ns )**

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C	Ta = -40~85°C	UNIT
				V <sub>CC</sub> (V)	LIMIT	
Minimum Pulse Width ( CK )	t <sub>W(L)</sub> t <sub>W(H)</sub>			5.0 ± 0.5	5.0	ns
Minimum Pulse Width ( $\overline{\text{CLR}}$ )	t <sub>W(L)</sub>			5.0 ± 0.5	5.0	
Minimum Set - up Time	t <sub>s</sub>			5.0 ± 0.5	3.5	
Minimum Hold Time	t <sub>h</sub>			5.0 ± 0.5	2.0	
Minimum Removal Time ( CLR )	t <sub>rem</sub>			5.0 ± 0.5	3.0	

**AC ELECTRICAL CHARACTERISTICS (  $C_L = 50\text{pF}$ ,  $R_L = 500\ \Omega$ , Input  $t_r = t_f = 3\text{ns}$  )**

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			Ta = -40~85°C		UNIT
			V <sub>CC</sub> (V)	MIN.	TYP.	MAX.	MIN.	MAX.
Propagation Delay Time (CK—Q)	t <sub>pLH</sub> t <sub>pHL</sub>		5.0 ± 0.5	—	7.1	10.1	1.0	11.5
Propagation Delay Time ( $\overline{\text{CLR}}$ —Q)	t <sub>pHL</sub>		5.0 ± 0.5	—	7.4	11.8	1.0	13.5
Maximum Clock Frequency	f <sub>MAX</sub>		5.0 ± 0.5	85	140	—	85	—
Input Capacitance	C <sub>IN</sub>			—	5	10	—	10
Power Dissipation Capacitance	C <sub>PD</sub> (1)			—	32	—	—	—

Note(1) C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

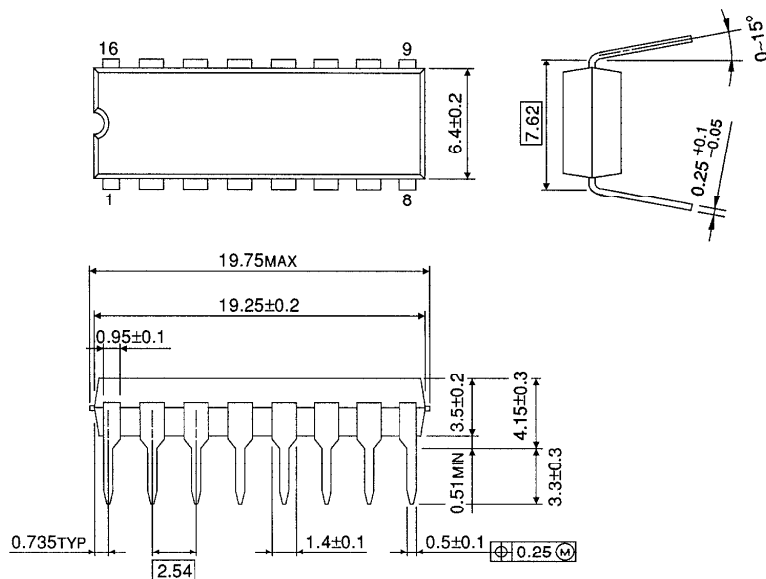
$$I_{CC(\text{opr})} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 6 \text{ (per F/F)}$$

And the total C<sub>PD</sub> when n pcs of Flip Flop operate can be gained by the following equation.

$$C_{PD} \text{ (total)} = 20 + 12 \cdot n$$

**DIP 16PIN OUTLINE DRAWING ( DIP16—P—300A )**

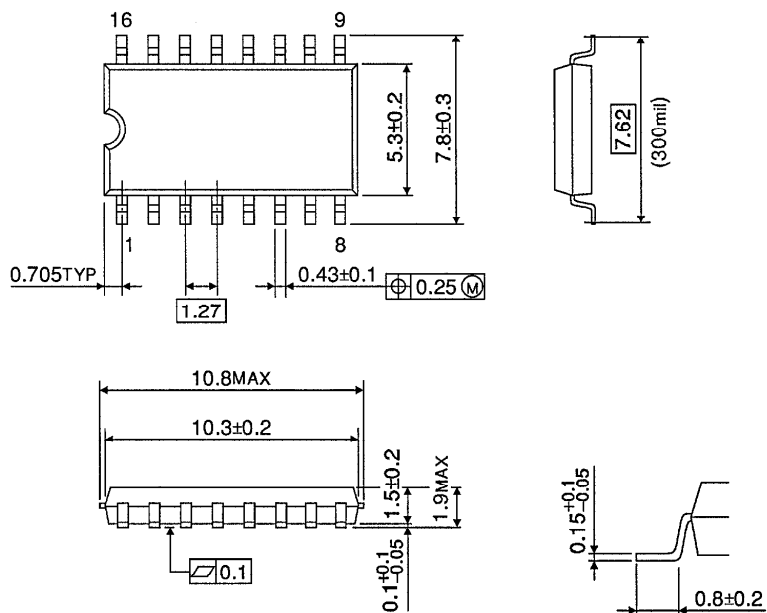
Unit in mm



Weight : 1.00g (TYP.)

**SOP 16PIN ( 200mil BODY ) OUTLINE DRAWING ( SOP16—P—300 )**

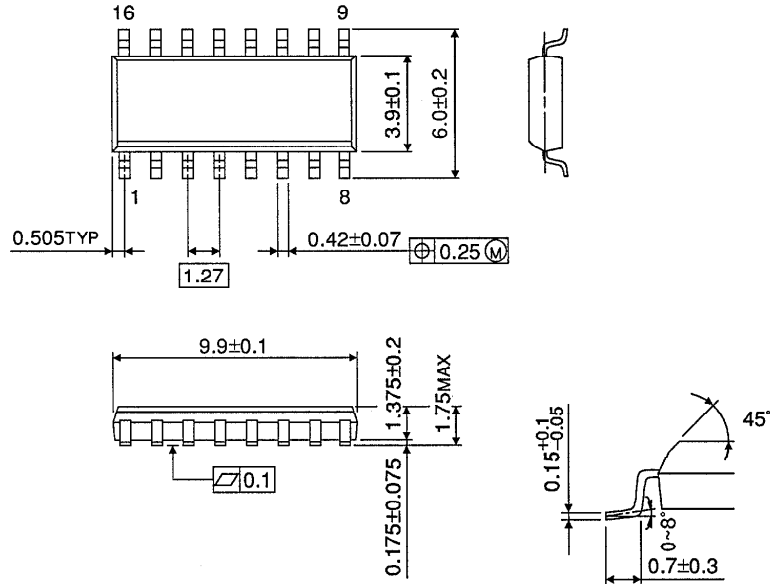
Unit in mm



Weight : 0.18g (TYP.)

**SOP 16PIN (150mil BODY) OUTLINE DRAWING (SOL16-P-150)**

Unit in mm



Weight : 0.13g (TYP.)