

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

**TC74HC161AP, TC74HC161AF, TC74HC161AFN**  
**TC74HC163AP, TC74HC163AF, TC74HC163AFN**

**SYNCHRONOUS PRESETTABLE 4-BIT COUNTER**

**TC74HC161AP/AF/AFN BINARY, ASYNCHRONOUS CLEAR**  
**TC74HC163AP/AF/AFN BINARY, SYNCHRONOUS CLEAR**

(Note) The JEDEC SOP (FN) is not available in Japan.

The TC74HC161A and 163A are high speed CMOS BINARY PRESETTABLE COUNTERs fabricated with silicon gate C<sup>2</sup>MOS technology.

They achieve the high speed operation similar to equivalent STTL while maintaining the CMOS low power dissipation. The CK input is active on the rising edge. Both  $\overline{\text{LOAD}}$  and  $\overline{\text{CLR}}$  inputs are active on low logic level.

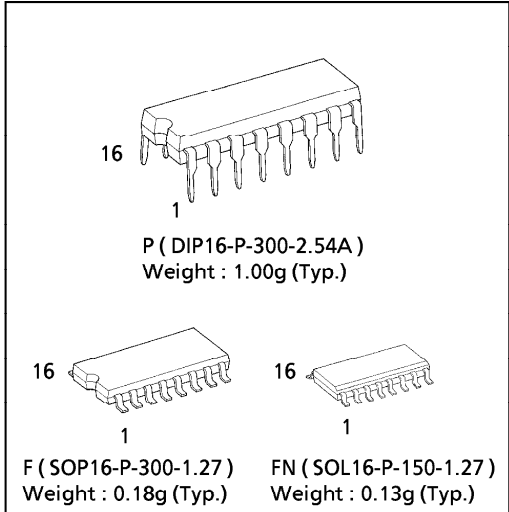
Presetting of all four IC's is synchronous to the rising edge of CK.

The clear function of the TC74HC163A is synchronous to CK, while the TC74HC161A is cleared asynchronously.

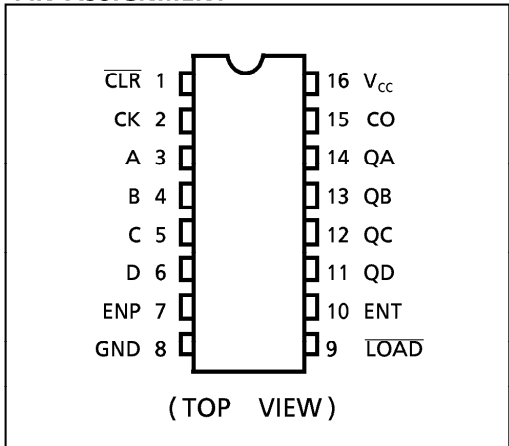
Two enable inputs (ENP and ENT) and CO are provided to enable easy cascading of counters, which facilitates easy implementation of n-bit counters without using external gates. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

**FEATURES:**

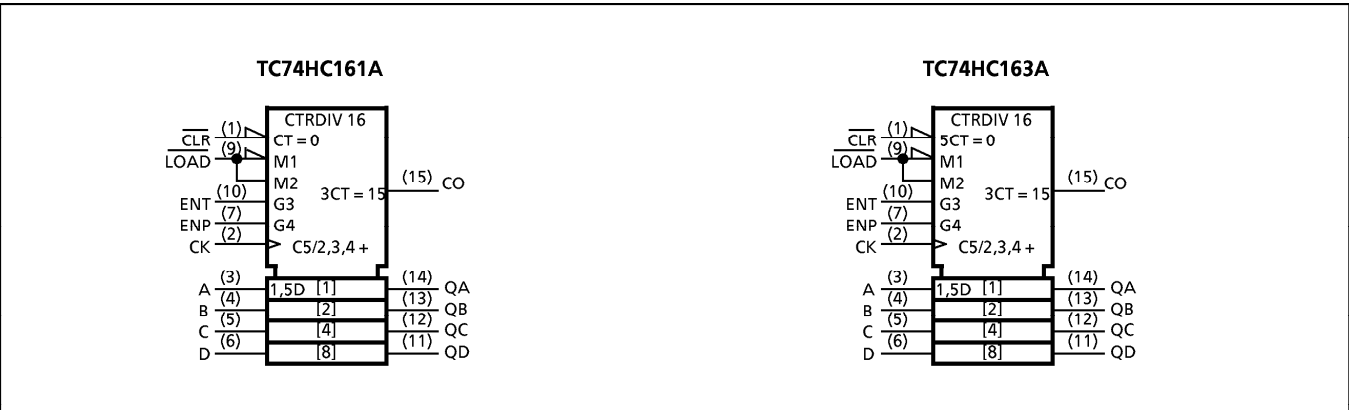
- High Speed.....  $f_{\text{MAX}} = 63\text{MHz}(\text{typ.})$  at  $V_{\text{CC}} = 5\text{V}$
- Low Power Dissipation.....  $I_{\text{CC}} = 4\mu\text{A}(\text{Max.})$  at  $T_a = 25^\circ\text{C}$
- High Noise Immunity.....  $V_{\text{NIH}} = V_{\text{NIL}} = 28\% V_{\text{CC}}(\text{Min.})$
- Output Drive Capability..... 10 LSTTL Loads
- Symmetrical Output Impedance...  $|I_{\text{OH}}| = |I_{\text{OL}}| = 4\text{mA}(\text{Min.})$
- Balanced Propagation Delays.....  $t_{\text{PLH}} \approx t_{\text{PHL}}$
- Wide Operating Voltage Range...  $V_{\text{CC}}(\text{opr.}) = 2\text{V} \sim 6\text{V}$
- Pin and Function Compatible with 74LS160~163



**PIN ASSIGNMENT**



**IEC LOGIC SYMBOL**



961001EBA2

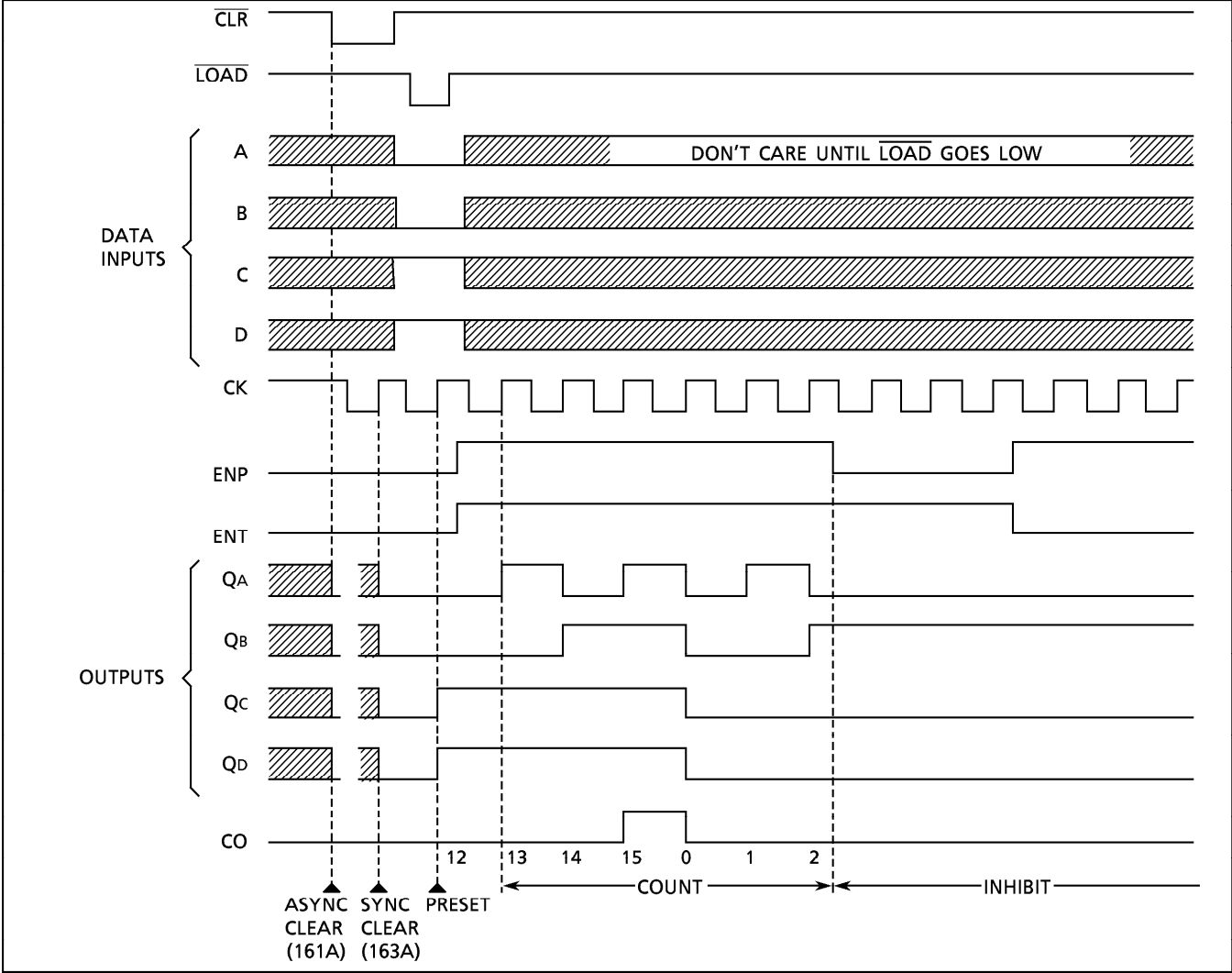
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TRUTH TABLE

TC74HC161A					TC74HC163A					OUTPUTS				FUNCTION
INPUTS					INPUTS					QA	QB	QC	QD	
CLR	LD	ENP	ENT	CK	CLR	LD	ENP	ENT	CK	L	L	L	L	RESET TO "0"
L	X	X	X	X	L	X	X	X	X	A	B	C	D	PRESET DATA
H	L	X	X	X	H	L	X	X	X	NO CHANGE				NO COUNT
H	H	X	L	X	H	H	X	L	X	NO CHANGE				NO COUNT
H	H	L	X	X	H	H	L	X	X	NO CHANGE				NO COUNT
H	H	H	H	X	H	H	H	H	X	COUNT UP				COUNT
H	X	X	X	X	X	X	X	X	X	NO CHANGE				NO COUNT

Note    X            : Don't Care  
          A, B, C, D : Logic Level of Data Inputs  
          Carry       : CARRY = ENT·QA · QB · QC · QD

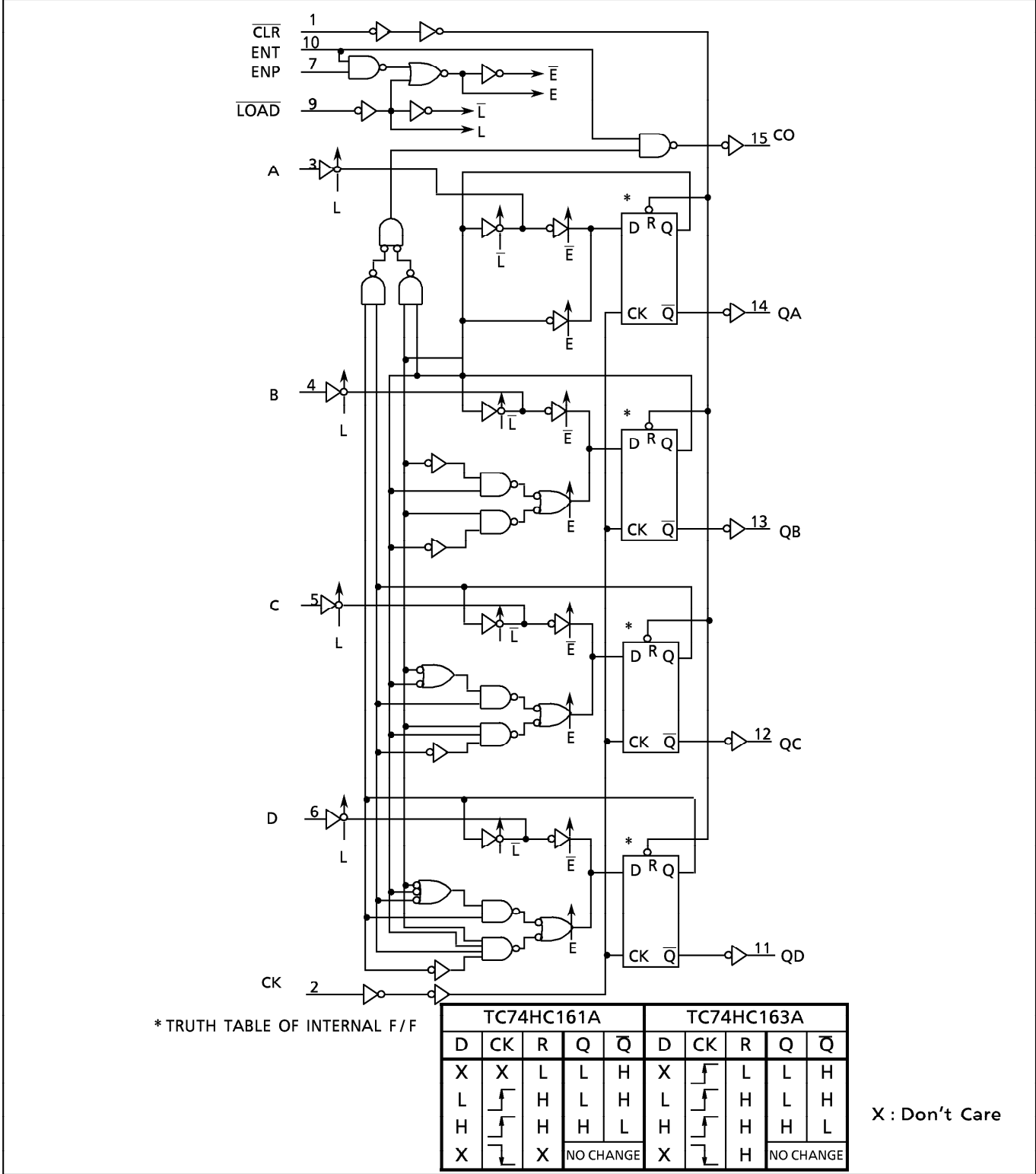
TIMING CHART



961001EBA2'

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SYSTEM DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	$V_{CC}$	$-0.5 \sim 7$	V
DC Input Voltage	$V_{IN}$	$-0.5 \sim V_{CC} + 0.5$	V
DC Output Voltage	$V_{OUT}$	$-0.5 \sim V_{CC} + 0.5$	V
Input Diode Current	$I_{IK}$	$\pm 20$	mA
Output Diode Current	$I_{OK}$	$\pm 20$	mA
DC Output Current	$I_{OUT}$	$\pm 25$	mA
DC $V_{CC}$ / Ground Current	$I_{CC}$	$\pm 50$	mA
Power Dissipation	$P_D$	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	$T_{stg}$	$-65 \sim 150$	°C

\*500mW in the range of  $T_a = -40^\circ\text{C} \sim 65^\circ\text{C}$ . From  $T_a = 65^\circ\text{C}$  to  $85^\circ\text{C}$  a derating factor of  $-10\text{mW}/^\circ\text{C}$  shall be applied until 300mW.

## RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	$V_{CC}$	$2 \sim 6$	V
Input Voltage	$V_{IN}$	$0 \sim V_{CC}$	V
Output Voltage	$V_{OUT}$	$0 \sim V_{CC}$	V
Operating Temperature	$T_{opr}$	$-40 \sim 85$	°C
Input Rise and Fall Time	$t_r, t_f$	$0 \sim 1000$ ( $V_{CC} = 2.0\text{V}$ ) $0 \sim 500$ ( $V_{CC} = 4.5\text{V}$ ) $0 \sim 400$ ( $V_{CC} = 6.0\text{V}$ )	ns

## DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	$V_{CC}$ (V)	$T_a = 25^\circ\text{C}$			$T_a = -40 \sim 85^\circ\text{C}$		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	$V_{IH}$		2.0 4.5 6.0	1.50 3.15 4.20	— — —	— — —	1.50 3.15 4.20	— — —	V
Low - Level Input Voltage	$V_{IL}$		2.0 4.5 6.0	— — —	— — —	0.50 1.35 1.80	— — —	0.50 1.35 1.80	V
High - Level Output Voltage	$V_{OH}$	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -20\mu\text{A}$	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	— — —	1.9 4.4 5.9	V
			$I_{OH} = -4 \text{ mA}$	4.5	4.18	4.31	—	4.13	
			$I_{OH} = -5.2 \text{ mA}$	6.0	5.68	5.80	—	5.63	
Low - Level Output Voltage	$V_{OL}$	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 20\mu\text{A}$	2.0 4.5 6.0	— — —	0.0 0.0 0.1	0.1 0.1 0.1	— — —	V
			$I_{OL} = 4 \text{ mA}$	4.5	—	0.17	0.26	—	
			$I_{OL} = 5.2 \text{ mA}$	6.0	—	0.18	0.26	—	
Input Leakage Current	$I_{IN}$	$V_{IN} = V_{CC} \text{ or GND}$	6.0	—	—	$\pm 0.1$	—	$\pm 1.0$	$\mu\text{A}$
Quiescent Supply Current	$I_{CC}$	$V_{IN} = V_{CC} \text{ or GND}$	6.0	—	—	4.0	—	40.0	

TIMING REQUIREMENTS (Input  $t_r = t_f = 6\text{ns}$ )

PARAMETER	SYMBOL	TEST CONDITION	$V_{CC}(V)$	$T_a = 25^\circ\text{C}$		$T_a = -40 \sim 85^\circ\text{C}$	UNIT
				TYP.	LIMIT	LIMIT	
Minimum Pulse Width (CK)	$t_{W(H)}$ $t_{W(L)}$	Fig. 1	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Pulse Width ( $\overline{\text{CLR}}$ ) *	$t_{W(L)}$	Fig. 4	2.0	—	75	95	
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Set-up Time (LOAD, ENP, ENT)	$t_s$	Fig. 2, 3	2.0	—	100	125	
			4.5	—	20	25	
			6.0	—	17	21	
Minimum Set-up Time (A, B, C, D)	$t_s$	Fig. 2	2.0	—	75	95	
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Set-up Time ( $\overline{\text{CLR}}$ ) **	$t_s$	Fig. 5	2.0	—	75	95	
			4.5	—	15	19	
			6.0	—	13	16	
Minimum Hold Time	$t_h$	Fig. 2, 3, 5	2.0	—	0	0	
			4.5	—	0	0	
			6.0	—	0	0	
Minimum Removal Time ( $\overline{\text{CLR}}$ ) *	$t_{\text{rem}}$	Fig. 4	2.0	—	50	65	
			4.5	—	10	13	
			6.0	—	9	11	
Clock Frequency	f		2.0	—	6	5	MHz
			4.5	—	31	25	
			6.0	—	36	29	

AC ELECTRICAL CHARACTERISTICS ( $C_L = 15\text{pF}$ ,  $V_{CC} = 5\text{V}$ ,  $T_a = 25^\circ\text{C}$ , Input  $t_r = t_f = 6\text{ns}$ )

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	$t_{TLH}$ $t_{THL}$	Fig. 1	—	4	8	ns
Propagation Delay Time (CK—Q)	$t_{PLH}$ $t_{PHL}$	Fig. 1	—	13	21	
Propagation Delay Time (CK—CO) [Count Mode]	$t_{PLH}$ $t_{PHL}$	Fig. 1	—	16	26	
Propagation Delay Time (CK—CO) [Preset Mode]	$t_{PLH}$	Fig. 2	—	18	30	
	$t_{PHL}$		—	20	35	
Propagation Delay Time (ENT—CO)	$t_{PLH}$ $t_{PHL}$	Fig. 6	—	10	17	
Propagation Delay Time ( $\overline{\text{CLR}}$ —Q) *	$t_{PHL}$	Fig. 4	—	17	26	
Propagation Delay Time ( $\overline{\text{CLR}}$ —CO) *	$t_{PHL}$	Fig. 4	—	20	35	MHz
Maximum Clock Frequency	$f_{\text{MAX}}$		36	63	—	

\*: for TC74HC161A only

\*\*: for TC74HC163A only

AC ELECTRICAL CHARACTERISTICS (  $C_L = 50\text{pF}$ , Input  $t_r = t_f = 6\text{ns}$  )

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C				Ta = -40~85°C		UNIT
			V <sub>CC</sub> (V)	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t <sub>TLH</sub> t <sub>THL</sub>		2.0	—	25	75	—	95	ns
			4.5	—	7	15	—	19	
			6.0	—	6	13	—	16	
Propagation Delay Time (CK—Q)	t <sub>pLH</sub> t <sub>pHL</sub>	Fig. 1	2.0	—	48	125	—	155	
			4.5	—	16	25	—	31	
			6.0	—	14	21	—	26	
Propagation Delay Time (CK—CO) [ Count Mode ]	t <sub>pLH</sub> t <sub>pHL</sub>	Fig. 1	2.0	—	57	150	—	190	
			4.5	—	19	30	—	38	
			6.0	—	16	26	—	33	
Propagation Delay Time (CK—CO) [ Preset Mode ]	t <sub>pLH</sub>	Fig. 2	2.0	—	66	175	—	220	
			4.5	—	22	35	—	44	
			6.0	—	19	30	—	37	
	t <sub>pHL</sub>		2.0	—	72	200	—	250	
			4.5	—	24	40	—	50	
			6.0	—	20	34	—	43	
Propagation Delay Time (ENT—CO)	t <sub>pLH</sub> t <sub>pHL</sub>	Fig. 6	2.0	—	39	100	—	125	
			4.5	—	13	20	—	25	
			6.0	—	11	17	—	21	
Propagation Delay Time (CLR—Q)*	t <sub>pHL</sub>	Fig. 4	2.0	—	60	150	—	190	
			4.5	—	20	30	—	38	
			6.0	—	17	26	—	33	
Propagation Delay Time ( $\overline{\text{CLR}}$ —CO)*	t <sub>pHL</sub>	Fig. 4	2.0	—	72	200	—	250	
			4.5	—	24	40	—	50	
			6.0	—	20	34	—	43	
Maximum Clock Frequency	f <sub>MAX</sub>		2.0	6	18	—	5	—	MHz
			4.5	31	53	—	25	—	
			6.0	36	62	—	29	—	
Input Capacitance	C <sub>IN</sub>			—	5	10	—	10	pF
Power Dissipation Capacitance	C <sub>PD</sub> (1)	( Note 1 )		—	34	—	—	—	

Note (1)  $C_{\text{PD}}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{\text{CC}}(\text{opr}) = C_{\text{PD}} \cdot V_{\text{CC}} \cdot f_{\text{IN}} + I_{\text{CC}}$$

When the outputs drive a capacitive load, total current consumption is the sum of  $C_{\text{PD}}$ , and  $\Delta I_{\text{CC}}$  which is obtained from the following formula :

In case of TC74HC161A / 163A :

$$\Delta I_{\text{CC}} = f_{\text{CK}} \cdot V_{\text{CC}} \left( \frac{C_{\text{QA}}}{2} + \frac{C_{\text{QB}}}{4} + \frac{C_{\text{QC}}}{8} + \frac{C_{\text{QD}}}{16} + \frac{C_{\text{CO}}}{16} \right)$$

$C_{\text{QA}} \sim C_{\text{QD}}$  and  $C_{\text{CO}}$  are the capacitances at QA~QD and CO, respectively.

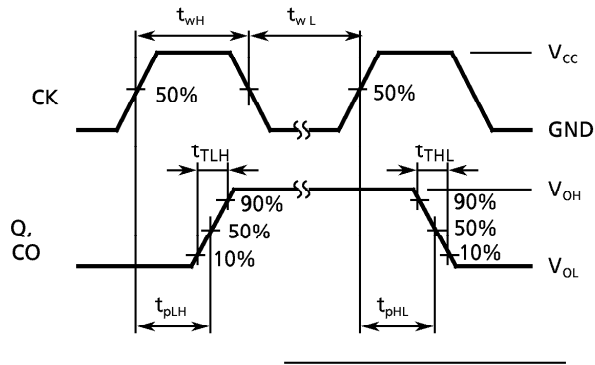
$f_{\text{CK}}$  is the input frequency of the CK.

(2) \* for TC74HC161A only

**SWITCHING CHARACTERISTICS TEST WAVEFORM**

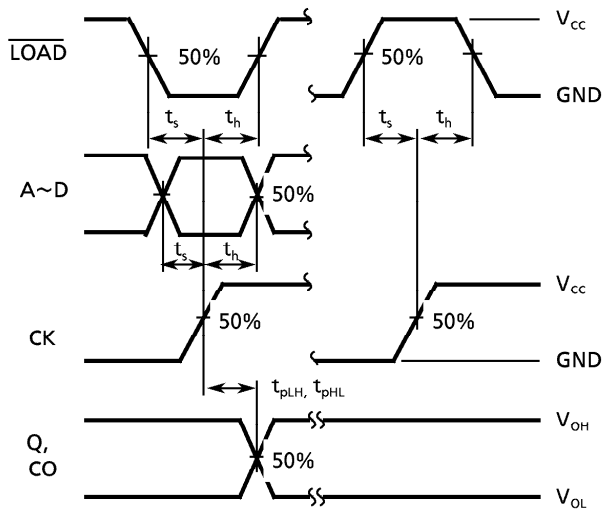
**COUNT MODE**

**( Fig. 1 )**



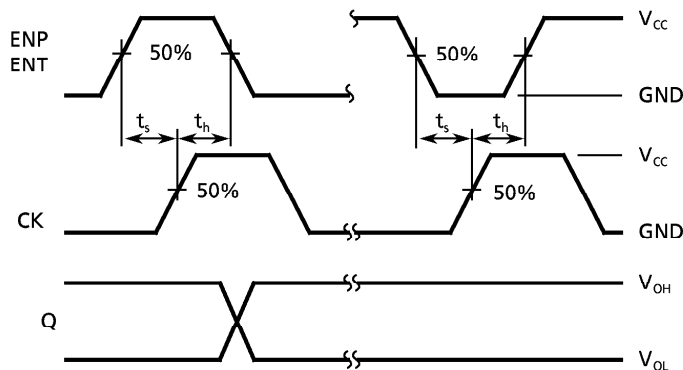
**PRESET MODE**

**( Fig. 2 )**



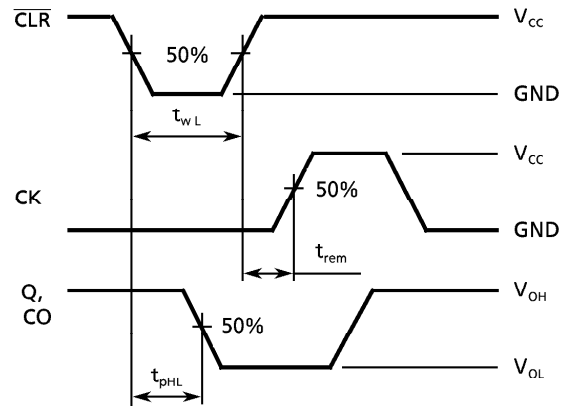
**COUNT ENABLE MODE**

**( Fig. 3 )**



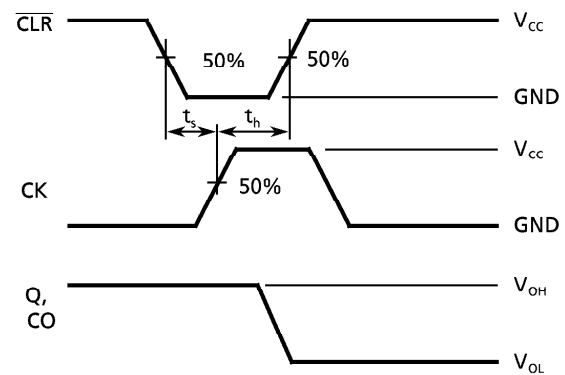
**CLEAR MODE (TC74HC161A)**

**( Fig. 4 )**



**CLEAR MODE (TC74HC163A)**

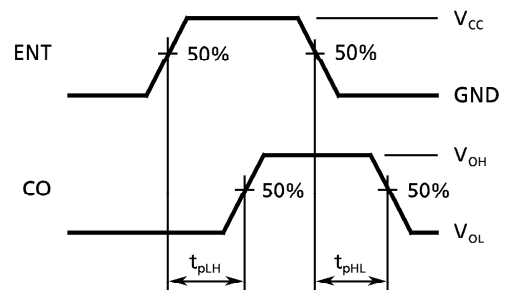
**( Fig. 5 )**



**CASCADE MODE**

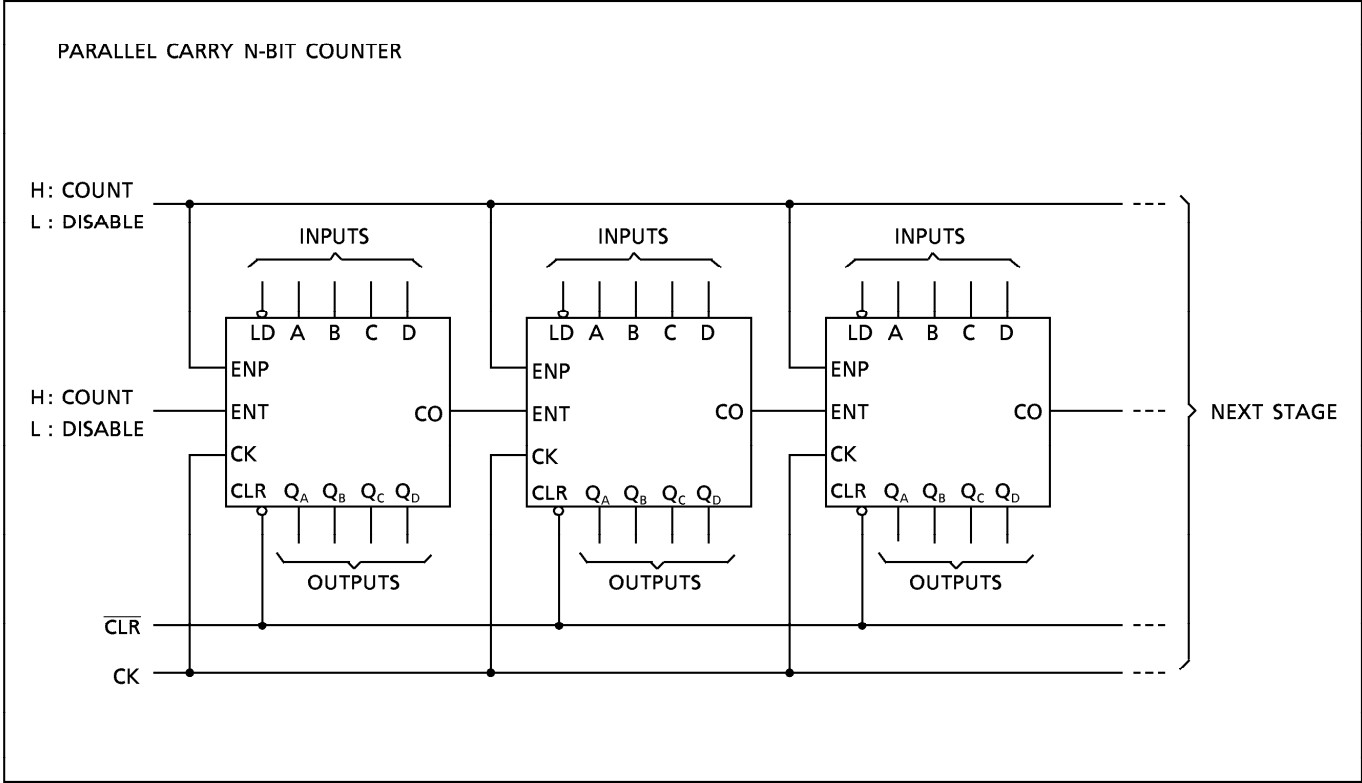
**(Fix Maximum Count)**

**( Fig. 6 )**



TYPICAL APPLICATION

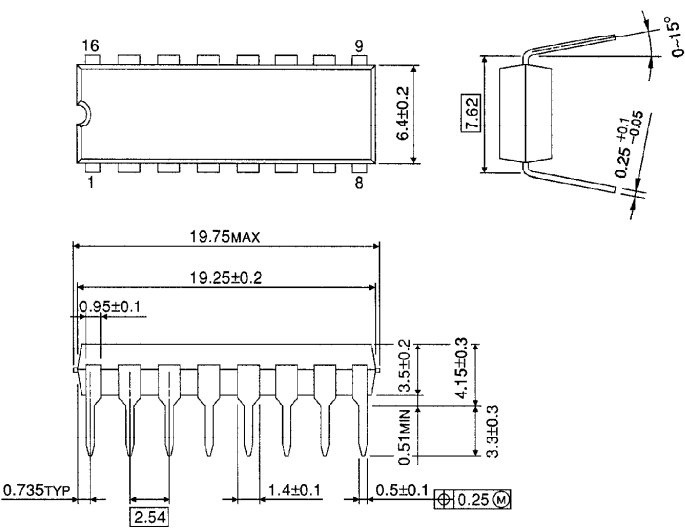
PARALLEL CARRY N-BIT COUNTER





DIP 16PIN OUTLINE DRAWING (DIP16-P-300-2.54A )

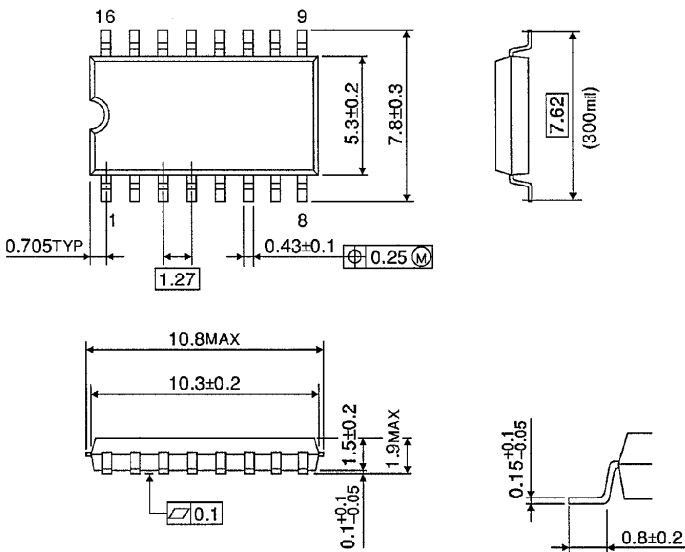
Unit in mm



Weight : 1.00g (Typ.)

SOP 16PIN ( 200mil BODY ) OUTLINE DRAWING ( SOP16-P-300-1.27 )

Unit in mm

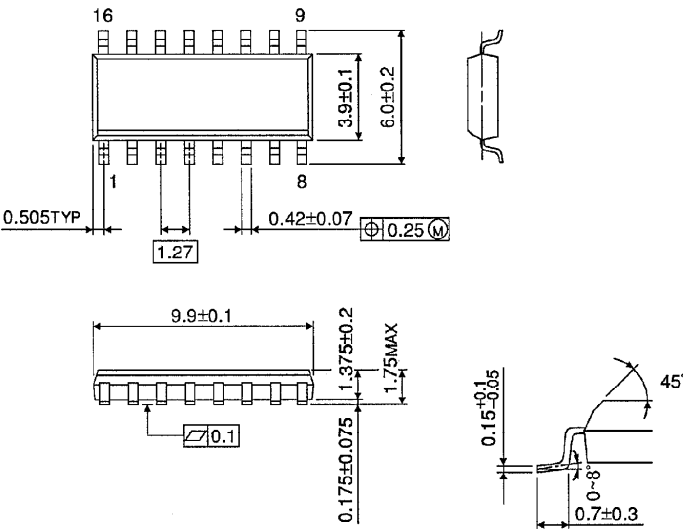


Weight : 0.18g (Typ.)

SOP 16PIN ( 150mil BODY ) OUTLINE DRAWING ( SOL14-P-150 -1.27)

Unit in mm

(Note) This package is not available in Japan.



Weight : 0.13g (Typ.)