

CMOS 4-BIT MICROCONTROLLER

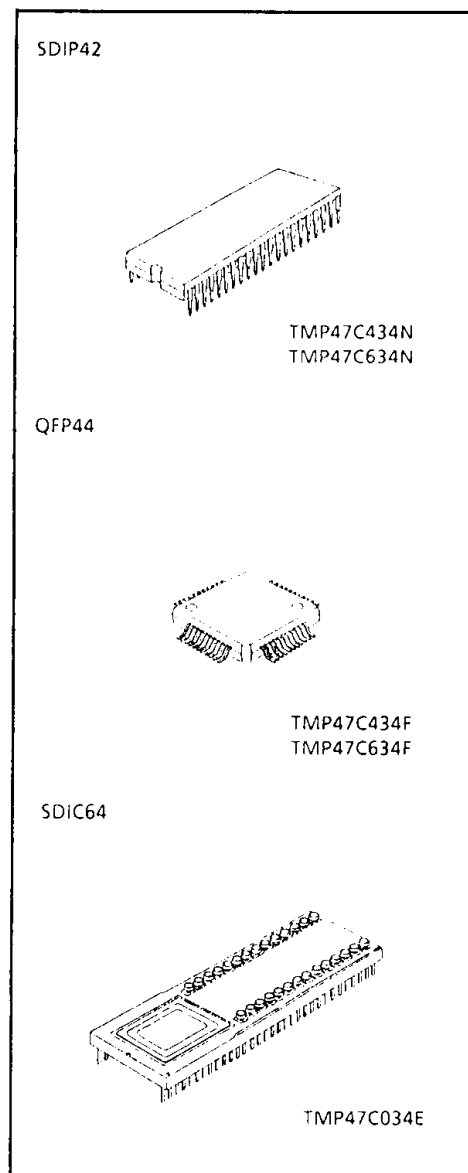
TMP47C434N, TMP47C634N
TMP47C434F, TMP47C634F

The 47C434/634 are based on the TLC5-470 CMOS series. The 47C434/634 have on-screen display circuit to display characters and marks which indicate channel or time on TV screen, A/D converter input, and D/A converter output.

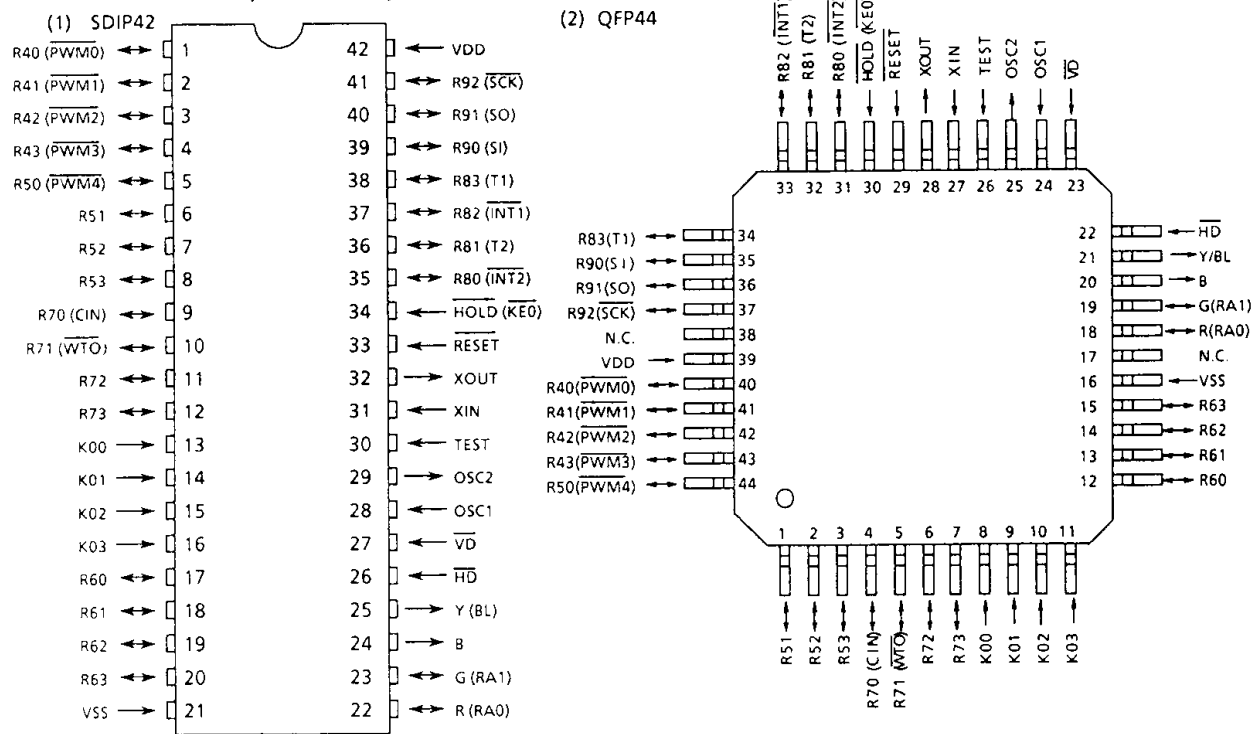
PART No.	ROM	RAM	PACKAGE	PIGGYBACK (adapter socket)
TMP47C434N TMP47C434F	4096 × 8-bit	256 × 4-bit	SDIP42 QFP44	TMP47C034E (BM1105)
TMP47C634N TMP47C634F	6144 × 8-bit	384 × 4-bit	SDIP42 QFP44	TMP47C034E (BM1105)

FEATURES

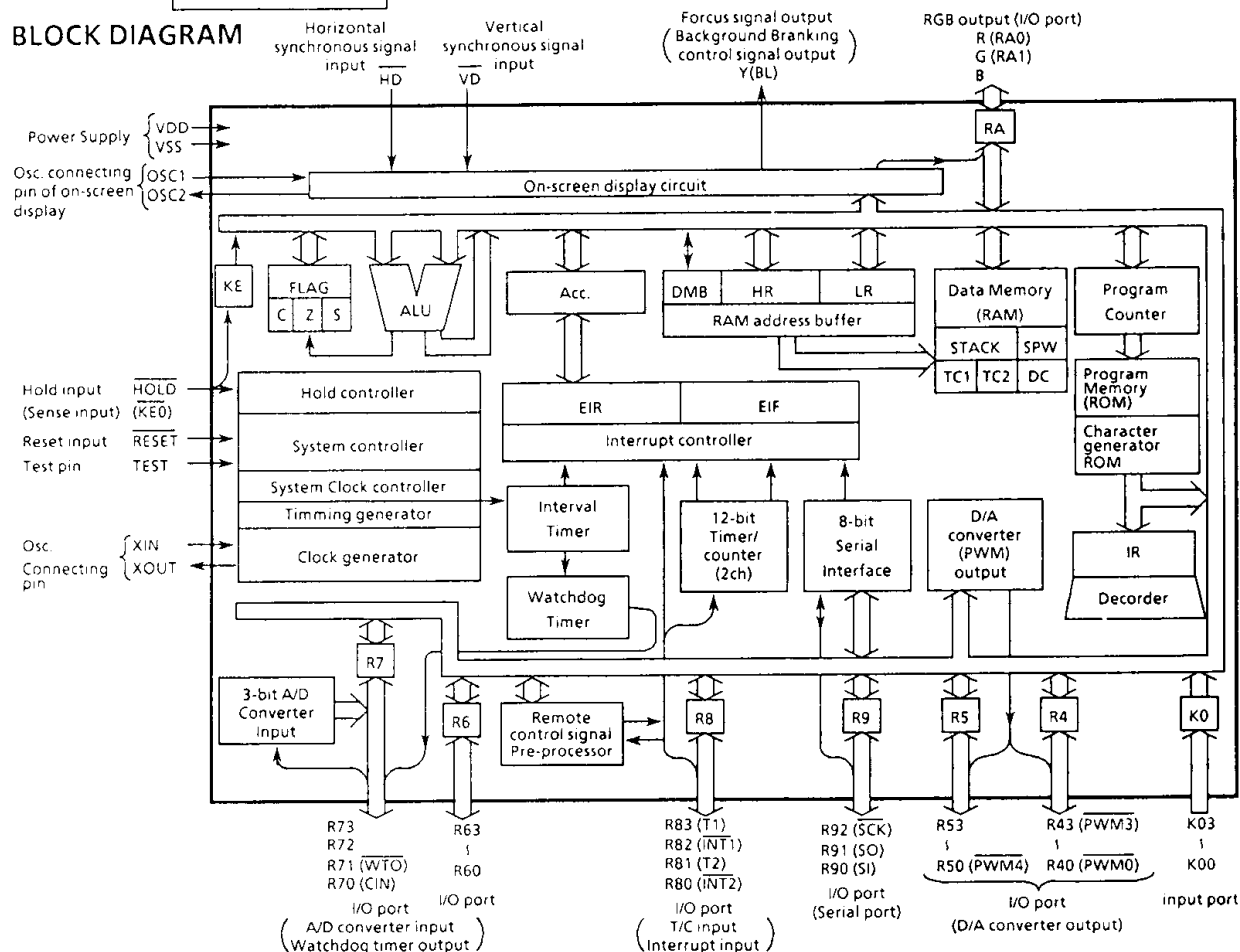
- ◆ 4-bit single chip microcomputer
- ◆ Instruction execution time : 1.9 μ s (at 4.2 MHz)
- ◆ 92 basic instructions
- ◆ Table look-up instructions
- ◆ Subroutine nesting : 15 levels max.
- ◆ 6 interrupt sources (External : 2, Internal : 4)
All sources have independent latches each, and multiple interrupt control is available
- ◆ I/O port (30 pins)
 - Input 2 ports 5 pins
 - I/O 7 ports 25 pins
- ◆ Interval Timer
- ◆ Two 12-bit Timer/Counters
Timer, event counter, and pulse width measurement mode
- ◆ Watchdog timer
- ◆ Serial Interface with 8-bit buffer
 - Simultaneous transmission and reception capability
 - External/internal clock, leading/trailing edge shift, 4/8-bit
- ◆ On-screen display circuit
 - Character patterns : 48 characters
 - Characters displayed : 16 columns × 2 lines
 - Composition : 8 × 8 dots (smoothing function)
 - Size of character : 2 kinds (line by line)
 - Color of character : 7 kinds (character by character)
 - Variable display position : horizontal / vertical 64 steps
- ◆ D/A converter (Pulse width modulation) outputs
 - 14-bit resolution 1 channel
 - 6-bit resolution 4 channels
- ◆ 3-bit A/D converter input
Auto frequency control signal (S-shaped curve) detection
- ◆ Horizontal synchronous signal is detected by timer/counter
- ◆ Remote control signal preprocessing capability
- ◆ High current outputs
LED direct drive capability (typ. 20mA × 4 bits)
- ◆ HOLD function : Battery/Capacitor back-up
- ◆ Real Time Emulator : BM47C834A



PIN ASSIGNMENT (TOP VIEW)



BLOCK DIAGRAM



PIN FUNCTION

PIN NAME	Input/Output	FUNCTIONS	
K03 - K00	input	4-bit input port	
R43 ($\overline{\text{PWM3}}$) R41 ($\overline{\text{PWM1}}$) R40 ($\overline{\text{PWM0}}$)	I/O (output)	4-bit I/O port with latch. When used as input port or D/A converter outputs pins, the latch must be set to "1".	6-bit D/A converter (PWM) output
R53 - R51	I/O		14-bit D/A converter (PWM) output
R50 ($\overline{\text{PWM4}}$)	I/O (output)		6-bit D/A converter (PWM) output
R63 - R60	I/O	4-bit I/O port with latch. When used as input port, the latch must be set to "1".	
R73 - R72	I/O	4-bit I/O port with latch. When used as input port, watchdog timer output pin, or A/D converter input pin, the latch must be set to "1".	
R71 ($\overline{\text{WTO}}$)	I/O (output)		Watchdog timer output
R70 (CIN)	I/O (input)		3-bit A/D converter input
R83 (T1) R82 ($\overline{\text{INT1}}$) R81 (T2) R80 ($\overline{\text{INT2}}$)	I/O (input)	4-bit I/O port with latch. When used as input port, external interrupt input pin, or timer/counter external input pin, the latch must be set to "1".	Timer/counter 1 external input
			External interrupt 1 input
			Timer/counter 2 external input
			External interrupt 2 input
R92 ($\overline{\text{SCK}}$) R91 (SO) R90 (SI)	I/O (I/O) I/O (output) I/O (input)	3-bit I/O port with latch. When used as input port or serial port, the latch must be set to "1".	Serial clock I/O
			Serial data output
			Serial data input
G (RA1) R (RA0) B	Output (I/O) Output	RGB output	2-bit I/O port with latch. When used as input port, the latch must be set to "1"
Y (BL)	Output (output)		Background blanking control signal output
HD , $\overline{\text{VD}}$	Input	Horizontal synchronous signal input, Vertical synchronous signal input	
OSC1, OSC2	input, output	Resonator connecting pin of on-screen display circuit	
XIN, XOUT	input, output	Resonator connecting pin. For inputting external clock, XIN is used and XOUT is opened.	
$\overline{\text{RESET}}$	input	Reset signal input	
$\overline{\text{HOLD}}$ (KE0)	input (input)	HOLD request/release signal input	Sense input
TEST	input	Test pin for out-going test. Be opened or fixed to low level.	
VDD	Power supply	+ 5V	
VSS		0V (GND)	

OPERATIONAL DESCRIPTION

Concerning the 47C434/634, the configuration and functions of hardwares are described.

As the description is provided with priority on those parts differing from the 47C660/860, the technical data sheets for the 47C660/860 shall also be referred to.

1. SYSTEM CONFIGURATION

- (1) Program Memory (ROM)
- (2) Data Memory (RAM)
- (3) Operation clock changeover control
- (4) I/O Ports
- (5) On-screen display (OSD) control circuit
- (6) A/D converter (comparator) input
- (7) D/A converter (Pulse Width Modulation) output

2. INTERNAL CPU FUNCTION

2.1 Program Memory(ROM)

Programs are stored in address 0000 to 17FF_H of 47C634 and in address 0000 to 0FFF_H of 47C434. By the ROM data reference instruction [LDH A,@DC + , LDL A,@DC] , the fixed data in address 1000_H to 17FF_H and 0000 to 0FFF_H can be loaded to the accumulator, respectively.

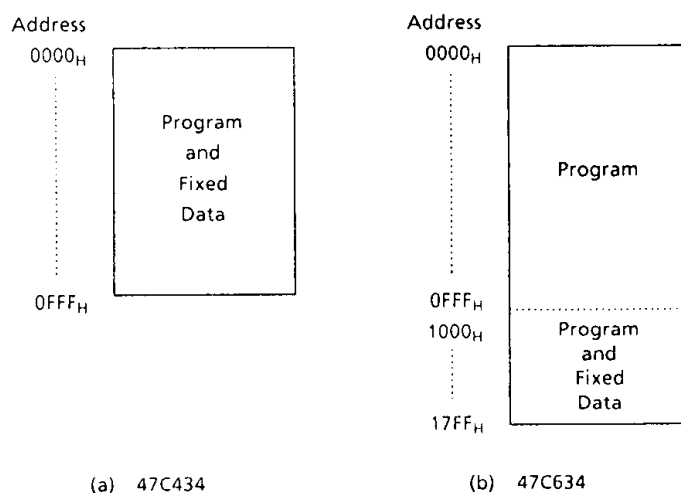


Figure 2-1. Program Memory

Note. With the 47C434, permanent data are stored at addresses 0000 – 0FFF_H but, when checking 47C434 operation using a piggy-back chip, it is necessary to store the permanent data to addresses 1000 – 1FFF_H, either.

2.2 Data memory (RAM)

The 47C634 contains 256×4 bits data memory bank 0 (DMB0) and 128×4 bits data memory bank 1 (DMB1). The 47C434 contains 256×4 bits data memory (DMB0). The bank is controlled by DMB.

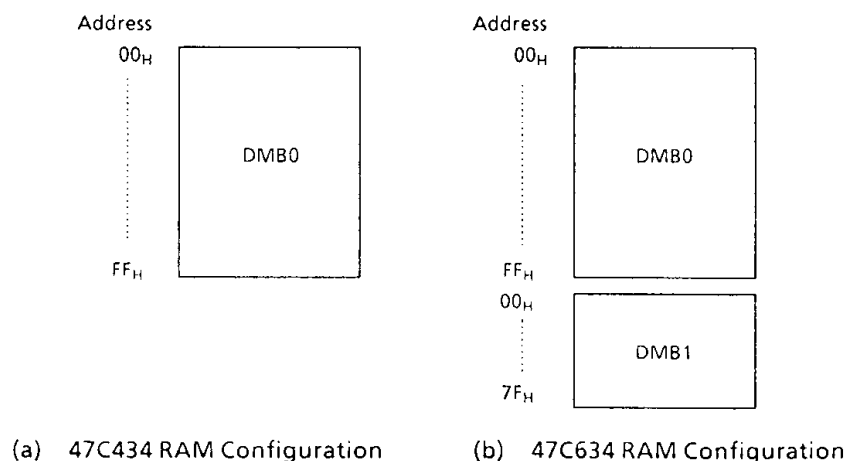


Figure 2-2. Data Memory (RAM)

2.3 Operation clock changeover control

On the 47C434/634 only single clock mode is available. As single clock mode is automatically selected at the initialization, there is no necessary to set system clock control command register (OP16).

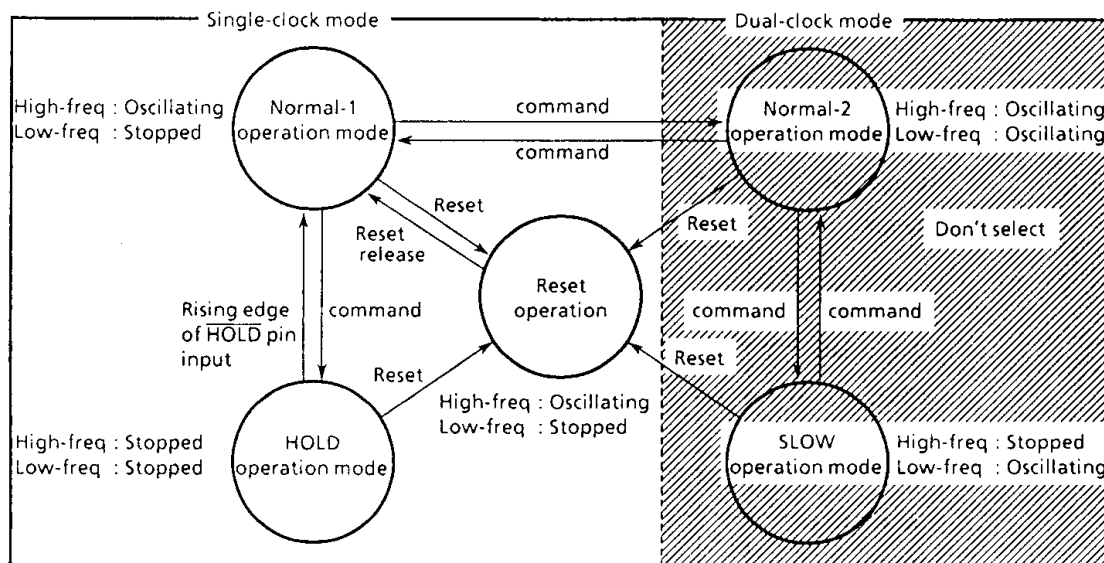


Figure 2-3. Operation Mode Transition Diagram

3. PERIPHERAL HARDWARE FUNCTION

3.1 I/O ports

The 47C434/634 have 9 I/O ports (30 pins) each as follows.

- ① K0 ; 4-bit input
- ② R4, R5 ; 4-bit input/output (shared with pulse width modulation output)
- ③ R6 ; 4-bit input/output
- ④ R7 ; 4-bit input/output (shared with comparator input and watchdog timer output)
- ⑤ R8 ; 4-bit input/output (shared with external interrupt input and timer/counter input)
- ⑥ R9 ; 3-bit input/output (shared with serial port)
- ⑦ RA ; 2-bit input/output (shared with on-screen display output)
- ⑧ KE ; 1-bit sense input (shared with hold request / release signal input)

This section describes ports of ② and ④, which are changed from the 47C660/860, and it describes port of ⑦, which item of on-screen display circuit.

Table 3-1 lists the port address assignments and the I/O instructions that can access the ports.

(1) Port R4 (R43-R40)

This is a 4-bit I/O port with latch. It is a port common to D/A converter(PWM) output port. R4 port output buffers are Tri-state, and each bit of them can be controled independently by the program. Controlling the Tri-state is performed by the command register accessed as port address OP00. When some bit of the OP00 is 0, the corresponding bit of the output buffers becomes high impedance state. The output latch should be set to "1" when the port is used as PWM output port, the PWM output should be to "H" level(PWM data is all "0")when the port is used as R4 port. The output buffers should be set to high impedance state, when the port is used as input port. And the R4 output latch be set to "1", PWM output be set to "High" level, and the output buffer be set to High-Impedance state during reset.

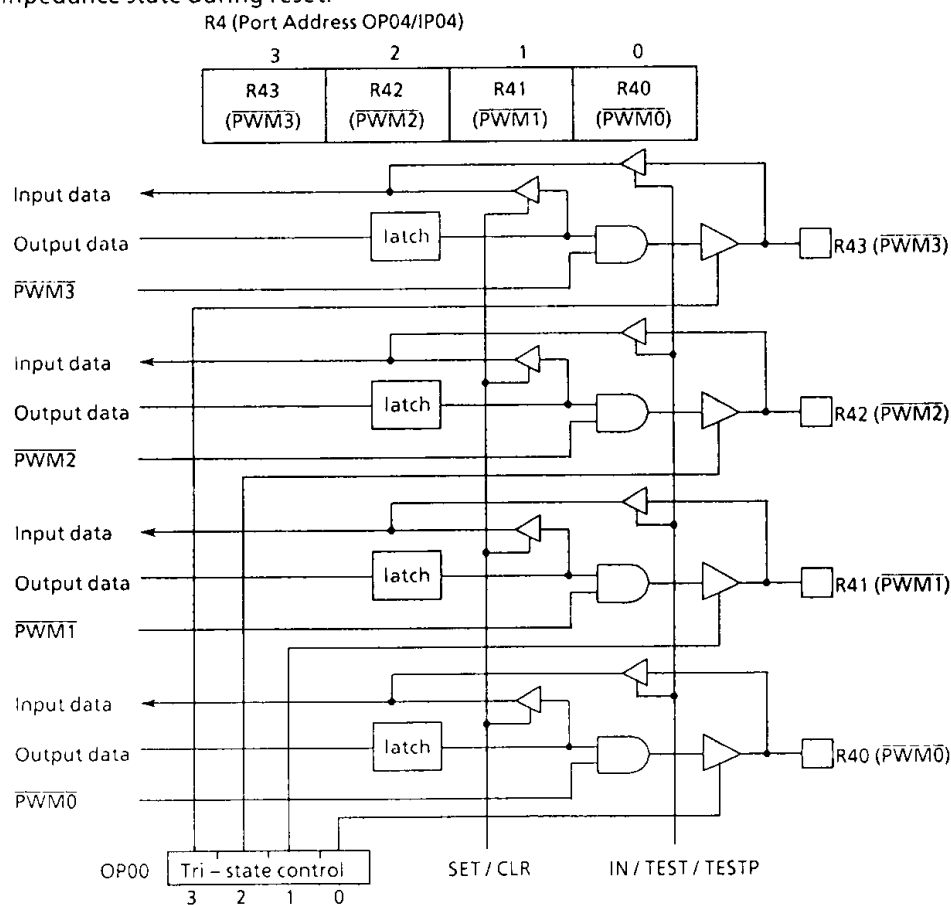


Figure 3-1. Port R4 (PWM)

(2) Port R5 (R53-R50)

The 4-bit I/O port with latch. The only R50 pin share D/A converter (PWM) output. The port output buffers are tri-state, and each bit of them can be controlled independently by the program. Controlling the tri-state is performed by the command register accessed as port address OP13.

```
Example : LD   A, #1111B      ; OP13 ← 1111B
          OUT  A, %OP13
          OUT  #05H, %OP05      ; R5 port ← 5H
```

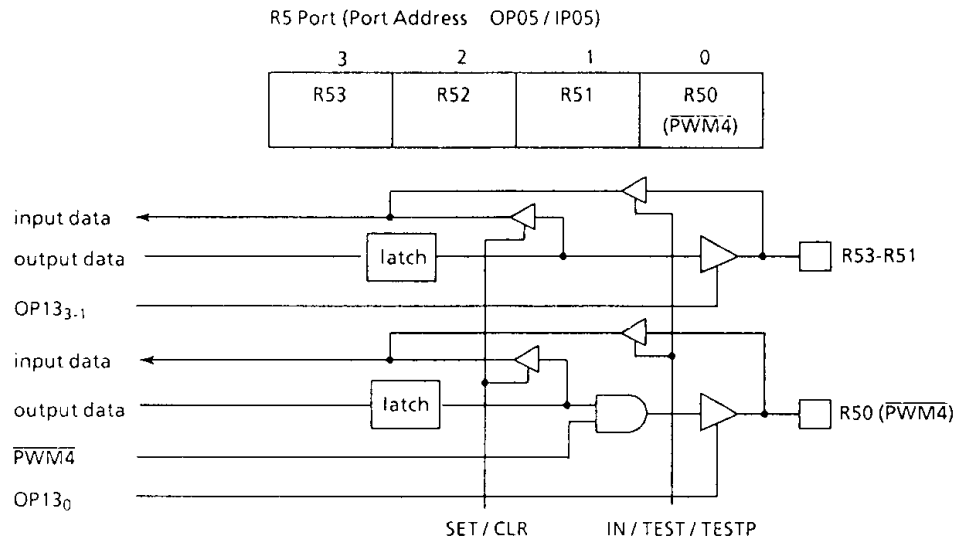


Figure 3-2. Port R5

(3) Port R7 (R73-R70)

The 4-bit I/O port with latch. When used as an input port, the latch should be set to "1". The latch is initialized to "1" during reset. R72, R73 pins is I/O port usually.

Pin R70 (CIN) is shared with the digital input usual and the A/D converter (comparator) input for Auto Frequency Control signal detection. CIN input is comparator input and setting of 3-bit D/A convert for reference voltage are performed by the comand register. Pin R71 (\overline{WTO}) is shared with the watchdog timer output. R70, R71 pins latch is initialized to "1" during reset, and they are able to use I/O port usually.

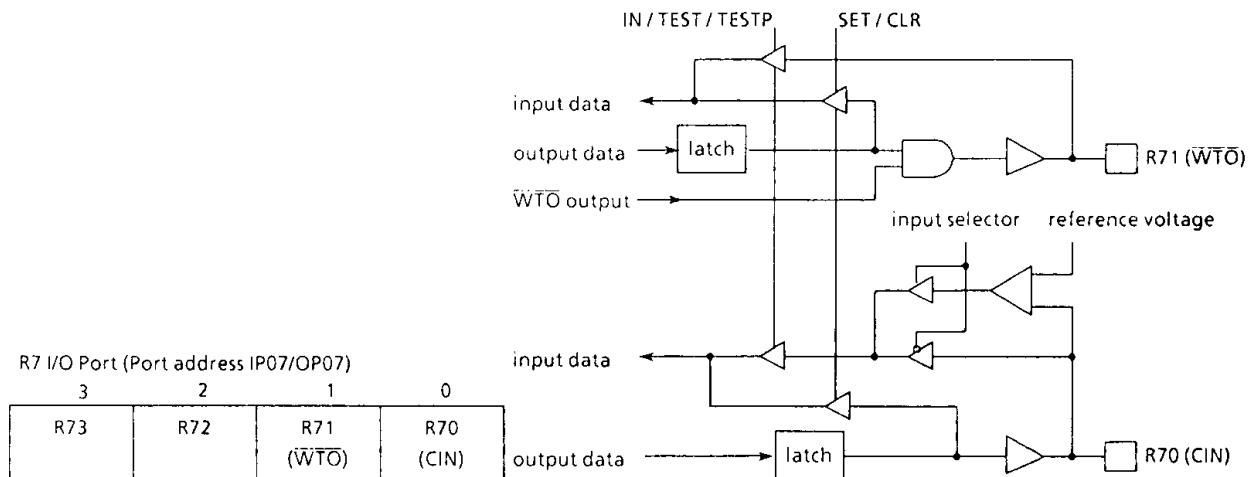


Figure 3-3. Port R7

Port address (**)	Port		I/O instruction					
	Input (IP**)	Output (OP**)	IN %p, A IN %p, @HL	OUT A, %p OUT @HL, %p	OUT #k, %p OUTB@HL	SET %p, b CLR %p, b	TEST %p, b TESTP %p, b	SET @L CLR @L TEST @L
00H	K0 input port	Tri – state(R4 port) control	○	○	○	—	○	—
01	—	—	—	—	—	—	—	—
02	—	—	—	—	—	—	—	—
03	—	—	—	—	—	—	—	—
04	R4 input port	R4 output port	○	○	○	○	○	○
05	R5 input port	R5 output port	○	○	○	○	○	○
06	R6 input port	R6 output port	○	○	○	○	○	○
07	R7 input port	R7 output port	○	○	○	○	○	○
08	R8 input port	R8 output port	○	○	○	○	○	○
09	R9 input port	R9 output port	○	○	○	○	○	○
0A	RA input port	RA output port	○	○	○	○	○	○
0B	—	—	—	—	—	—	—	—
0C	—	OSD command selector	—	—	—	—	—	—
0D	Remote control count value register	Remote control offset valve register	○	○	○	—	—	—
0E	status input (Note 2)	Remote control single preprocess circuit control	○	○	○	—	○	—
0F	Serial receive buffer	Serial transmit buffer	○	○	○	—	—	—
10H	undefined	Hold operation mode	—	—	—	—	—	—
11	undefined	—	—	—	—	—	—	—
12	undefined	A/D converter input control	—	○	—	—	—	—
13	undefined	Tri – state (R5 port) control	—	○	—	—	—	—
14	undefined	—	—	—	—	—	—	—
15	undefined	Watchdog timer control	—	○	—	—	—	—
16	undefined	—	—	—	—	—	—	—
17	undefined	PWM buffer selector	—	○	—	—	—	—
18	undefined	PWM data transfer buffer	—	○	—	—	—	—
19	undefined	Interval timer interrupt control	—	○	—	—	—	—
1A	undefined	OSD control	—	○	—	—	—	—
1B	undefined	—	—	—	—	—	—	—
1C	undefined	Timer/counter 1 control	—	○	—	—	—	—
1D	undefined	Timer/counter 2 control	—	○	—	—	—	—
1E	undefined	SIO control 1	—	○	—	—	—	—
1F	undefined	SIO control 2	—	○	—	—	—	—

Note 1: "—" means the reserved state. Unavailable for the user programs.

Note 2: the status input of serial interface, clock generator, and HOLD (KE0) pin.

Table 3-1. Port Address Assignments and Available I/O Instructions

3.2 On-screen display (OSD) circuit

An on-screen display (OSD) circuit used to display characters and symbols is built into the TV screen. A maximum of 32 characters, as 16 columns \times 2 lines, out of 48 character patterns can be displayed at a time.

3.2.1 OSD Circuit Function

① Number of characters	48 kinds
② Number of characters displayed	32 characters (16 columns \times 2 lines)
③ Composition of a character	8 \times 8 dots (with smoothing function)
④ Size of character	2 kinds (selectable line by line)
⑤ Color of character	7 kinds (selectable character by character)
⑥ Display position variable	horizontal 64 steps, vertical 64 steps

3.2.2 OSD Circuit Configuration

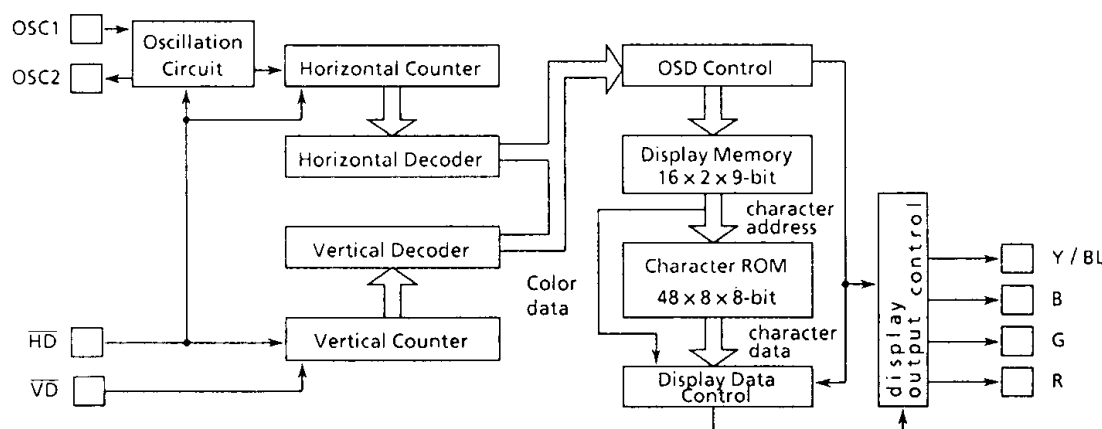


Figure 3-4. OSD Circuit

3.2.3 OSD Circuit Control

The OSD circuit is controlled by the command selector (OP0C) and control register (OP1A). Table 3-2 shows the relationship between OP0C and OP1A. OP1A is multiplexed with the six output control registers which control the display start position, color of character and character size of character, and the two transfer control registers which transfer character data to the display memory.

The output control registers consist of 8 bits and all bits can be written by accessing OP1A two times. However, the second access is not required unless the second data are changed. The addressed "0 to 5" are assigned to the six output control registers. OP1A can be accessed by writing the address of the control register where data are to be changed to OP0C. The transfer control registers can be accessed by writing "6" or "7" to OP0C. The transfer control registers have a 12-bit configuration and can access OP1A three times succession. The first access sets which column is displayed within one line 16 columns. The second and third accesses written 6 bit of character data.

The display memory has a 16-columns \times 9-bit \times 2 lines configuration with a one-to-one correspondence to the number of columns displayed on the screen. The display data consist of 6 character data bits and 3 color data bits for a total of 9 bits. When "6" is written to OP0C, line 1 is stored to the display memory, when "7" is written to OP0C, line 2 is stored. That is after accessing OP0C, the character data specified the second and third times are written to the display memory area specified in the first OP1A access together with the color data loaded to control register DCR50. Thus color can be specified for each character. After setting of all control registers is completed, the character data read from the character ROM(00 to 2FH) are output to the R, G and B pins together with the color data by setting OP0C to "F".

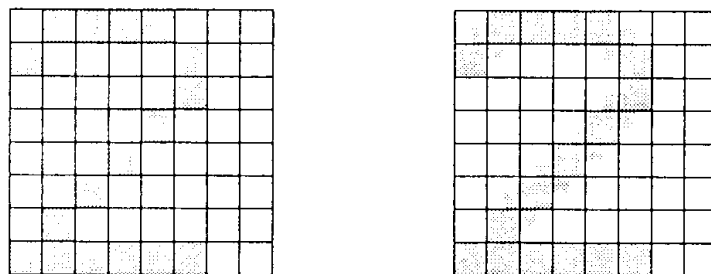
OSD command selector (OP0C)	OSD control register to be accessed through OP1A			
0	Control for the horizontal start position of the first display line			
		3	2	1 0
DCR00	—	—	HS15	HS14 (1st access)
DCR01	HS13	HS12	HS11	HS10 (2st access)
1	Control for the vertical start position of the first display line			
		3	2	1 0
DCR10	—	—	VS15	VS14 (1st access)
DCR11	VS13	VS12	VS11	VS10 (2st access)
2	Control for the horizontal start position of the second display line.			
		3	2	1 0
DCR20	—	—	HS25	HS24 (1st access)
DCR21	HS23	HS22	HS21	HS20 (2st access)
3	Control for the vertical start position of the second display line.			
		3	2	1 0
DCR30	—	—	VS25	VS24 (1st access)
DCR31	VS23	VS22	VS21	VS20 (2st access)
4	Control for the character sizes,smoothing switch and OSD output polarities			
		3	2	1 0
DCR40	CS21	CS20	CS11	CS10 (1st access)
DCR41	ESMZ	BLIV	YIV	RGBIV (2st access)
5	Control for the color register and OSD output buffers' tri-state'			
		3	2	1 0
DCR50	—	RDT	GDT	BDT (1st access)
DCR51	EBF3	EBF2	EBF1	EBF0 (2st access)
6	display memory write mode for the first display line(address 00-0F)			
		3	2	1 0
	DMA3	DMA2	DMA1	DMA0 (1st access)
	—	—	CRA5	CRA4 (2st access)
	CRA3	CRA2	CRA1	CRA0 (3st access)
7	display memory write mode for the second display line(address 10-1F)			
		3	2	1 0
	DMA3	DMA2	DMA1	DMA0 (1st access)
	—	—	CRA5	CRA4 (2st access)
	CRA3	CRA2	CRA1	CRA0 (3st access)
E	display OFF			
F	display ON			

Table 3-2. OSD control commands and control registers

(1) Composition of character and smoothing function

Each character is composed by 8×8 dots. Each dot corresponds to a bit in the character ROM. Figure 3-5. (a) shows an example Composition of a character.

Smoothing function is the function to make characters look smooth. In the time the smoothing function is enabled, additional dots are displayed in the middle of the place where two dots contact each other only at a corner. Controlling of the smoothing function is performed by ESMZ in the OSD control register DCR41. Figure 3-5. (b) shows an example of the smoothing function.



(a) without smoothing

(b) with smoothing

Figure 3-5. Composition of character and smoothing function

(2) Character size and color to display

Size of the characters displayed on screen is selectable line by line from 2 sizes. The size of the first and second display line is designated by CS11-CS10 and CS21-CS20 in the OSD control register DCR40, respectively.

Table 3-3 shows the setting values and character sizes of DCR40.

Table 3-4 shows the display character sizes.

One out of seven colors can be selected for each character to be displayed and are determined by RDT, GDT, and BDT of DCR50. The color data are written to the display memory automatically at the same time as character data are written

Character size (DCR40)	second display line		first display line	
	CS21	CS20	CS11	CS10
small character	1	0	1	0
large character	0	1	0	1
display OFF	0	0	0	0

Figure 3-3. Designation of character size

	small character	large character
dot size	$2T_{HD} \times 2T_{OSC}$	$4T_{HD} \times 4T_{OSC}$
character size	$16T_{HD} \times 16T_{OSC}$	$32T_{HD} \times 32T_{OSC}$

Note. T_{HD} : the period of horizontal synchronous signal
 T_{OSC} : the period of OSD clock oscillation

Figure 3-4. character size.

colors displayed on screen	color data(DCR50)		
	RDT	GDT	BDT
Blank	0	0	0
Blue	0	0	1
Green	0	1	0
Sian	0	1	1
Red	1	0	0
Mazenda	1	0	1
Yellow	1	1	0
White	1	1	1

Note. Color to display : RGB pin uses Red, Green, Blue such as.

Table 3-5. select of color to display

(3) Display start position

Display start position of each display line on screen can be shifted by software.

The vertical and horizontal display starting position for the first line is determined by HS10 to 15 and VS10 to 15 of DCR00 to 11.

The vertical and horizontal display starting position for the second line is determined by HS20 to 25 and VS20 to 25 of DCR20 to 31. Each has a resolution of 64 steps.

The control register and display line on screen are shown in Table 3-6.

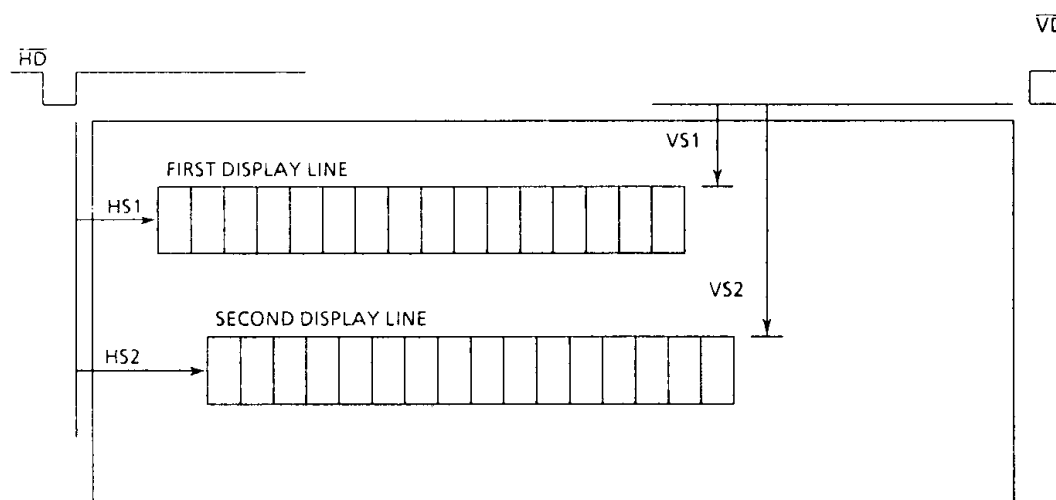


Figure 3-6. TV screen image

SYMBOL	CONTENTS
HS10~HS15	horizontal start position of the first display line $HS1 = ((32 \times HS15 + 16 \times HS14 + 8 \times HS13 + 4 \times HS12 + 2 \times HS11 + HS10) \times 4 + X) T_{OSC}$
VS10~VS15	vertical start position of the first display line $VS1 = (32 \times VS15 + 16 \times VS14 + 8 \times VS13 + 4 \times VS12 + 2 \times VS11 + VS10) \times 4T_{HD}$
HS20~HS25	horizontal start position of the second display line $HS2 = ((32 \times HS25 + 16 \times HS24 + 8 \times HS23 + 4 \times HS22 + 2 \times HS21 + HS20) \times 4 + X) T_{OSC}$
VS20~VS25	vertical start position of the second display line $VS2 = (32 \times VS25 + 16 \times VS24 + 8 \times VS23 + 4 \times VS22 + 2 \times VS21 + VS20) \times 4T_{HD}$

Note. X: X is 17 when small character.
 X is 34 when large character.

Table 3-6. Display start position

- * The vertical display positions of lines 1 and 2 can be specified independently but, to prevent overlapping of the two lines on the display, the value for the vertical display position of line 2 must satisfy $(VS2 > VS1 + CS11 \times 16T_{HD} + CS10 \times 32T_{HD})$.

3.2.4 Y/BL signal

The Y signal (the logical or output of the R, G and B signals) makes the display clearer by deleting the background only where characters are displayed. The BL signal deletes the entire background for one character (8 × 8 dots) and is output for all data except that at address 2FH in the character ROM.

The Y/BL pin is used for both Y signal and BL signal output. Which of the two signals is to be output is determined by the upper 2 bits of OP0A. The dotted lines in Figure 3-7 show the Y/BL signal output being scanned.

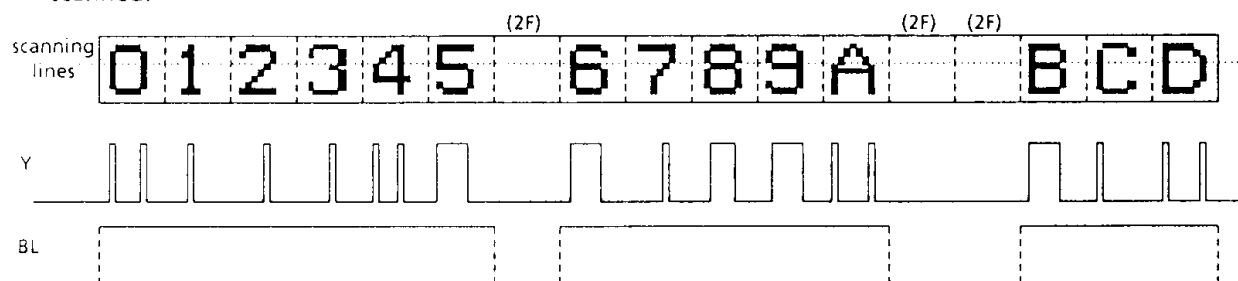


Figure 3-7. Example of Y and BL signal output

3.2.5 Control of OSD outputs buffer

The OSD outputs for Y,BL and RGB use tri – state output buffers for which the respective polarities can be inverted. Polarity is controlled by DRC41 and tri – state is controlled by DRC51.

Bit 3 of DRC41 is used for controlling the smoothing function.

register	bit	symbol	output name	data "0"	data "1"
DRC41	3	ESMZ	—	smoothing OFF	smoothing ON
	2	BLIV	BL	active High	active Low
	1	YIV	Y	active High	active Low
	0	RGBIV	RGB	active High	active Low
DRC51	3	EBF3	Y / BL	output buffer OFF	output buffer ON
	2	EBF2	B	output buffer OFF	output buffer ON
	1	EBF1	G	output buffer OFF	output buffer ON
	0	EBF0	R	output buffer OFF	output buffer ON

Figure 3-7. Control of OSD output

3.2.6 RA Port Function

R signal output and G signal output ports are also used as I/O ports. When not used for color signals, use is possible as normal I/O ports. RA port and Y/BL selection is performed by OP0A.

Also, the upper 2 bits of IP0A are used to input the OSD display status.

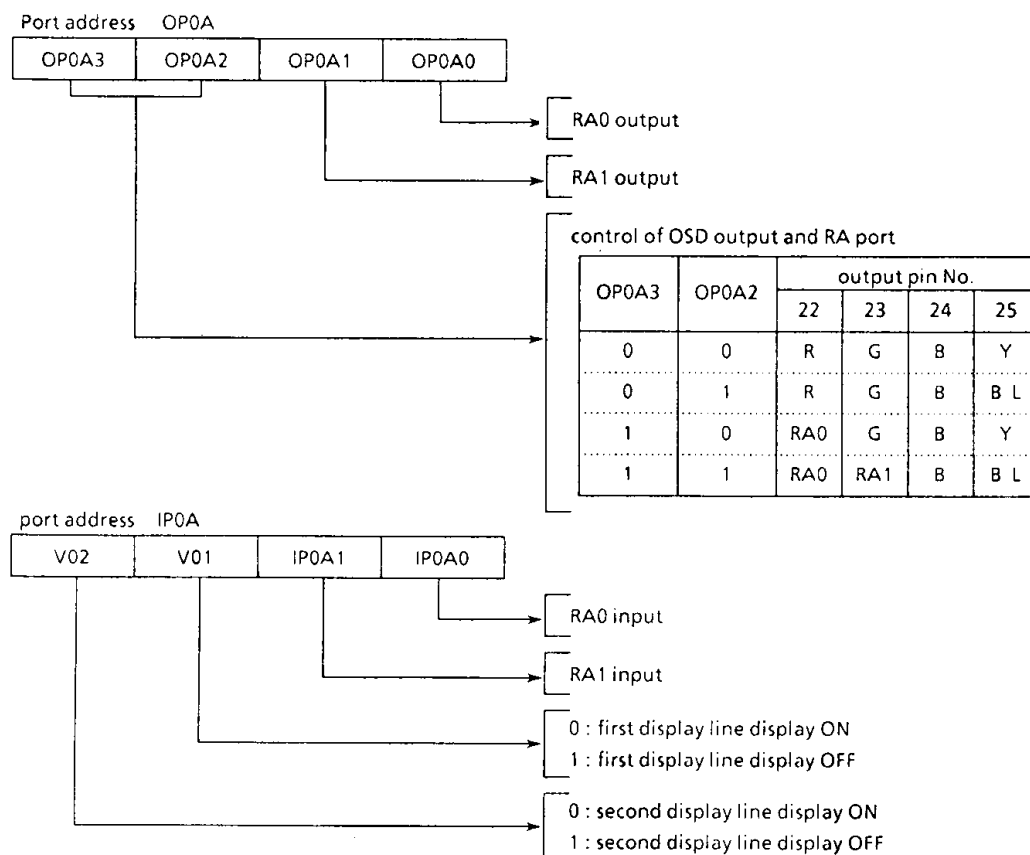


Figure 3-8. Port RA

3.2.7 Character ROM (Standard characters)

Figure 3-9 shows the standard pattern characters and symbols available as character data. Character patterns can also be set by the user. For details, refer to the section on piggyback chip 47C034.

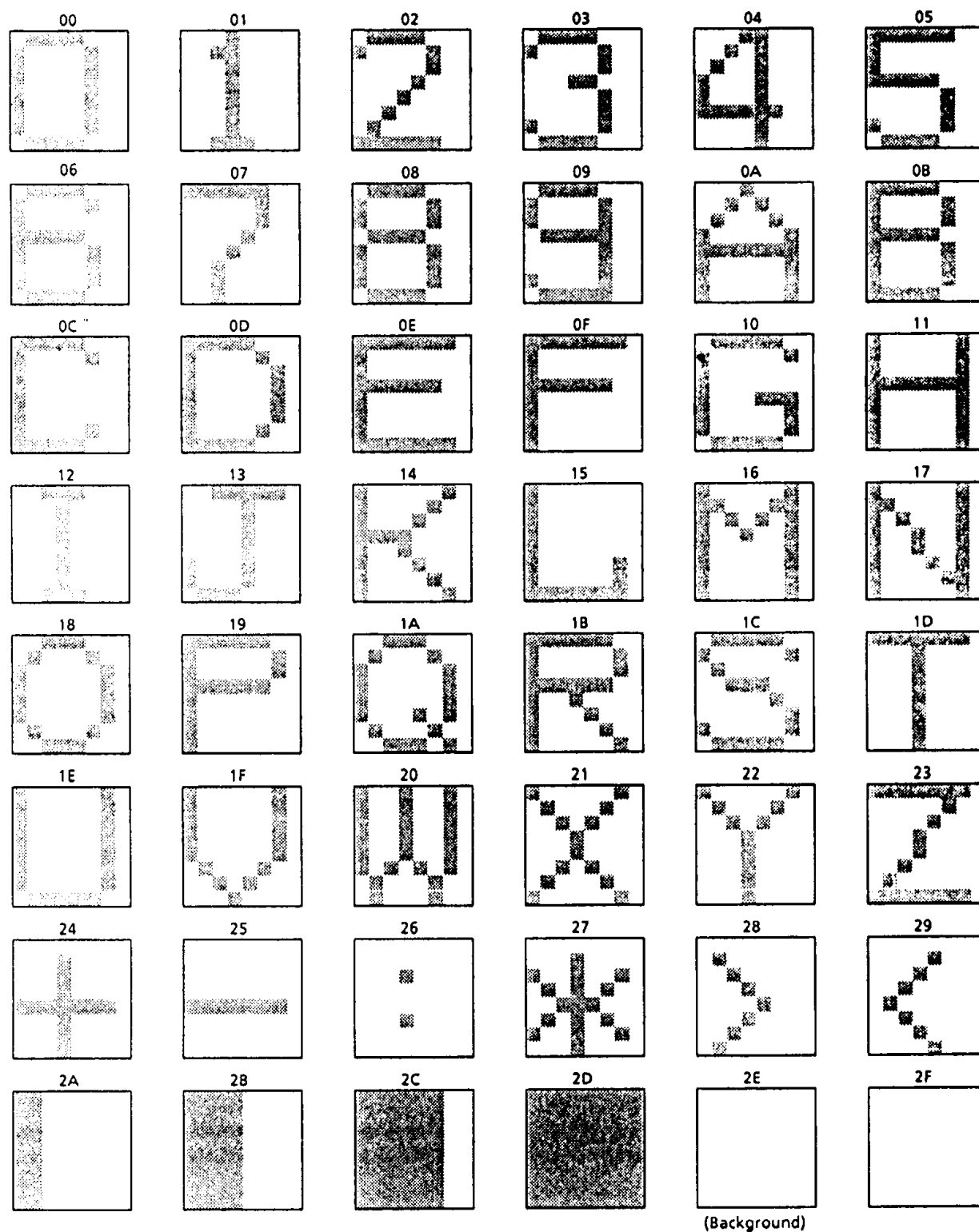


Figure 3-9. Character ROM address and character pattern

3.3 3-bit A/D converter (Comparator) input

Comparator input consists of a comparator and a 3-bit D/A converter. AFC input voltage can be detected in 8 steps by sensing bit 0 of IP07 while changing the reference voltage (D/A converter output voltage) with the command register (OP12).

R70 pin is also used for comparator input. Bit 3 is used to set R70 pin for ordinary digital input.

The comparator is disabled and bit 3 is set to "0" during reset. The latch should be set to "1" when R70 pin is used for comparator input and digital input.

3.3.1 Circuit Configuration

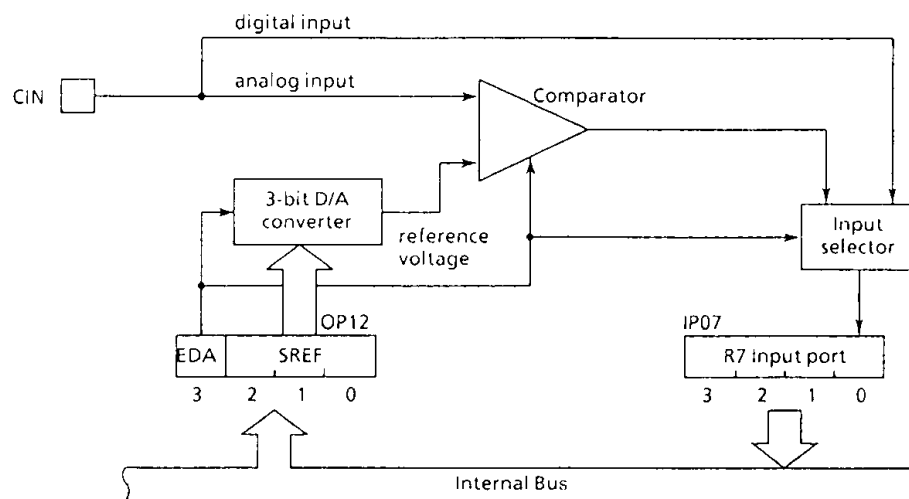


Figure 3-10. Comparator input circuit

3.3.2 Control of Comparator Input

The reference voltage of the comparator is set using the lower 3 bits of the command register. Table 3-8 shows the reference voltage when $V_{DD} = 5V$.

Comparator input control command register (Port address OP12)

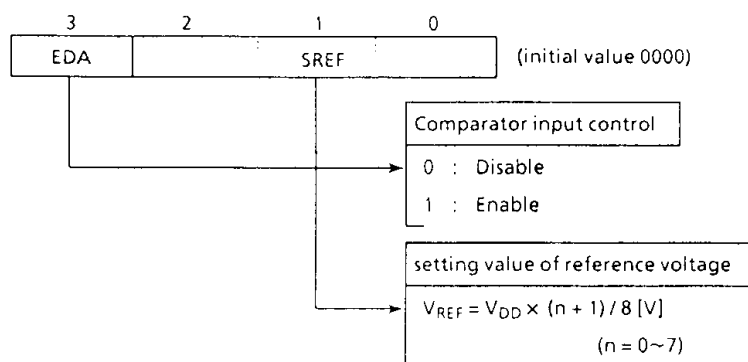


Figure 3-11. Control Command Register

OP12			reference voltage [V]
2	1	0	
0	0	0	0.62
0	0	1	1.25
0	1	0	1.87
0	1	1	2.50
1	0	0	3.12
1	0	1	3.75
1	1	0	4.37
1	1	1	5.00

Table 3-8. Reference Voltage

3.4 D / A converter (PWM) output

The 47C434/634 have five channels built-in D/A converter (Pulse width Modulation) outputs. $\overline{\text{PWM}}$ output can easily be obtained by connecting an external low pass filter.

$\overline{\text{PWM}}$ outputs data are multiplex to the R4 port and R50 pin. When the R4 ($\overline{\text{PWM}}$) port and R50 pin are used for $\overline{\text{PWM}}$ output, the corresponding bits of R4, R50 output latch should be set to "1". The R4, R5 output latch is initialized to "1" during reset.

$\overline{\text{PWM}}$ output is controlled by the buffer selector (OP17) and the data transfer buffer (OP18). PWM data written to the data transfer buffer can be sent to the PWM data latch by writing "CH" to the buffer selector, and $\overline{\text{PWM}}$ output. PWM output. PWM data transferred to the PWM data latch remain intact until overwritten. Resetting and holding clear the buffer selector, data transfer buffer and PWM data latch to "0" ($\overline{\text{PWM}}$ output is "H" level).

3.4.1 Configuration of Pulse Width Modulation circuit

Configuration of pulse width modulation circuit shown in Figure 3-13.

3.4.2 Output waveform of PWM circuit

(1) $\overline{\text{PWM0}}$ output

$\overline{\text{PWM0}}$ is a PWM output controlled by 14 bits data. The basic period of the $\overline{\text{PWM0}}$ is $T_M = 2^{15} / f_c$.

The higher 8 bits of 14 bits data are used to control the pulse width of the pulse output with the period of $T_S = T_M / 64$, which is the sub - period of the $\overline{\text{PWM0}}$. When the 8 bits data are decimal n ($0 \leq n \leq 255$), this pulse width becomes $n \times t_0$, where $t_0 = 2 / f_c$.

The lower 6 bits of 14 bits data are used to control the generation of an additional t_0 wide pulse in each T_S period. When the 6 bits data are decimal m ($0 \leq m \leq 63$), the additional pulse is generated in each of m periods out of 64 periods contained in a T_M period. The relationship between the 6 bits data and the position of T_S period where the additional pulse is generated is shown in Table 3-9.

(2) $\overline{\text{PWM1}}$ - $\overline{\text{PWM4}}$ output

Each of $\overline{\text{PWM1}}$ to $\overline{\text{PWM4}}$ is a PWM output controlled by 6 bits data. The period of them is $T_M = 2^7 / f_c$. When the 6 bits data are decimal k ($0 < k < 63$), the pulse width becomes $k \times t_0$. The waveform is also illustrated in Figure 3-12.

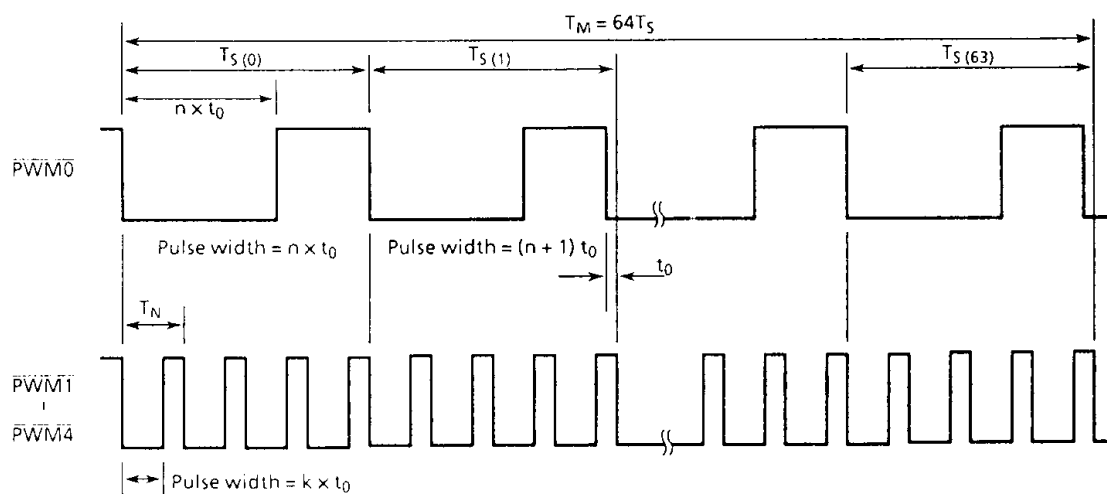


Figure 3-12. $\overline{\text{PWM}}$ Output Waveform (It is shown to the additional pulse $T_{S(1)}$ and $T_{S(63)}$ of the $\overline{\text{PWM0}}$)

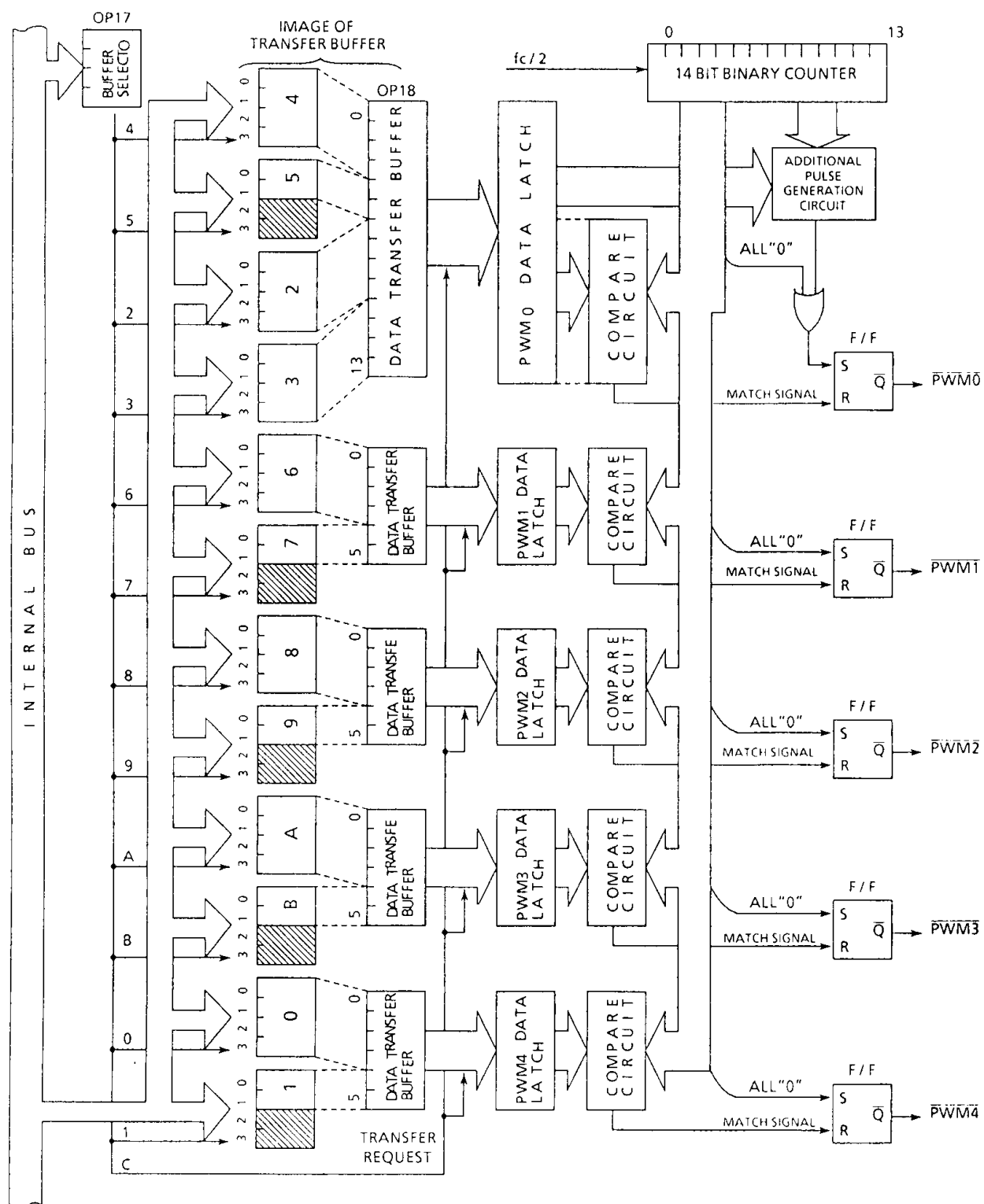


Figure 3-13. Pulse Width Modulation Circuit

Bit position of 6 bits data	Relative position of T_S where the output pulse is generated (No. i of $T_{S(i)}$ is listed)
bit0	32
bit1	16, 48
bit2	8, 24, 40, 56
bit3	4, 12, 20, 28, 36, 44, 52, 60
bit4	2, 6, 10, 14, 18, 22, 26, 30, ..., 58, 62
bit5	1, 3, 5, 7, 9, 11, 13, 15, 17, ..., 59, 61, 63

Note . When the corresponding bit is "1", it is output.

Table 3-9. Correspondence between 6 bits data and the additional pulse generated T_S periods

3.4.3 Control of PWM circuit (Data transfer)

\overline{PWM} output is controlled by writing output data to a data transfer buffer (OP18). For writing, the output data are divided using the buffer selector (OP17). Buffer numbers are assigned to the data transfer buffers for these divided data, after which the data are written as shown in Table 3-10.

- ① The number of the transfer buffer to which the data are to be written is written to the buffer selector (OP17).
- ② The corresponding PWM data are written to the selected buffer (OP18).
- ③ Operations ① and ② are repeated, continuously writing data to the transfer buffer.
- ④ When all of the output data have been written. " C_H " is written to the buffer selector.

While the output data are being written to the transfer buffer, the previously written data are being output. For $\overline{PWM0}$ output, switching to \overline{PWM} output occurs at a maximum of $2^{15}/f_c$ [sec] (at 4MHz, 8192fs) after " C_H " is written to the buffer selector. For $\overline{PWM1}$ through $\overline{PWM4}$ output data switching, this requires $2^9/f_c$ [sec] (at 4MHz, 128 μ s).

Buffer Number (OP17)	Correspondence to bit (OP18)	Mode	PWM Output
0	Bit of PWM4 transfer buffer 3 ~ 0	Write	Preceding data
1	Bit of PWM4 transfer buffer 5 ~ 4	Write	Preceding data
2	Bit of PWM0 transfer buffer 9 ~ 6	Write	Preceding data
3	Bit of PWM0 transfer buffer 13 ~ 10	Write	Preceding data
4	Bit of PWM0 transfer buffer 3 ~ 0	Write	Preceding data
5	Bit of PWM0 transfer buffer 5 ~ 4	Write	Preceding data
6	Bit of PWM1 transfer buffer 3 ~ 0	Write	Preceding data
7	Bit of PWM1 transfer buffer 5 ~ 4	Write	Preceding data
8	Bit of PWM2 transfer buffer 3 ~ 0	Write	Preceding data
9	Bit of PWM2 transfer buffer 5 ~ 4	Write	Preceding data
A	Bit of PWM3 transfer buffer 3 ~ 0	Write	Preceding data
B	Bit of PWM3 transfer buffer 5 ~ 4	Write	Preceding data
C	None	Transfer	Present data

Table 3-10. The bit and Buffer number of data transfer Buffer

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0V)

PARAMETER	SYMBOL	PINS	RATING	UNIT
Supply Voltage	V _{DD}		- 0.3 to 7	V
Input Voltage	V _{IN}		- 0.3 to V _{DD} + 0.3	V
Output Voltage	V _{OUT1}	Except sink open drain pin	- 0.3 to V _{DD} + 0.3	V
	V _{OUT2}	Sink open drain pin except R7 port	- 0.3 to 10	
Output Current (Per 1 pin)	I _{OUT1}	R6 port	30	mA
	I _{OUT2}	R7, R8, R9 port	3.2	
Output Current (Total)	Σ I _{OUT1}	R6 port	60	mA
Power Dissipation	PD		600	mW
Soldering Temperature (time)	T _{sld}		260 (10sec)	°C
Storage Temperature	T _{stg}		- 55 to 125	°C
Operating Temperature	T _{opr}		- 30 to 70	°C

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V, T_{opr} = - 30 to 70°C)

PARAMETER	SYMBOL	PINS	CONDITION	Min.	Max.	UNIT
Supply Voltage	V _{DD}		in the Normal mode	4.5	6.0	V
			in the HOLD mode	2.0		
Input High Voltage	V _{IH1}	Except Hysteresis Input	V _{DD} ≥ 4.5V	V _{DD} × 0.7	V _{DD}	V
	V _{IH2}	Hysteresis Input		V _{DD} × 0.75		
	V _{IH3}		V _{DD} < 4.5V	V _{DD} × 0.9		
Input Low Voltage	V _{IL1}	Except Hysteresis Input	V _{DD} ≥ 4.5V	0	V _{DD} × 0.3	V
	V _{IL2}	Hysteresis Input			V _{DD} × 0.25	
	V _{IL3}		V _{DD} < 4.5V		V _{DD} × 0.1	
Clock Frequency	f _c			0.4	4.2	MHz
	f _{OSD}			-	6.0	

Note. Input Voltage V_{IH3}, V_{IL3}: in the HOLD mode.

D.C. CHARACTERISTICS

(V_{SS} = 0V, T_{opr} = -30 to 70°C)

PARAMETER	SYMBOL	PINS	CONDITION	Min.	Typ.	Max.	UNIT
Hysteresis Voltage	V _{HS}	Hysteresis Input		—	0.7	—	V
Input Current	I _{IN1}	K0 port, TEST, RESET, HOLD	V _{DD} = 5.5V, V _{IN} = 5.5V / 0V	—	—	±2	μA
	I _{IN2}	R port (open drain)					
Input Low Current	I _{IL}	R port (push-pull)	V _{DD} = 5.5V, V _{IN} = 0.4V	—	—	-2	mA
Input Resistance	R _{IN1}	K0 port with pull-up/pull-down		30	70	150	KΩ
	R _{IN2}	RESET		100	220	450	
Output leakage Current	I _{LO}	Tri-state R6, R8, R9 port (open drain)	V _{DD} = 5.5V, V _{OUT} = 5.5V	—	—	±2	μA
Output High Voltage	V _{OH1}	R port (push-pull)	V _{DD} = 4.5V, I _{OH} = -200μA	2.4	—	—	V
	V _{OH2}	R port (tri-state)	V _{DD} = 4.5V, I _{OH} = -0.7mA	4.1	—	—	
Output Low Voltage	V _{OL1}	R7, R8, R9 port	V _{DD} = 4.5V, I _{OL} = 1.6mA	—	—	0.4	V
	V _{OL2}	R port (tri-state)	V _{DD} = 4.5V, I _{OL} = 0.7mA				
Output Low Current	I _{OL}	R6 port	V _{DD} = 4.5V, V _{OL} = 1.0V	—	20	—	mA
Supply Current (in the Normal mode)	I _{DD}		V _{DD} = 5.5V, f _c = 4MHz	—	3	6	mA
Supply Current (in the HOLD mode)	I _{DDH}		V _{DD} = 5.5V	—	0.5	10	μA

Note 1. Typ. values show those at T_{opr} = 25°C, V_{DD} = 5V.

Note 2. Input Current I_{IN1} : The current through resistor is not included, when the pull-up / pull-down resistor is contained.

Note 3. Supply Current : V_{IN} = 5.3 V / 0.2 V
 The K0 port is open when the pull-up / pull-down resistor is contained.
 The voltage applied to the R port is within the valid range V_{IL} or V_{IH}.

A / D CONVERTER CHARACTERISTICS

PARAMETER	SYMBOL	PINS	CONDITION	Min.	Typ.	Max.	UNIT
Analog input voltage	V _{AIN}	CIN		V _{SS}	—	V _{DD}	V
A / D conversion error	—			—	—	± $\frac{1}{4}$	LSB

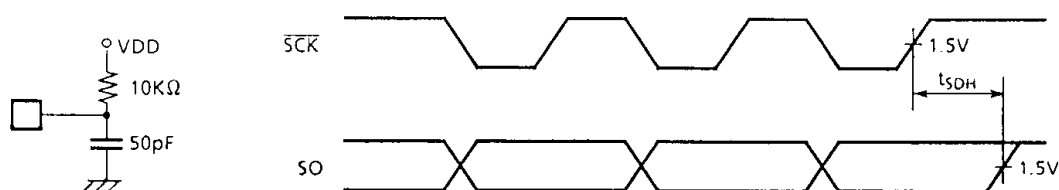
A.C. CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = 4.5 to 6.0V, T_{opr} = -30 to 70°C)

PARAMETER	SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT
Instruction Cycle Time	t _{cy}		1.9	-	20	μs
High level Clock Pulse Width	t _{WCH}	For external clock operation	80	-	-	ns
Low level Clock Pulse Width	t _{WCL}					
Shift data Hold Time	t _{SDH}		0.5t _{cy} - 300	-	-	ns

*Note. Shift data Hold Time*External circuit for \overline{SCK} pin and SO pin.

Serial port (Completion of transmission)



RECOMMENDED OSCILLATING CONDITIONS

(V_{SS} = 0V, V_{DD} = 4.5 to 6.0V, T_{opr} = -30 to 70°C)

(1) 4MHz

Ceramic Resonator

CSA4.00MG

(MURATA)

C_{XIN} = C_{XOUT} = 30pF

KBR-4.00MS

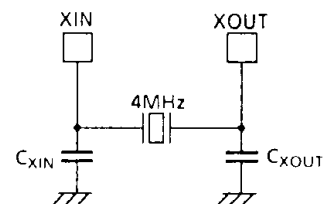
(KYOCERA)

C_{XIN} = C_{XOUT} = 30pF

Crystal Oscillator

204B-6F 4.0000

(TOYOCOM)

C_{XIN} = C_{XOUT} = 20pF

(2) 400KHz

Ceramic Resonator

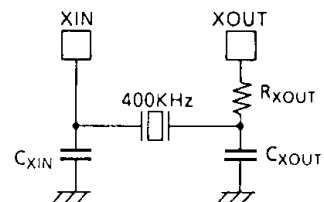
CSB400B

(MURATA)

C_{XIN} = C_{XOUT} = 220pF,

KBR-400B

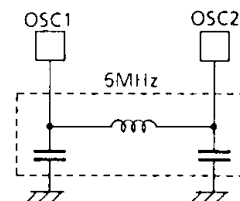
(KYOCERA)

R_{XOUT} = 6.8KΩC_{XIN} = C_{XOUT} = 100pF,R_{XOUT} = 10KΩ

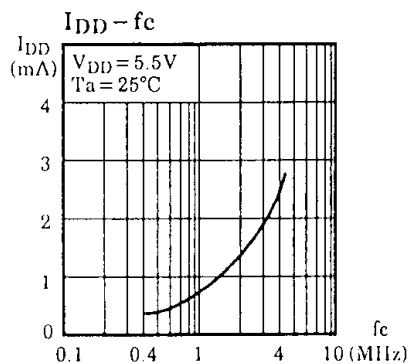
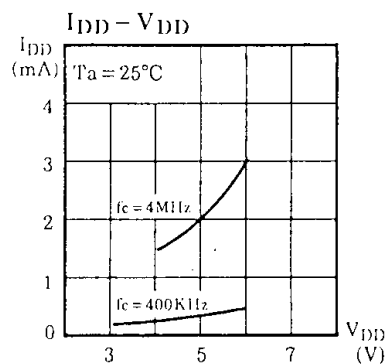
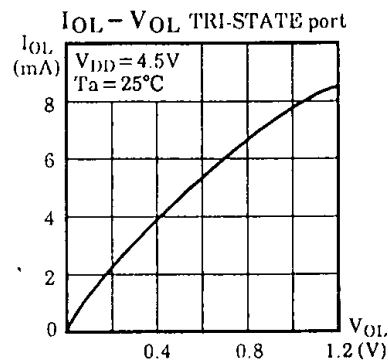
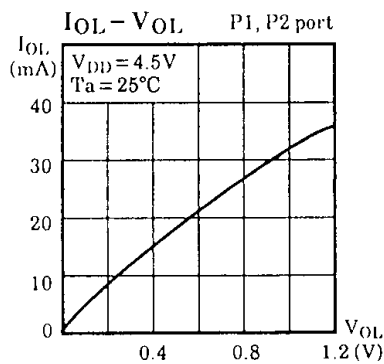
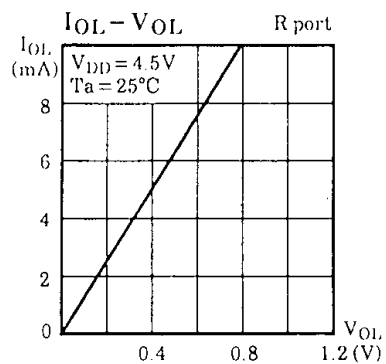
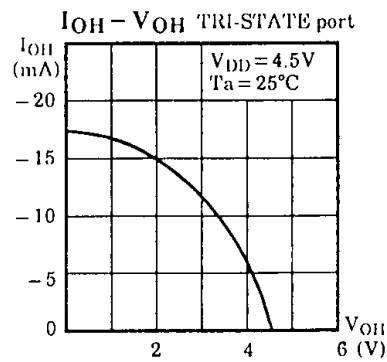
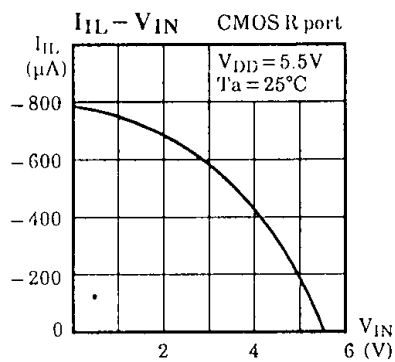
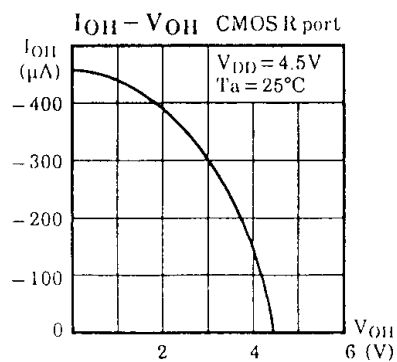
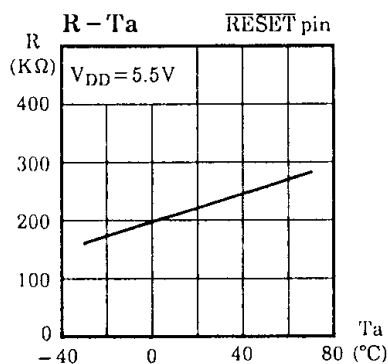
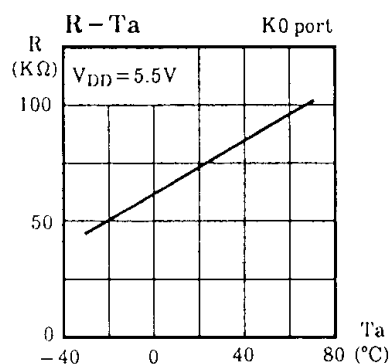
(3) 6MHz (for DOS)

LC Resonator

TBEKSE5-30361FBY (TOUKOU)



TYPICAL CHARACTERISTICS



INPUT/OUTPUT CIRCUITRY

(1) Control pins

Input/output circuitries of the 47C434/634 control pins are shown below.

CONTROL PIN	I/O	CIRCUITRY	REMARKS
XIN XOUT	Input Output		Resonator connecting pins $R = 1\text{K}\Omega$ (typ.) $R_f = 1.5\text{M}\Omega$ (typ.) $R_0 = 2\text{K}\Omega$ (typ.)
$\overline{\text{RESET}}$	Input		Hysteresis input Contained pull-up resistor $R_{IN} = 220\text{K}\Omega$ (typ.) $R = 1\text{K}\Omega$ (typ.)
$\overline{\text{HOLD}} (\overline{\text{KE0}})$	Input (Input)		Hysteresis input (Sense input) $R = 1\text{K}\Omega$ (typ.)
TEST	Input		Contained pull-down resistor $R_{IN} = 70\text{K}\Omega$ (typ.) $R = 1\text{K}\Omega$ (typ.)
OSC1 OSC2	Input Output		Oscillation terminals for DOS $R = 1\text{K}\Omega$ (typ.) $R_f = 1.5\text{M}\Omega$ (typ.) $R_0 = 2\text{K}\Omega$ (typ.)
$\overline{\text{HD}}$ $\overline{\text{VD}}$	Input		Synchronous signal input Hysteresis input $R = 1\text{K}\Omega$ (typ.)

(2) I/O ports

The input/output circuitries of the 47C434/634 I/O ports are shown below, any one of the circuitries (PB, PC, PF, PU) can be chosen by a code as a mask option.

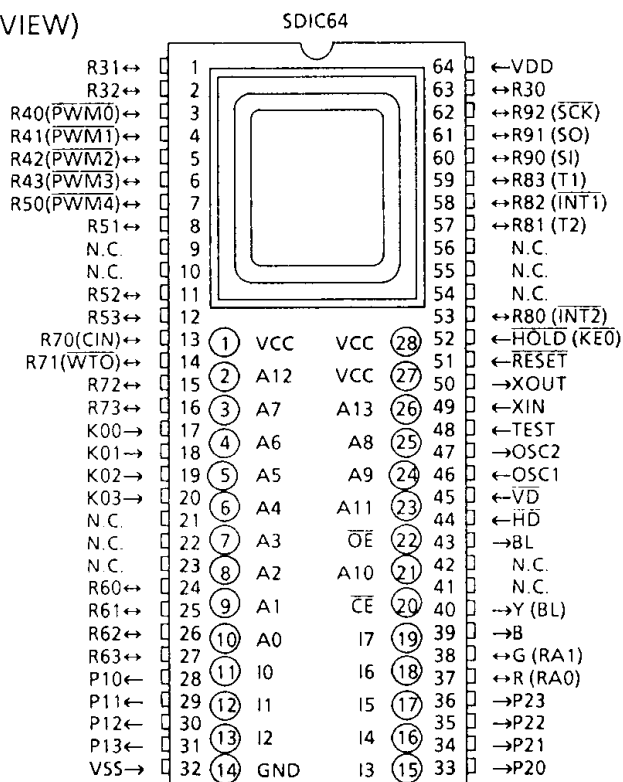
PORT	I/O	INPUT/OUTPUT CIRCUITRY and CODE		REMARKS
K0	Input	PB	PC, PF, PU	Pull-up or pull-down resistor $R_{IN} = 70K\Omega$ (typ.) $R = 1K\Omega$ (typ.)
R4 R50	I/O	PB, PC	PF, PU	Tri-state or Sink open drain Initial "Hi-Z" $R = 1K\Omega$ (typ.)
R51 R52 R53	I/O			Tri-state Initial "Hi-Z" $R = 1K\Omega$ (typ.)
R6 R8 R9	I/O	R6	R8, R9	Sink open drain Initial "Hi-Z" Hysteresis input (R8, R9) $R = 1K\Omega$ (typ.)
R7	I/O	R70 Initial "Hi-Z"	R71~R73 Initial "High"	Sink open drain and push-pull Comparator input (R70 pin) $R = 1K\Omega$ (typ.)
R (RA0) G (RA1)	I/O	PB, PC, PF	PU	Tri-state Initial "Hi-Z" $R = 1K\Omega$ (typ.)
B Y (BL)	Output			R, G : Side a B, Y : Side b

CMOS 4-BIT MICROCONTROLLER

TMP47C034E

The 47C034, which is equipped with an EPROM as program memory, is a piggyback type evaluator chip used for development and operational confirmation of the 47C434/634 application systems (programs). Conversion adapter socket BM1105 can be used to convert the 64-pin package of the 47C034 for pin compatibility with the 42-pin mask ROM 47C434/634. Conversion adapter socket BM1106 can be used to convert from 64 pins for pin compatibility with the 54-pin 47C635.

PIN ASSIGNMENT (TOP VIEW)



PIN FUNCTION (Top of the package)

PIN NAME	Input / Output	FUNCTIONS
A13 - A0	Output	Program memory address output
I7 - I0	Input	Program memory data input
\overline{CE}	Output	Chip enable signal output
\overline{OE}		Output enable signal output
VCC	Power supply	+ 5V (connected with VDD)
GND		0V (connected with VSS)

A.C. CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Address Delay Time	t_{AD}	$V_{SS} = 0V, V_{DD} = 4.5 \text{ to } 6.0V$	—	—	150	ns
Data Setup Time	t_{IS}	$C_L = 100pF$	150	—	—	ns
Data Hold Time	t_{IH}	$T_{opr} = -40 \text{ to } 70^\circ C$	50	—	—	ns

NOTES FOR USE

(1) Program memory

Figure 1 shows the program storage area. The 47C034 has a data table at addresses 2000-217F_H (48 characters × 16 bits) for on-screen display data so that characters and symbols can be displayed on TV screens. Thus, a 64k EPROM is not used.

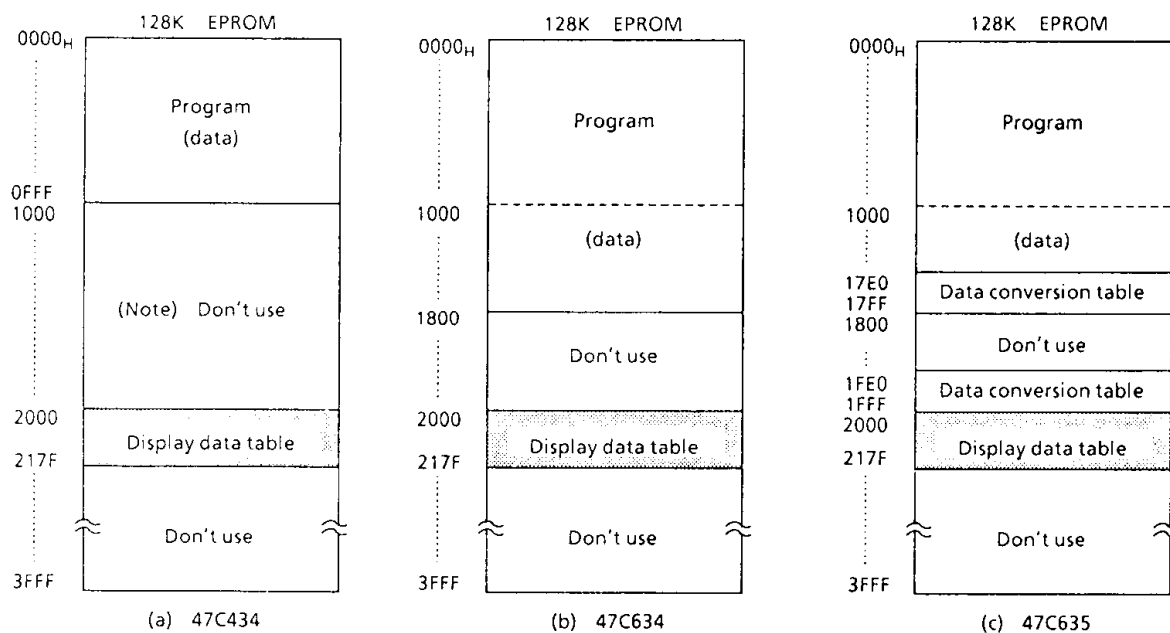
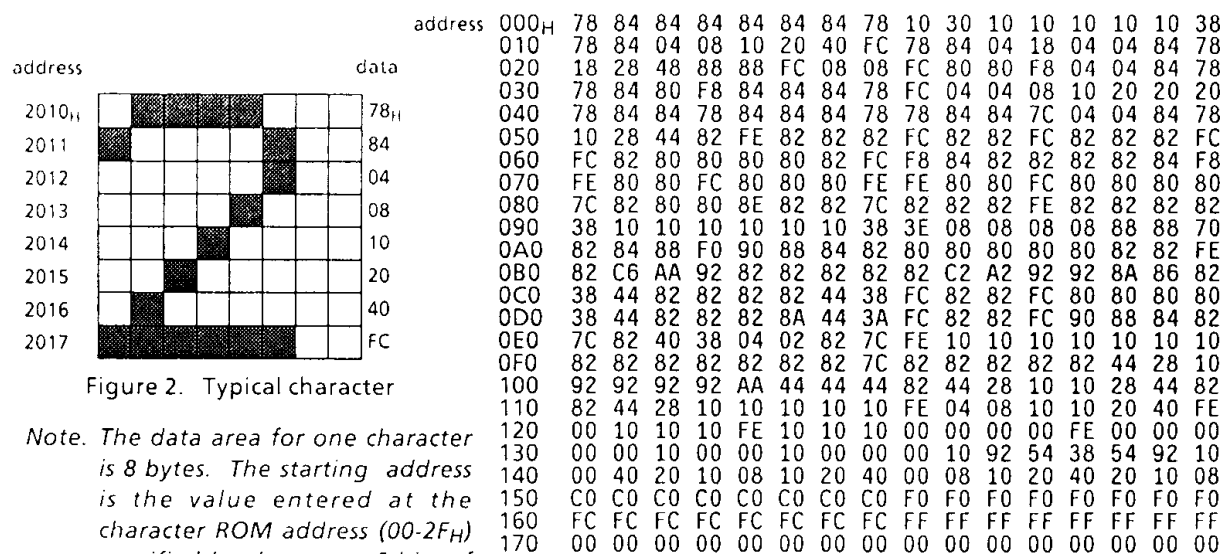


Figure 1. Program area

Note. When using the 47C034 to check 47C635 operation, place data conversion tables at two locations. With the 47C434, permanent data are placed at addresses 0000-0FFF_H but, when the 47C034 is used, it is necessary to put the same data that is at addresses 0000-0FFF_H at 1000_H and following addresses. Also, with the 47C634 and 47C635, the permanent data at addresses 1000-17FF_H are read out when the permanent data at addresses 1800-1FFF_H are accessed.

(2) Data table for on-screen display (OSD)

With the 47C034, an OSD display character ROM is generated inside the EPROM used. The characters configured using the data loaded to EPROM addresses 2000-217F_H are display on the TV screen, therefore, characters can be freely set by the user. When a program is being submitted, write the character data to 2000_H and the following addresses. Figure 1-2 shows typical character (8 × 8 bits) addresses and data. Figure 1-3 shows a list of standard patterns in hexadecimal.



Note. The data area for one character is 8 bytes. The starting address is the value entered at the character ROM address (00-2F_H) specified by the upper 6 bits of the 9-bit program area (000-17F_H).

Figure 3. Standard character data (from address 2000_H)

(3) Input/output ports

The input/output circuit for the 47C034 input/output ports is the same as that of the 47C434/634 and 47C635 (code : PC), except that a pulldown resistor is not built into the K0 port.

When using as code PB or PC evaluators, it is necessary to connect an external resistor.

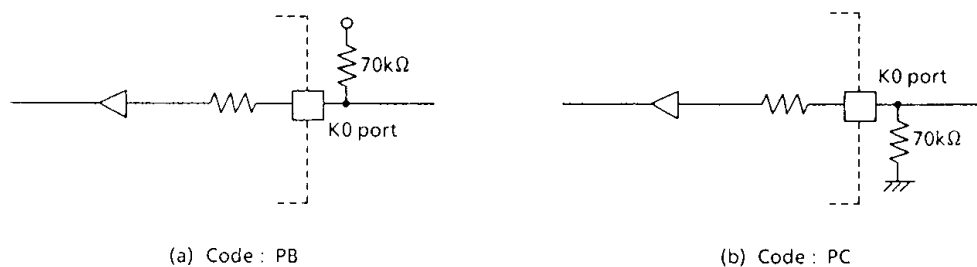


Figure 4. I/O code and external circuitry

Note. The 47C434/634 do not have built-in P1, P2 and R3 ports. Also, the 47C034 pins R40-R43 and R50 form a tristate output buffer; therefore, caution is required when using as the 47C434/634 code PF.