Data Sheet
July 2003

CB64-Type 10 Gb/s Transponder with 16-Ch. 622 Mb/s MUX/DeMUX and Selectable FEC Rate

Features

- Supports standard OC-192/STM-64 data rate of 9.9532 Gb/s, selectable FEC rate of 10.6642 Gb/s or 10.709 Gb/s, and the Ethernet rate of 10.3125 Gb/s
- Cooled 1.5 µm EML laser transmitter and PIN receiver
- Available with optional internal reference clock clean-up circuit for improved jitter performance
- Differential LVDS data interface
- Automatic transmitter optical power control
- Laser bias monitor output
- Optical transmitter enable input
- Laser degrade alarms
- Laser back-facet monitor output
- Laser temperature monitor/alarm output
- Receiver loss of power (LOP) analog output
- Transponder alarm interrupt
- Loss-of-lock (LOL) alarm
- Selectable MUX reference input clock: 155.52 MHz or 622.08 MHz (scaled when operating at the FEC rate)
- Supports contraclocking mode of operation as well as forward-forward clocking mode
- Provides 10 Gb/s electrical system diagnostics loopback (scaled when operating at the FEC rate)
- Operating case temperature range: 0 °C to 65 °C[1]
- Compact size: 4 in. x 3.5 in. x 0.53 in.
- Fully compatible with 300-pin,10 Gb/s transponder MSA
- Pigtailed low-profile package with choice of industry-standard connectors

Applications

- Telecommunications:
  — Optical networking
  — Inter- and intraoffice SONET/SDH
  — Metropolitan area networks
  — Subscriber loop
- High-speed data communications

Description

The CB64-type transponder is a bidirectional module designed to provide a SONET or SDH compliant electro-optical interface between the SONET/SDH photonic physical layer and the electrical section layer. The module contains a 10 Gb/s optical transmitter and a 10 Gb/s optical receiver in the same physical package along with the electronics necessary to multiplex and demultiplex sixteen 622 Mb/s electrical channels.

1. Note that this device meets NEBS GR63 requirements of operation at 70 °C for 14 days (max) per year, or 96 hours of continuous operation.

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Conventions

All signals referenced in *italics* are for future use.

Description (continued)

Clock synthesis and clock recovery circuits are also included within the module. The module also supports 10 GbE Ethernet rate of 10.3 Gb/s and FEC rate of 10.6642 Gb/s or 10.709 Gb/s and all input and output clock and data rates are scaled appropriately when operating at the FEC rate. Figure 1 shows a simplified block diagram of the CB64-type transponder.

In the transmitting direction, the transceiver module multiplexes sixteen 622.08 Mb/s differential LVDS compatible electrical data signals into an optical signal at 9.95328 Gb/s for launching into optical fiber. The optical transmitter is available with a cooled, fieldproven 1.55 µm EML laser for up to 40 km, intermediate reach (IR-2) applications. An optional internal reference clock clean-up circuit within CB64-type provides improved jitter performance. The optical output signal is SONET and ITU compliant for OC-192/STM-64 applications as shown in Table 10 on page 26.

In the receiving direction, the transceiver module receives a 9.95328 Gb/s optical signal and converts it to an electrical signal, extracts a clock signal, then demultiplexes the data into sixteen 622 Mb/s differential LVDS compatible data signals. The receiver operates over the wavelength range of 1.1 µm to 1.6 µm, and is fully compliant to SONET/SDH OC-192/STM-64 physical layer specifications as shown in Table 11 on page 26.

Note that all signals referenced in *italics* in this document are for future use.

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect reliability.

Table 1. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Operating Case Temperature Range	T_C	0	65[1]	°C
Storage Case Temperature Range	T_S	–40	85	°C
–5.2 V Supply Voltage	V_{EE}	0.5	–5.5	V
3.3 V Supply Voltage	V_{DD}	–0.5	3.6	V
5.0 V Supply Voltage	V_{CC}	–0.5	5.5	V
Voltage on Any LVDS Pin	—	0	V_{CC}	—
High-speed LVDS Output Source Current	—	—	50	mA
Static Discharge Voltage[2]	ESD	—	500	V
Relative Humidity (noncondensing)	RH	—	85	%
Receiver Maximum Input Power PIN Diode	P_{IN}	—	8.0	dBm
Minimum Fiber Bend Radius	—	1.25 (31.8)	—	in. (mm)

1. Note that this device meets NEBS GR63 requirements of operation at 70 °C for 14 days (Max) per year, or 96 hours of continuous operation.
2. Human-body target model is 500 V.

Block Diagram

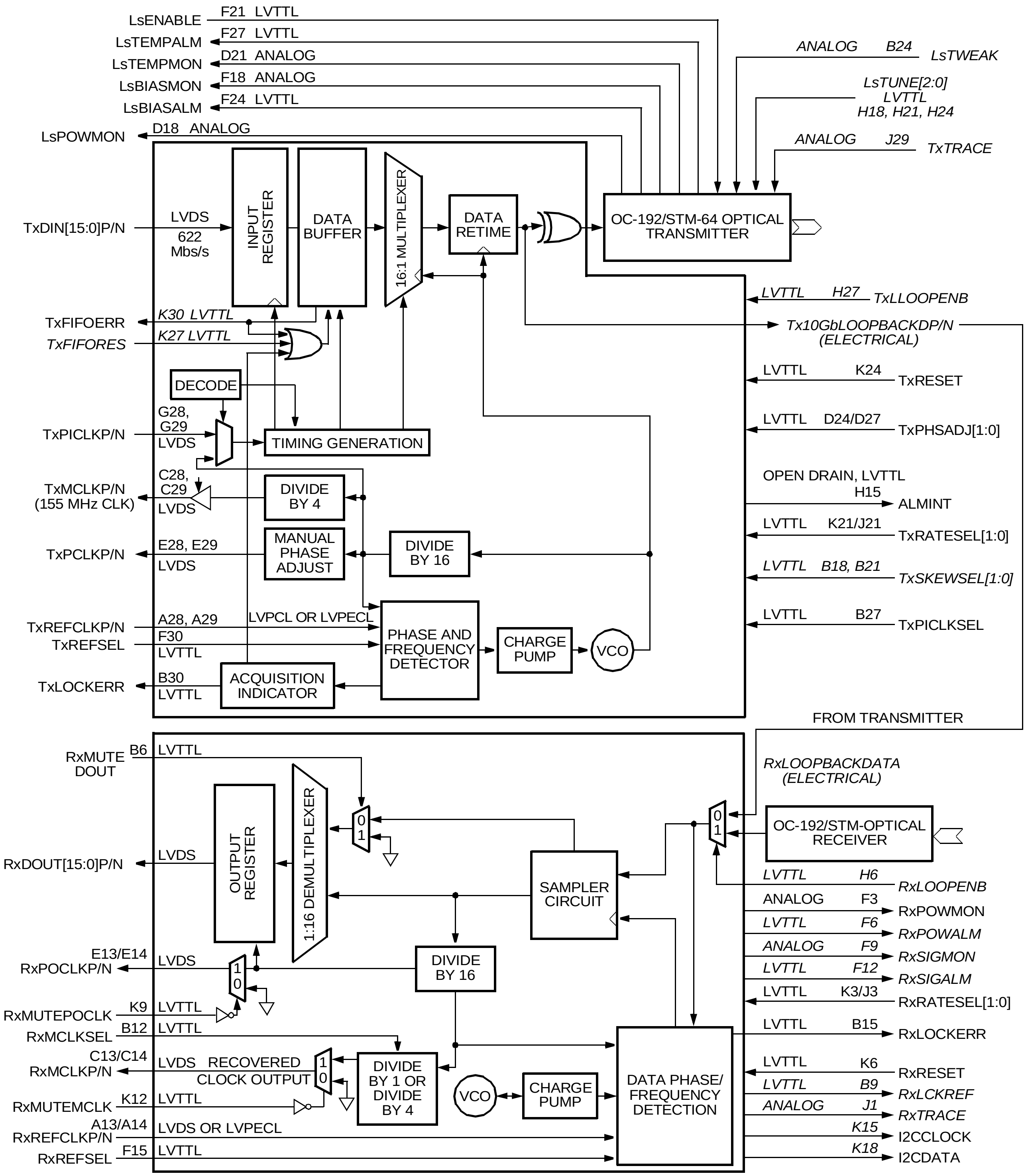

Figure 1. CB64-Type Transponder Block Diagram

1-1280(F).a

Pin Information

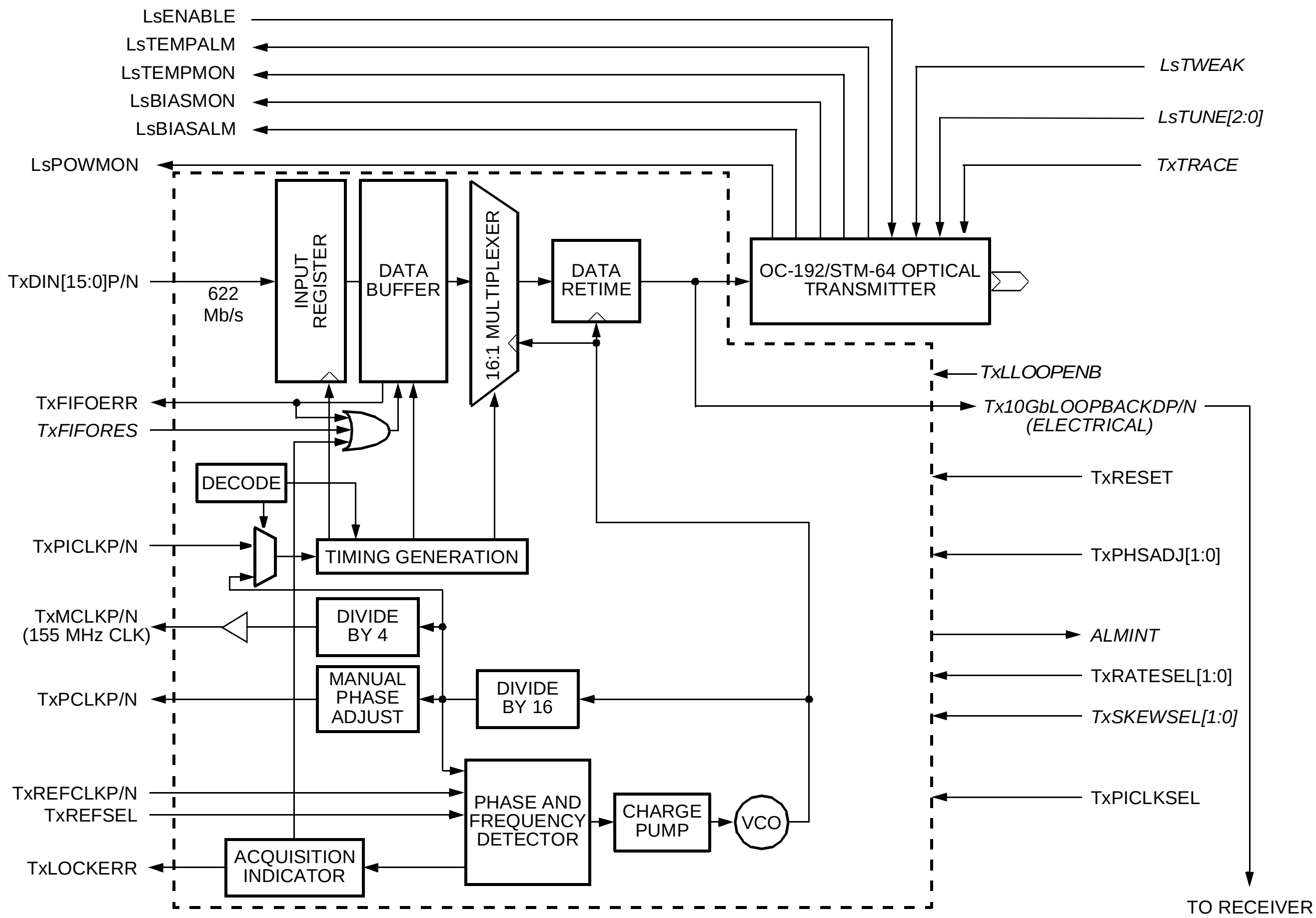

Figure 2. Transmitter Block Diagram

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Transmitter Input/Output Pin Descriptions

Table 2. CB64-Type Transponder, Transmitter Input/Output Pin Descriptions

Pin Name	Pin Description
LsENABLE	**Laser Enable Input.** A logic low on this input pin enables the transmitter's laser. A logic high disables the laser so there is no optical output.
LsTEMPMON	**Laser Temperature Monitor (Analog).** Provides a measure of the laser's operating temperature. If the laser temperature reaches 25 °C, the output voltage will be approximately 2.5 V. The output voltage varies from 0 V to 3.1 V over the entire temperature range (from 0 °C to 85 °C), and a polynomial temperature value in terms of output voltage is given by the following equation: $y = 14.0x^2 – 89.4x + 156.2$ where y = temperature in °C and x = output voltage in volts. A simplified and more accurate equation using a limited range of 15 °C to 55 °C and 1.5 V to 3.0 V can also be used as indicated below: $y = –28.0x + 95$ where y = temperature in °C, and x = output voltage in volts.

Pin Information (continued)

Transmitter Input/Output Pin Descriptions (continued)

Table 2. CB64-Type Transponder, Transmitter Input/Output Pin Descriptions (continued)

Pin Name	Pin Description
LsTEMPALM	**Laser Temperature Alarm.** This alarm will go active-low when the temperature deviates ± 2.5 °C from beginning-of-life (BOL) temperature setpoint.
LsBIASMON	**Laser Bias Monitor Voltage (Analog) Slope.** Provides a measure of the laser's dc bias current as well as an indication of the health of the laser in the transmitter. This output power changes at the rate of 20 mV/mA of bias current to the laser. All of the monitoring voltage is defined with respect to GND.
LsBIASALM	**Laser Bias Alarm.** This alarm will go active-low when the bias current to the laser increases by 50% from its beginning-of-life (BOL) value.
LsPOWMON	**Normalized Laser Power Monitor Voltage (Analog).** Provides an indication of the optical output power level from the transmitter laser. LsPOWMON amplifier gain is normalized to 500 mV for the nominal transmitter optical output power. If the optical power decreases by 3 dB from the beginning of Life (BOL), this output will drop to approximately 250 mV. Back-facet monitor transfer function varies from module to module, and as long as the automatic power control loop is working, the laser output power remains constant. LsPOWMON is not an alarm signal but rather a performance monitoring feature. The user can measure the transmitter aging by summarizing the laser bias variation, temperature changes, and output power at the same time.
TxDIN[15:0]P/N	**16-bit Differential LVDS Parallel Data Input**. TxDIN15P/N is the most significant bit of the input word and is the first bit serialized. TxDIN0P/N is the least significant bit of the input word and is the last bit serialized. TxD[15:0]P/N is sampled on the rising edge of TxPICLK (when TxPICLKSEL = 0) or on the rising and falling edge of TxPICLK (when TxPICLKSEL = 1). Note that this data will scale appropriately when operating at the FEC rate. Internally biased and terminated.
TxFIFOERR	**Transmit FIFO Data Storage Overflow.** Indicates active-low when an overflow has occurred in the parallel data storage element. Operationally, when TxFIFOERR occurs, the transponder automatically re-centers the pointers in the parallel data storage element for fastest FIFO overrun recovery.
TxREFCLKP/N	**622.08 MHz or 155.52 MHz Input Reference Clock.** This input is used as the reference for the internal clock frequency synthesizer inside the MUX that generates the 9.9538 GHz bit-rate clock used to shift data out of the parallel-to-serial converter. Note that this clock frequency must scale appropriately when operating at the FEC rate. Internally ac coupled and biased.
TxREFSEL	**Transmitter Reference Select.** Used for selection of the TxREFCLK frequency. Logic 0 is for 155 MHz, logic 1 or no connection for 622 MHz.
TxPCLKP/N	**Transmitter Parallel Clock.** A 622.08 MHz differential output reference parallel clock. It is normally used to coordinate transfers between customer board logic and the MUX device. Note that this clock will scale appropriately when operating at the FEC rate.
TxPHASADJ[1:0]	**Transmitter Phase Adjust.** Adjusts phase of TxPCLKP/N clock in 90° steps.
TxLOCKERR	**Lock Detect/Phase Error (Active-Low).** It goes low when MUX PLL has not locked to the TxREFCLK.
TxMCLKP/N	**Transmitter 155 MHz Clock Output From the Clock Synthesizer of the MUX.** This output can be connected to the reference clock input of the deMUX chip, thereby eliminating the need for a separate RxREFCLK VCO on the customer board. Note that this clock will scale appropriately when operating at the FEC rate.

Pin Information (continued)

Transmitter Input/Output Pin Descriptions (continued)

Table 2. CB64-Type Transponder, Transmitter Input/Output Pin Descriptions (continued)

Pin Name	Pin Description
TxPICLKP/N	**Differential LVDS Compatible Parallel Input Clock.** A 622.08 MHz nominally 50% duty cycle input clock, to which TxDin[15:0]P/N is aligned. TxPICLK is used to transfer the data on the 16 TxDIN inputs into the holding register in the parallel-to-serial converter. Note that this clock will scale appropriately when operating at the FEC rate. Internally biased and terminated.
TxPICLKSEL	**TxPICLK Clock Select.** Used to select between the 622.08 MHz or 311.04 MHz dual-edge clock options of the TxPICLKP/N. Logic 0 is for 622.08 MHz and logic 1 is for 311.04 MHz.
TxRESET	**MUX Master Reset.** Reset input for the device. Reset must be held active-low for a minimum of 6.4 ns. During a reset, the true data outputs are in the low state and the barred data outputs are in the high state. For normal power sequencing on power-up, no reset is required.
ALMINT	**Alarm Interrupt (Active-Low).** Combined logic level (OR) output of *RxPOWALM, RxSIGALM,* RxLOCKERR, LsBIASALM, LsTEMPALM, and TxLOCKERR. The signal is an open drain-type LVTTL output. Some of these signals are defined in the following section.
TxRATESEL[1:0][1]	**Transmitter Rate Select, FEC Rate Select (Active-Low).** Selects the normal OC-192/STM-64 rate of 9.9532 GHz, 10 GbE Ethernet rate of 10.3 Gb/s or the FEC rate of 10.6642 GHz: x, 0 = FEC rate of 10.6642/10.709 Gb/s, selected with TxREFCLK x, 1 = OC-192/STM-64 rate of 9.9532 Gb/s or 10GbE rate of 10.312 Gb/s, selected with TxREFCLK where x is either 0 or 1. Note that all input and output clock and data rates are scaled appropriately when operating at the FEC rate.
LsTWEAK *LsTUNE[2:0]* *TxFIFORES* *TxLLOOPENB* *TxTRACE*	*Pins reserved by MSA. Functions not implemented.*

1. TxRATESEL[1] is not internally connected. TxRATESEL[0] selects between normal OC-192 rate and FEC rate. 10 GbE can be used with either setting of TxRATESEL[0].

Pin Information (continued)

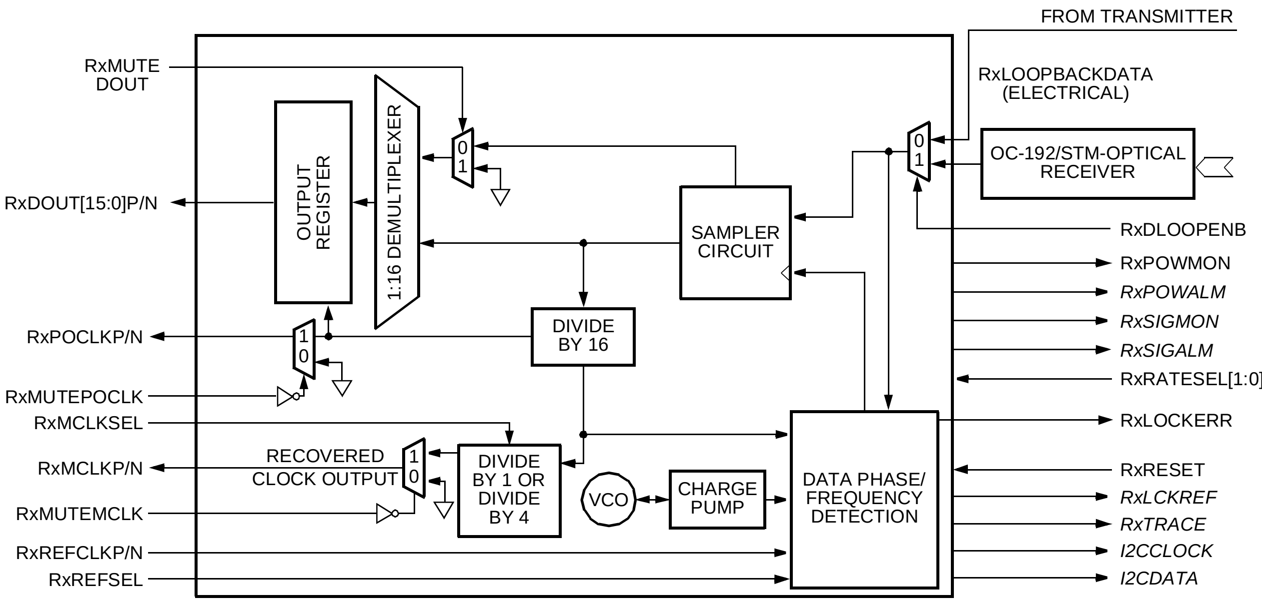


Figure 3. Receiver Block Diagram

Receiver Input/Output Pin Descriptions

Table 3. CB64-Type Transponder, Receiver Input/Output Pin Descriptions

Pin Name	Pin Description
RxLOCKERR	**Clock Recovery Error Indicator (Active-Low)**. Indicates when the internal clock recovery has not locked onto the incoming data stream. RxLOCKERR is an asynchronous output.
RxREFCLKP/N	**Differential ac-Coupled Reference Clock Input at 155.52 MHz or 622 MHz.** The PLL inside the deMUX will lock onto this reference in absence of optical serial input data. Note that this clock frequency must scale to the appropriate reference rate when not operating at the standard OC-192 SONET/SDH rate. Internally ac coupled and biased.
RxREFSEL	**RxREFCLK Frequency Selector**. Logic 0 for 155 MHz (divide by 64) and logic 1 or no connections for 622 MHz (divide by 16).
RxDOUT[15:0]P/N	**16-bit Differential LVDS Parallel Output Data Bus.** DOUT[15:0] is the 622 Mb/s 16-bit output word. DOUT15P/N is the most significant bit of the received word and is the first bit received. DOUT0P/N is the least significant bit of the received word and is the last bit received. Note that this clock frequency must scale to the appropriate reference rate when not operating at the standard OC-192 SONET/SDH rate. Internally ac coupled and biased.
RxPOCLKP/N	**Recovered Differential LVDS Parallel Output Clock of 622 MHz (Nominally 50% Duty Cycle)**. This clock is recovered from the incoming optical signal and is aligned to the DOUT[15:0] output data. When RxPOCLKP/N is not locked to the incoming data signal, RxLOCKERR will be forced low. Pins are active but forced to differential logic low when RxMUTE DOUT = 0. Note that this clock frequency must scale to the appropriate reference rate when not operating at the standard OC-192 SONET/SDH rate. Internally ac coupled and biased.

Pin Information (continued)

Receiver Input/Output Pin Descriptions (continued)

Table 3. CB64-Type Transponder, Receiver Input/Output Pin Descriptions (continued)

Pin Name	Pin Description
RxMUTEPOCLK	Disables the output clock of 622 MHz.
RxPOWMON	**Input Power Monitor Voltage (Analog).** Provides a relative measure of the average input optical (ac + dc) power to the receiver. This signal is referenced to ground. Output voltage to input optical transfer function is 1.0 V/mW.
RxRATESEL[1:0]	**Receiver Rate Select (Active-Low).** Selects the normal OC-192/STM-64 rate, 10 GbE rate, or FEC rate: x, 0 = FEC rate of 10.6642 Gb/s or 10.7092 Gb/s x, 1 = OC-192/STM-64 rate of 9.9532 Gb/s or 10 GbE Ethernet rate of 10.3125 Gb/s where x is either 0 or 1 Note that all input and output clock and data rates are scaled appropriately when operating at the FEC rate.
RxMCLKP/N	**Receiver 155 MHz or 622 MHz Output Clock.**
RxMUTEMCLK	When RxMUTEMCLK is 0, it mutes RxMCLK. Normal operation, when RxMUTEMCLK is 1.
RxMCLKSEL	When 0, RxMCLKSEL selects the RxMCLK frequency of 155 MHz. When 1, RxMCLKSEL selects the RxMCLK frequency of 622 MHz.
RxRESET	**Active-low.** Resets all synchronous logic. During a reset, the data outputs are in the logic low state. Reset must be held active-low for a minimum of 6.4 ns while the internal oscillator is active: 0 = reset 1 or no connection = normal operation
RxDLOOPENB	**Diagnostic Loopback Enable (Active-Low).** Enables diagnostic loopback (10 Gb/s MUX to 10 Gb/s deMUX).
RxMUTEDOUT	**Receiver Mute DOUT (Active-Low).** When RxMUTEDout is active, it forces all deMUX output data RxDout[15:0]P/N to a logic low level. When RxMUTEDOUT is inactive, data to the deMUX will be processed normally. 0 = deMUX output muted 1 or no connection = normal operation
I^2CCLOCK *I^2CDATA* *RxSIGMON* *RxSIGALM* *RxLCKREF* *RxTRACE* *RxPOWALM*	*Pins reserved in MSA. Functions not implemented.*

Pin Information (continued)

Transponder Pin Map

Table 4. Transponder Pin Map

					Receiver Section					
	K	**J**	**H**	**G**	**F**	**E**	**D**	**C**	B	A
1	5.0 V Analog	*RxTRACE*	Frame GND	RxDOUT12P	*1.8 V Digital*	RxDOUT8P	Digital GND	RxDOUT4P	Digital GND	RxDOUT0P
2	5.0 V Analog	FFU	Frame GND	RxDOUT12N	*1.8 V Digital*	RxDOUT8N	Digital GND	RxDOUT4N	Digital GND	RxDOUT0N
3	RxRATESEL0	RxRATESEL1	FFU	Digital GND	RxPOWMON	Digital GND	FFU	Digital GND	FFU	Digital GND
4	3.3 V Analog	NUC	Frame GND	RxDOUT13P	3.3 V Digital	RxDOUT9P	Digital GND	RxDOUT5P	Digital GND	RxDOUT1P
5	3.3 V Analog	NUC	Frame GND	RxDOUT13N	3.3 V Digital	RxDOUT9N	Digital GND	RxDOUT5N	Digital GND	RxDOUT1N
6	RxRESET	NUC	RxDLOOPENB	Digital GND	*RxPOWALM*	Digital GND	FFU	Digital GND	RxMUTEDOUT	Digital GND
7	FFU	FFU	Analog GND	RxDOUT14P	3.3 V Digital	RxDOUT10P	Digital GND	RxDOUT6P	Digital GND	RxDOUT2P
8	FFU	FFU	Analog GND	RxDOUT14N	3.3 V Digital	RxDOUT10N	Digital GND	RxDOUT6N	Digital GND	RxDOUT2N
9	RxMUTEPOCLK	NUC	FFU	Digital GND	*RxSIGMON*	Digital GND	FFU	Digital GND	*RxLCKREF*	Digital GND
10	–5.2 V Analog	FFU	Analog GND	RxDOUT15P	–5.2 V Digital	RxDOUT11P	Digital GND	RxDOUT7P	Digital GND	RxDOUT3P
11	–5.2 V Analog	FFU	Analog GND	RxDOUT15N	–5.2 V Digital	RxDOUT11N	Digital GND	RxDOUT7N	Digital GND	RXDOUT3N
12	RxMUTEMCLK	NUC	FFU	Digital GND	*RxSIGALM*	Digital GND	FFU	Digital GND	RxMCLKSEL	Digital GND
13	–5.2 V Analog	FFU	Analog GND	FFU	–5.2 V Digital	RxPOCLKP	Digital GND	RxMCLKP	Digital GND	RxREFCLKP
14	–5.2 V Analog	*RxALMINT*	Analog GND	FFU	–5.2 V Digital	RxPOCLKN	Digital GND	RxMCLKN	Digital GND	RxREFCLKN
15	I²CCLOCK	NUC	ALMINT	Digital GND	RxREFSEL	Digital GND	FFU	Digital GND	RxLOCKERR	Digital GND
					Transmitter Section					
	K	**J**	**H**	**G**	**F**	**E**	**D**	**C**	B	A
16	5.0 V Analog	*TxALMINT*	Analog GND	TxDIN12P	*1.8 V Digital*	TxDIN8P	Digital GND	TxDIN4P	Digital GND	TxDIN0P
17	5.0 V Analog	FFU	Analog GND	TxDIN12N	*1.8 V Digital*	TxDIN8N	Digital GND	TxDIN4N	Digital GND	TxDIN0N
18	I²CDATA	NUC	*LsTUNE0**	Digital GND	LsBIASMON	Digital GND	LsPOWMON	Digital GND	*TxSKEWSEL0*	Digital GND
19	3.3 V Analog	FFU	Analog GND	TxDIN13P	3.3 V Digital	TxDIN9P	Digital GND	TxDIN5P	Digital GND	TxDIN1P
20	3.3 V Analog	FFU	Analog GND	TxDIN13N	3.3 V Digital	TxDIN9N	Digital GND	TxDIN5N	Digital GND	TxDIN1N
21	TxRATESEL0	TxRATESEL1	*LsTUNE1**	Digital GND	LsENABLE	Digital GND	LsTEMPMON*	Digital GND	*TxSKEWSEL1*	Digital GND
22	3.3 V Analog	FFU	Analog GND	TxDIN14P	3.3 V Digital	TxDIN10P	Digital GND	TxDIN6P	Digital GND	TxDIN2P
23	3.3 V Analog	FFU	Analog GND	TxDIN14N	3.3 V Digital	TxDIN10N	Digital GND	TxDIN6N	Digital GND	TxDIN2N
24	TxRESET	NUC	*LsTUNE2**	Digital GND	LsBIASALM	Digital GND	TxPHSADJ0	Digital GND	*LsTWEAK**	Digital GND
25	–5.2 V Analog	NUC	Frame GND	TxDIN15P	–5.2 V Digital	TxDIN11P	Digital GND	TxDIN7P	Digital GND	TxDIN3P
26	–5.2 V Analog	NUC	Frame GND	TxDIN15N	–5.2 V Digital	TxDIN11N	Digital GND	TxDIN7N	Digital GND	TxDIN3N
27	TxFIFORES	NUC	*TxLLOOPENB*	Digital GND	LsTEMPALM*	Digital GND	TxPHSADJ1	Digital GND	TxPICLKSEL	Digital GND
28	–5.2 V Analog	FFU	Frame GND	TxPICLKP	–5.2 V Digital	TxPCLKP	Digital GND	TxMCLKP	Digital GND	TxREFCLKP
29	–5.2 V Analog	*TxTRACE*	Frame GND	TxPICLKN	–5.2 V Digital	TxPCLKN	Digital GND	TxMCLKN	Digital GND	TxREFCLKN
30	TxFIFOERR	NUC	*TxLINETIMSEL*	DIGital GND	TxREFSEL	Digital GND	FFU	Digital GND	TxLOCKERR	Digital GND

* This feature is only available on lasers using thermoelectric coolers.

Receiver Section		Transmitter Section		Other
(medium grey)	Rx power and GND supplies	(dark grey)	Tx power and GND supplies	NUC: no user connection
(light grey)	Rx dc signals	(grey)	Tx dc signals	FFU: reserved for future use
(white)	622 Mb/s differential signals (transmitter and receiver sections)			*Italics:* future feature (not immediately available)

Pin Information (continued)

Truth Tables

Table 5. CB64-Type Transponder Pin-Map Truth Table (Transmitter)

Pin Name and Pin Configuration		Description
LsENABLE		
0		Normal Operation.
1		Laser Disabled.
LsBIASALM		
0		Laser Bias Alarm Active.
1		Normal Operation.
LSTEMPALM		
0		Laser Temperature Alarm Active.
1		Normal Operation.
TxREFSEL		
0		Selects a TxREFCLK Frequency of 155 MHz.
1		Selects a TxREFCLK Frequency of 622 MHz.
TxPICLKSEL[1]		
0		Selects the TxPICLK Frequency of 622MHz.
1		Selects the TxPICLK Frequency of 311 MHz.
TxLOCKERR		
0		Indicates Loss of PLL Lock.
1		Normal Operation.
TxRESET		
0		Asynchronous MUX System Reset.
1		Normal Operation.
TxFIFOERR		
0		Indicates a MUX FIFO Error.
1		Normal Operation.
ALMINT		
0		Indicates an Alarm.
1		Normal Operation.
TxRATESEL1	TxRATESEL0	
0 or 1	0	FEC rate of 10.6642 Gb/s or 10.7092 Gb/s.
0 or 1	1	OC-192/STM-64 rate of 9.9532 GHz or 10GbE rate of 10.3125 Gb/s.
TxPHSADJ1	TxPHSADJ0	
0	0	Adjusts the Phase of the TxPLCK by 0°.
0	1	Adjusts the Phase of the TxPLCK by 90°.
1	0	Adjusts the Phase of the TxPLCK by 180°.
1	1	Adjusts the Phase of the TxPLCK by 270°.

1. TxPICLK frequency of 622 MHz is the MSA standard. The TxPICLK function should be tied to ground when not used.

Pin Information (continued)

Truth Tables (continued)

Table 6. CB64-Type Transponder Pin-Map Truth Table (Receiver)

Pin Name and Pin Configuration		Description
RxRESET		
0		Asynchronous DeMUX System Reset.
1		Normal Operation.
RxMUTEPOCLK		
0		Mutes the RxPOCLK.
1		Normal Operations.
RxMUTEMCLK		
0		Mutes the RxMCLK.
1		Normal Operations.
RxDLOOPENB		
0		Enables Diagnostic Loopback (10 Gb/s MUX to 10 Gb/s DeMUX).
1		Normal Operation.
RxMUTEDOUT		
0		Mutes the RxDOUT[15:0].
1		Normal Operation.
RxLCKREF		
0		*RxPOCLK Locks to RxREFCLK.*
1		*Normal Operation.*
RxMCLKSEL		
0		Selects the RxMCLK Frequency of 155 MHZ.
1		Selects the RxMCLK Frequency of 622 MHZ.
RxLOCKERR		
0		Indicates Loss of PLL Lock.
1		Normal Operation.
RxPOWALM		
0		Indicates Alarm Active.
1		Normal Operation.
RxSIGALM		
0		Indicates Alarm Active.
1		Normal Operation.
RxREFSEL		
0		Selects an RxREFCLK Frequency of 155 MHz.
1		Selects an RxREFCLK Frequency of 622 MHz.
RxRATESEL1	RxRATESEL0	
0 or 1	0	FEC Rate of 10.6642 Gb/s or 10.7092 Gb/s.
0 or 1	1	OC-192/STM-64 Rate of 9.9532 GHz or 10GbE rate of 10.3125 Gb/s.

Pin Information (continued)

Pin-Map Definitions

Table 7. CB64-Type Transponder Pin-Map Definitions

Pin #	Pin Name	I/O	Logic	Description
A1	RxDout0P	O	LVDS	Receiver 622 Mb/s Data Output.
A2	RxDout0N	O	LVDS	Receiver 622 Mb/s Data Output.
A3	Digital GND	I	Supply	Receiver Digital Ground.
A4	RxDout1P	O	LVDS	Receiver 622 Mb/s Data Output.
A5	RxDout1N	O	LVDS	Receiver 622 Mb/s Data Output.
A6	Digital GND	I	Supply	Receiver Digital Ground.
A7	RxDout2P	O	LVDS	Receiver 622 Mb/s Data Output.
A8	RxDout2N	O	LVDS	Receiver 622 Mb/s Data Output.
A9	Digital GND	I	Supply	Receiver Digital Ground.
A10	RxDout3P	O	LVDS	Receiver 622 Mb/s Data Output.
A11	RxDout3N	O	LVDS	Receiver 622 Mb/s Data Output.
A12	Digital GND	I	Supply	Receiver Digital Ground.
A13	RxREFCLKP	I	LVDS or LVPECL	Receiver Reference Clock.
A14	RxREFCLKN	I	LVDS or LVPECL	Receiver Reference Clock.
A15	Digital GND	I	Supply	Receiver Digital Ground.
A16	TxDin0P	I	LVDS	Transmitter 622 Mb/s Data Input.
A17	TxDin0N	I	LVDS	Transmitter 622 Mb/s Data Input.
A18	Digital GND	I	Supply	Transmitter Digital Ground.
A19	TxDin1P	I	LVDS	Transmitter 622 Mb/s Data Input.
A20	TxDin1N	I	LVDS	Transmitter 622 Mb/s Data Input.
A21	Digital GND	I	Supply	Transmitter Digital Ground.
A22	TxDin2P	I	LVDS	Transmitter 622 Mb/s Data Input.
A23	TxDin2N	I	LVDS	Transmitter 622 Mb/s Data Input.
A24	Digital GND	I	Supply	Transmitter Digital Ground.
A25	TxDin3P	I	LVDS	Transmitter 622 Mb/s Data Input.
A26	TxDin3N	I	LVDS	Transmitter 622 Mb/s Data Input.
A27	Digital GND	I	Supply	Transmitter Digital Ground.
A28	TxREFCLKP	I	LVDS or LVPECL	Transmitter Reference Clock.
A29	TxREFCLKN	I	LVDS or LVPECL	Transmitter Reference Clock.
A30	Digital GND	I	Supply	Transmitter Digital Ground.

Receiver Section		Transmitter Section		Other
	Rx power and GND supplies		Tx power and GND supplies	NUC: no user connection
	Rx dc signals		Tx dc signals	FFU: reserved for future use
	622 Mb/s differential signals (transmitter and receiver sections)			*Italics:* future feature (not immediately available)

Pin Information (continued)

Pin-Map Definitions (continued)

Table 7. CB64-Type Transponder Pin-Map Definitions (continued)

Pin #	Pin Name	I/O	Logic	Description
B1	Digital GND	I	Supply	Receiver Digital Ground.
B2	Digital GND	I	Supply	Receiver Digital Ground.
B3	FFU	—	—	Reserved for Future Use.
B4	Digital GND	I	Supply	Receiver Digital Ground.
B5	Digital GND	I	Supply	Receiver Digital Ground.
B6	RxMUTEDOUT	I	LVTTL	Mutes the Data Outputs of the DeMUX.
B7	Digital GND	I	Supply	Receiver Digital Ground.
B8	Digital GND	I	Supply	Receiver Digital Ground.
B9	*RxLCKREF*	I	LVTTL	Locks RxPOCLK to RxREFCLK.
B10	Digital GND	I	Supply	Receiver Digital Ground.
B11	Digital GND	I	Supply	Receiver Digital Ground.
B12	RxMCLKSEL	I	LVTTL	Selects Speed of Output RxMCLK.
B13	Digital GND	I	Supply	Receiver Digital Ground.
B14	Digital GND	I	Supply	Receiver Digital Ground.
B15	RxLOCKERR	O	LVTTL	Loss of Lock of RxPOCLK (active-low).
B16	Digital GND	I	Supply	Transmitter Digital Ground.
B17	Digital GND	I	Supply	Transmitter Digital Ground.
B18	*TxSKEWSEL0*	I	LVTTL	Adjusts Skew of TxPICLK (LSB).
B19	Digital GND	I	Supply	Transmitter Digital Ground.
B20	Digital GND	I	Supply	Transmitter Digital Ground.
B21	*TxSKEWSEL1*	I	LVTTL	Adjusts Skew of TxPICLK (MSB).
B22	Digital GND	I	Supply	Transmitter Digital Ground.
B23	Digital GND	I	Supply	Transmitter Digital Ground.
B24	*LsTWEAK*	I	Analog	Laser Fine Tuning of DWDM Wavelength.
B25	Digital GND	I	Supply	Transmitter Digital Ground.
B26	Digital GND	I	Supply	Transmitter Digital Ground.
B27	TxPICLKSEL	I	LVTTL	Selects Speed of Input TxPICLK.
B28	Digital GND	I	Supply	Transmitter Digital Ground.
B29	Digital GND	I	Supply	Transmitter Digital Ground.
B30	TxLOCKERR	O	LVTTL	Indicates Loss of TxPLL Lock.

Receiver Section		Transmitter Section		Other
	Rx power and GND supplies		Tx power and GND supplies	NUC: no user connection
	Rx dc signals		Tx dc signals	FFU: reserved for future use
	622 Mb/s differential signals (transmitter and receiver sections)			*Italics:* future feature (not immediately available)

Pin Information (continued

Pin-Map Definitions (continued)

Table 7. CB64-Type Transponder Pin-Map Definitions (continued)

Pin #	Pin Name	I/O	Logic	Description
C1	RXDOUT4P	O	LVDS	Receiver 622 Mb/s Data Output.
C2	RXDOUT4N	O	LVDS	Receiver 622 Mb/s Data Output.
C3	Digital GND	I	Supply	Receiver Digital Ground.
C4	RXDOUT5P	O	LVDS	Receiver 622 Mb/s Data Output.
C5	RXDOUT5N	O	LVDS	Receiver 622 Mb/s Data Output.
C6	Digital GND	I	Supply	Receiver Digital Ground.
C7	RXDOUT6P	O	LVDS	Receiver 622 Mb/s Data Output.
C8	RXDOUT6N	O	LVDS	Receiver 622 Mb/s Data Output.
C9	Digital GND	I	Supply	Receiver Digital Ground.
C10	RXDOUT7P	O	LVDS	Receiver 622 Mb/s Data Output.
C11	RXDOUT7N	O	LVDS	Receiver 622 Mb/s Data Output.
C12	Digital GND	I	Supply	Receiver Digital Ground.
C13	RXMCLKP	O	LVDS	VCO-Derived Output Rx Clock.
C14	RXMCLKN	O	LVDS	VCO-Derived Output Rx Clock.
C15	Digital GND	I	Supply	Receiver Digital Ground.
C16	TXDIN4P	I	LVDS	Transmitter 622 Mb/s Data Input.
C17	TXDIN4N	I	LVDS	Transmitter 622 Mb/s Data Input.
C18	Digital GND	I	Supply	Transmitter Digital Ground.
C19	TXDIN5P	I	LVDS	Transmitter 622 Mb/s Data Input.
C20	TXDIN5N	I	LVDS	Transmitter 622 Mb/s Data Input.
C21	Digital GND	I	Supply	Transmitter Digital Ground.
C22	TXDIN6P	I	LVDS	Transmitter 622 Mb/s Data Input.
C23	TXDIN6N	I	LVDS	Transmitter 622 Mb/s Data Input.
C24	Digital GND	I	Supply	Transmitter Digital Ground.
C25	TXDIN7P	I	LVDS	Transmitter 622 Mb/s Data Input.
C26	TXDIN7N	I	LVDS	Transmitter 622 Mb/s Data Input.
C27	Digital GND	I	Supply	Transmitter Digital Ground.
C28	TXMCLKP	O	LVDS	VCO-Derived Output Tx Clock.
C29	TXMCLKN	O	LVDS	VCO-Derived Output Tx Clock.
C30	Digital GND	I	Supply	Transmitter Digital Ground.

Receiver Section		Transmitter Section		Other
	Rx power and GND supplies		Tx power and GND supplies	NUC: no user connection
	Rx dc signals		Tx dc signals	FFU: reserved for future use
	622 Mb/s differential signals (transmitter and receiver sections)			*Italics:* future feature (not immediately available)

Pin Information (continued)

Pin-Map Definitions (continued)

Table 7. CB64-Type Transponder Pin-Map Definitions (continued)

Pin #	Pin Name	I/O	Logic	Description
D1	Digital GND	I	Supply	Receiver Digital Ground.
D2	Digital GND	I	Supply	Receiver Digital Ground.
D3	FFU	—	—	Reserved for Future Use.
D4	Digital GND	I	Supply	Receiver Digital Ground.
D5	Digital GND	I	Supply	Receiver Digital Ground.
D6	FFU	—	—	Reserved for Future Use.
D7	Digital GND	I	Supply	Receiver Digital Ground.
D8	Digital GND	I	Supply	Receiver Digital Ground.
D9	FFU	—	—	Reserved for Future Use.
D10	Digital GND	I	Supply	Receiver Digital Ground.
D11	Digital GND	I	Supply	Receiver Digital Ground.
D12	FFU	—	—	Reserved for Future Use.
D13	Digital GND	I	Supply	Receiver Digital Ground.
D14	Digital GND	I	Supply	Receiver Digital Ground.
D15	FFU	—	—	Reserved for Future Use.
D16	Digital GND	I	Supply	Transmitter Digital Ground.
D17	Digital GND	I	Supply	Transmitter Digital Ground.
D18	LsPOWMON	O	Analog	Laser Output Power Monitor.
D19	Digital GND	I	Supply	Transmitter Digital Ground.
D20	Digital GND	I	Supply	Transmitter Digital Ground.
D21	LsTEMPMON	O	Analog	Laser Temperature Monitor.
D22	Digital GND	I	Supply	Transmitter Digital Ground.
D23	Digital GND	I	Supply	Transmitter Digital Ground.
D24	TxPHSADJ0	I	LVTTL	Adjusts Phase of TxPCLK (LSB).
D25	Digital GND	I	Supply	Transmitter Digital Ground.
D26	Digital GND	I	Supply	Transmitter Digital Ground.
D27	TxPHSADJ1	I	LVTTL	Adjusts Phase of TxPCLK (MSB).
D28	Digital GND	I	Supply	Transmitter Digital Ground.
D29	Digital GND	I	Supply	Transmitter Digital Ground.
D30	FFU	—	—	Reserved for Future Use.

Receiver Section		Transmitter Section		Other
	Rx power and GND supplies		Tx power and GND supplies	NUC: no user connection
	Rx dc signals		Tx dc signals	FFU: reserved for future use
	622 Mb/s differential signals (transmitter and receiver sections)			*Italics:* future feature (not immediately available)

Pin Information (continued)

Pin-Map Definitions (continued)

Table 7. CB64-Type Transponder Pin-Map Definitions (continued)

Pin #	Pin Name	I/O	Logic	Description
E1	RXDOUT8P	O	LVDS	Receiver 622 Mb/s Data Output.
E2	RXDOUT8N	O	LVDS	Receiver 622 Mb/s Data Output.
E3	Digital GND	I	Supply	Receiver Digital Ground.
E4	RXDOUT9P	O	LVDS	Receiver 622 Mb/s Data Output.
E5	RXDOUT9N	O	LVDS	Receiver 622 Mb/s Data Output.
E6	Digital GND	I	Supply	Receiver Digital Ground.
E7	RXDOUT10P	O	LVDS	Receiver 622 Mb/s Data Output.
E8	RXDOUT10N	O	LVDS	Receiver 622 Mb/s Data Output.
E9	Digital GND	I	Supply	Receiver Digital Ground.
E10	RXDOUT11P	O	LVDS	Receiver 622 Mb/s Data Output.
E11	RXDOUT11N	O	LVDS	Receiver 622 Mb/s Data Output.
E12	Digital GND	I	Supply	Receiver Digital Ground.
E13	RXPOCLKP	O	LVDS	Receiver Parallel Output Clock.
E14	RXPOCLKN	O	LVDS	Receiver Parallel Output Clock.
E15	Digital GND	I	Supply	Receiver Digital Ground.
E16	TXDIN8P	I	LVDS	Transmitter 622 Mb/s Data Input.
E17	TXDIN8N	I	LVDS	Transmitter 622 Mb/s Data Input.
E18	Digital GND	I	Supply	Transmitter Digital Ground.
E19	TXDIN9P	I	LVDS	Transmitter 622 Mb/s Data Input.
E20	TXDIN9N	I	LVDS	Transmitter 622 Mb/s Data Input.
E21	Digital GND	I	Supply	Transmitter Digital Ground.
E22	TXDIN10P	I	LVDS	Transmitter 622 Mb/s Data Input.
E23	TXDIN10N	I	LVDS	Transmitter 622 Mb/s Data Input.
E24	Digital GND	I	Supply	Transmitter Digital Ground.
E25	TXDIN11P	I	LVDS	Transmitter 622 Mb/s Data Input.
E26	TXDIN11N	I	LVDS	Transmitter 622 Mb/s Data Input.
E27	Digital GND	I	Supply	Transmitter Digital Ground.
E28	TXPCLKP	O	LVDS	Transmitter Parallel Output Clock.
E29	TXPCLKN	O	LVDS	Transmitter Parallel Output Clock.
E30	Digital GND	I	Supply	Transmitter Digital Ground.

Receiver Section		Transmitter Section		Other
	Rx power and GND supplies		Tx power and GND supplies	NUC: no user connection
	Rx dc signals		Tx dc signals	FFU: reserved for future use
	622 Mb/s differential signals (transmitter and receiver sections)			*Italics:* future feature (not immediately available)

Pin Information (continued)

Pin-Map Definitions (continued)

Table 7. CB64-Type Transponder Pin-Map Definitions (continued)

Pin #	Pin Name	I/O	Logic	Description
F1	*1.8 V Digital*	I	Supply	Receiver Digital Power.
F2	*1.8 V Digital*	I	Supply	Receiver Digital Power.
F3	RxPOWMON	O	Analog	Receiver Power Monitor (ac + dc).
F4	3.3 V Digital	I	Supply	Receiver Digital Power.
F5	3.3 V Digital	I	Supply	Receiver Digital Power.
F6	*RxPOWALM*	O	LVTTL	Loss of Receiver Average Power Alarm.
F7	3.3 V Digital	I	Supply	Receiver Digital Power.
F8	3.3 V Digital	I	Supply	Receiver Digital Power.
F9	*RxSIGMON*	O	Analog	Receiver Signal Monitor (ac only).
F10	–5.2 V Digital	I	Supply	Receiver Digital Power.
F11	–5.2 V Digital	I	Supply	Receiver Digital Power.
F12	*RxSIGALM*	O	LVTTL	Loss of Receiver ac Power Alarm
F13	–5.2 V Digital	I	Supply	Receiver Digital Power.
F14	–5.2 V Digital	I	Supply	Receiver Digital Power.
F15	RxREFSEL	I	LVTTL	Selects RxREFCLK Frequency.
F16	*1.8 V Digital*	I	Supply	Transmitter Digital Power.
F17	*1.8 V Digital*	I	Supply	Transmitter Digital Power.
F18	LsBIASMON	O	Analog	Laser Bias Current Monitor.
F19	3.3 V Digital	I	Supply	Transmitter Digital Power.
F20	3.3 V Digital	I	Supply	Transmitter Digital Power.
F21	LsENABLE	I	LVTTL	Laser Enable (disable is inverse).
F22	3.3 V Digital	I	Supply	Transmitter Digital Power.
F23	3.3 V Digital	I	Supply	Transmitter Digital Power.
F24	LsBIASALM	O	LVTTL	Laser Bias Current Alarm.
F25	–5.2 V Digital	I	Supply	Transmitter Digital Ground.
F26	–5.2 V Digital	I	Supply	Transmitter Digital Ground.
F27	LsTEMPALM	O	LVTTL	Laser Temperature Alarm.
F28	–5.2 V Digital	I	Supply	Transmitter Digital Power.
F29	–5.2 V Digital	I	Supply	Transmitter Digital Power.
F30	TxREFSEL	I	LVTTL	Selects TxREFCLK Frequency.

Receiver Section		Transmitter Section		Other
	Rx power and GND supplies		Tx power and GND supplies	NUC: no user connection
	Rx dc signals		Tx dc signals	FFU: reserved for future use
	622 Mb/s differential signals (transmitter and receiver sections)			*Italics:* future feature (not immediately available)

Pin Information (continued)

Pin-Map Definitions (continued)

Table 7. CB64-Type Transponder Pin-Map Definitions (continued)

Pin #	Pin Name	I/O	Logic	Description
G1	RXDOUT12P	O	LVDS	Receiver 622 Mb/s Data Output.
G2	RXDOUT12N	O	LVDS	Receiver 622 Mb/s Data Output.
G3	Digital GND	I	Supply	Receiver Digital Ground.
G4	RXDOUT13P	O	LVDS	Receiver 622 Mb/s Data Output.
G5	RXDOUT13N	O	LVDS	Receiver 622 Mb/s Data Output.
G6	Digital GND	I	Supply	Receiver Digital Ground.
G7	RXDOUT14P	O	LVDS	Receiver 622 Mb/s Data Output.
G8	RXDOUT14N	O	LVDS	Receiver 622 Mb/s Data Output.
G9	Digital GND	I	Supply	Receiver Digital Ground.
G10	RXDOUT15P	O	LVDS	Receiver 622 Mb/s Data Output.
G11	RXDOUT15N	O	LVDS	Receiver 622 Mb/s Data Output.
G12	Digital GND	I	Supply	Receiver Digital Ground.
G13	FFU	—	—	Reserved for Future Use.
G14	FFU	—	—	Reserved for Future Use.
G15	Digital GND	I	Supply	Receiver Digital Ground.
G16	TXDIN12P	I	LVDS	Transmitter 622 Mb/s Data Input.
G17	TXDIN12N	I	LVDS	Transmitter 622 Mb/s Data Input.
G18	Digital GND	I	Supply	Transmitter Digital Ground.
G19	TXDIN13P	I	LVDS	Transmitter 622 Mb/s Data Input.
G20	TXDIN13N	I	LVDS	Transmitter 622 Mb/s Data Input.
G21	Digital GND	I	Supply	Transmitter Digital Ground.
G22	TXDIN14P	I	LVDS	Transmitter 622 Mb/s Data Input.
G23	TXDIN14N	I	LVDS	Transmitter 622 Mb/s Data Input.
G24	Digital GND	I	Supply	Transmitter Digital Ground.
G25	TXDIN15P	I	LVDS	Transmitter 622 Mb/s Data Input.
G26	TXDIN15N	I	LVDS	Transmitter 622 Mb/s Data Input.
G27	Digital GND	I	Supply	Transmitter Digital Ground.
G28	TXPICLKP	I	LVDS	Transmitter Parallel Input Clock.
G29	TXPICLKN	I	LVDS	Transmitter Parallel Input Clock.
G30	Digital GND	I	Supply	Transmitter Digital Ground.

Receiver Section		Transmitter Section		Other
	Rx power and GND supplies		Tx power and GND supplies	NUC: no user connection
	Rx dc signals		Tx dc signals	FFU: reserved for future use
	622 Mb/s differential signals (transmitter and receiver sections)			*Italics:* future feature (not immediately available)

Pin Information (continued)

Pin-Map Definitions (continued)

Table 7. CB64-Type Transponder Pin-Map Definitions (continued)

Pin #	Pin Name	I/O	Logic	Description
H1	Frame GND	I	Supply	Frame GND Tied to Chassis Ground.
H2	Frame GND	I	Supply	Frame GND Tied to Chassis Ground.
H3	FFU	—	—	Reserved for Future Use.
H4	Frame GND	I	Supply	Frame GND Tied to Chassis Ground.
H5	Frame GND	I	Supply	Frame GND Tied to Chassis Ground.
H6	RxDLOOPENB	I	LVTTL	Diagnostic Loopback Enable.
H7	Analog GND	I	Supply	Receiver Analog Ground.
H8	Analog GND	I	Supply	Receiver Analog Ground.
H9	FFU	—	—	Reserved for Future Use.
H10	Analog GND	I	Supply	Receiver Analog Ground.
H11	Analog GND	I	Supply	Receiver Analog Ground.
H12	FFU	—	—	Reserved for Future Use.
H13	Analog GND	I	Supply	Receiver Analog Ground.
H14	Analog GND	I	Supply	Receiver Analog Ground.
H15	ALMINT	O	Open Drain	Electrical OR of All Rx and Tx Alarms.
H16	Analog GND	I	Supply	Transmitter Analog Ground.
H17	Analog GND	I	Supply	Transmitter Analog Ground.
H18	*LsTUNE0*	I	LVTTL	Wavelength-Select Pin 0 (LSB).
H19	Analog GND	I	Supply	Transmitter Analog Ground.
H20	Analog GND	I	Supply	Transmitter Analog Ground.
H21	*LsTUNE1*	I	LVTTL	Wavelength-Select Pin 1.
H22	Analog GND	I	Supply	Transmitter Analog Ground.
H23	Analog GND	I	Supply	Transmitter Analog Ground.
H24	*LsTUNE2*	I	LVTTL	Wavelength-Select Pin 2 (MSB).
H25	Frame GND	I	Supply	Frame GND Tied to Chassis Ground.
H26	Frame GND	I	Supply	Frame GND Tied to Chassis Ground.
H27	*TxLLOOPENB*	I	LVTTL	Line Loopback Enable.
H28	Frame GND	I	Supply	Frame GND Tied to Chassis Ground.
H29	Frame GND	I	Supply	Frame GND Tied to Chassis Ground.
H30	*TxLINETIMSEL*	I	LVTTL	Line Timing Select.

Receiver Section		Transmitter Section		Other
	Rx power and GND supplies		Tx power and GND supplies	NUC: no user connection
	Rx dc signals		Tx dc signals	FFU: reserved for future use
	622 Mb/s differential signals (transmitter and receiver sections)			*Italics:* future feature (not immediately available)

Pin Information (continued)

Pin-Map Definitions (continued)

Table 7. CB64-Type Transponder Pin-Map Definitions (continued)

Pin #	Pin Name	I/O	Logic	Description
J1	*RxTRACE*	O	Analog	Low Frequency Photodiode Output.
J2	FFU	—	—	Reserved for Future Use.
J3	RxRATESEL1	I	LVTTL	Receiver Bit Rate Select (MSB).
J4	NUC	—	—	No User Connection.
J5	NUC	—	—	No User Connection.
J6	NUC	—	—	No User Connection.
J7	FFU	—	—	Reserved for Future Use.
J8	FFU	—	—	Reserved for Future Use.
J9	NUC	—	—	No User Connection.
J10	FFU	—	—	Reserved for Future Use.
J11	FFU	—	—	Reserved for Future Use.
J12	NUC	—	—	No User Connection.
J13	FFU	—	—	Reserved for Future Use.
J14	*RxALMINT*	O	Open Drain	Electrical OR of All Rx Alarms.
J15	NUC	—	—	No User Connection.
J16	*TxALMINT*	O	Open Drain	Electrical OR of All Tx Alarms.
J17	FFU	—	—	Reserved for Future Use.
J18	NUC	—	—	No User Connection.
J19	FFU	—	—	Reserved for Future Use.
J20	FFU	—	—	Reserved for Future Use.
J21	TxRATESEL1	I	LVTTL	Receiver Bit Rate Select (MSB).
J22	FFU	—	—	Reserved for Future Use.
J23	FFU	—	—	Reserved for Future Use.
J24	NUC	—	—	No User Connection.
J25	NUC	—	—	No User Connection.
J26	NUC	—	—	No User Connection.
J27	NUC	—	—	No User Connection.
J28	FFU	—	—	Reserved for Future Use.
J29	*TxTRACE*	I	Analog	Low-Frequency Transmitter Input.
J30	NUC	—	—	No User Connection.

Receiver Section		Transmitter Section		Other
	Rx power and GND supplies		Tx power and GND supplies	NUC: no user connection
	Rx dc signals		Tx dc signals	FFU: reserved for future use
	622 Mb/s differential signals (transmitter and receiver sections)			*Italics:* future feature (not immediately available)

Pin Information (continued)

Pin-Map Definitions (continued)

Table 7. CB64-Type Transponder Pin-Map Definitions (continued)

Pin #	Pin Name	I/O	Logic	Description
K1	5.0 V Analog	I	Supply	Receiver Analog Power
K2	5.0 V Analog	I	Supply	Receiver Analog Power
K3	RxRATESEL0	I	LVTTL	Receiver Bit Rate Select (LSB)
K4	3.3 V Analog	I	Supply	Receiver Analog Power
K5	3.3 V Analog	I	Supply	Receiver Analog Power
K6	RxRESET	I	LVTTL	Receiver Asynchronous System Reset
K7	FFU	—	—	Reserved for Future Use
K8	FFU	—	—	Reserved for Future Use
K9	RxMUTEPOCLK	I	LVTTL	Mutes the RxPOCLK
K10	–5.2 V Analog	I	Supply	Receiver Analog Power
K11	–5.2 V Analog	I	Supply	Receiver Analog Power
K12	RxMUTEMCLK	I	LVTTL	Mutes the RxMCLK
K13	–5.2 V Analog	I	Supply	Receiver Analog Power
K14	–5.2 V Analog	I	Supply	Receiver Analog Power
K15	I^2CCLOCK	I	LVTTL	I^2C Clock Input for Remote Access
K16	5.0 V Analog	I	Supply	Transmitter Analog Power
K17	5.0 V Analog	I	Supply	Transmitter Analog Power
K18	I^2CDATA	I/O	LVTTL	I^2C Data Input/Output for Remote Access
K19	3.3 V Analog	I	Supply	Transmitter Analog Power
K20	3.3 V Analog	I	Supply	Transmitter Analog Power
K21	TxRATESEL0	I	LVTTL	Transmitter Bit Rate Select (LSB)
K22	3.3 V Analog	I	Supply	Transmitter Analog Power
K23	3.3 V Analog	I	Supply	Transmitter Analog Power
K24	TxRESET	I	LVTTL	Transmitter Asynchronous System Reset
K25	–5.2 V Analog	I	Supply	Transmitter Analog Power
K26	–5.2 V Analog	I	Supply	Transmitter Analog Power
K27	TxFIFORES	I	LVTTL	MUX FIFO Reset
K28	–5.2 V Analog	I	Supply	Transmitter Analog Power
K29	–5.2 V Analog	I	Supply	Transmitter Analog Power
K30	TxFIFOERR	O	LVTTL	MUX FIFO Error Indicator

Receiver Section		Transmitter Section		Other
	Rx power and GND supplies		Tx power and GND supplies	NUC: no user connection
	Rx dc signals		Tx dc signals	FFU: reserved for future use
	622 Mb/s differential signals (transmitter and receiver sections)			*Italics:* future feature (not immediately available)

Electrical/Optical Characteristics

Maximum and minimum values are specified over operating case temperature range at 50% duty cycle.

Table 8. Receiver Electrical I/O Characteristics (T_C = 0 °C to 65 °C)

Parameter	Symbol	Logic	Min	Typ	Max	Unit
Receiver Input Power Monitor	RxPOWMON	Analog	0.8	1	1.2	V/mW
Receiver Input ac Power Monitor	*RxSIGMON*	*Analog*	—	*TBD*	—	*V/mV*
Clock Recovery Lock Error: Output High, V_{OH} Output Low, V_{OL}	RxLOCKERR	LVTTL	 2.4 0	 — —	 3.47 0.8	 V V
Select MCLK (155 MHz/622 MHz): Input High, V_{IH} Input Low, V_{IL}	RxMCLKSEL	LVTTL*	 2.1 0	 — —	 3.47 0.8	 V V
Select Reference Clock: Input High, V_{IH} Input Low, V_{IL}	RxREFSEL	LVTTL*	 2.1 0	 — —	 3.47 0.8	 V V
Mute Parallel Output Clock: Input High, V_{IH} Input Low, V_{IL}	RxMUTEPOCLK	LVTTL*	 2.1 0	 — —	 3.47 0.8	 V V
Reset: Input High, V_{IH} Input Low, V_{IL}	RxRESET	LVTTL*	 2.1 0	 — —	 3.47 0.8	 V V
Rate Select: Input High, V_{IH} Input Low, V_{IL}	RxRATESEL[1:0]	LVTTL*	 2.1 0	 — —	 3.47 0.8	 V V
Rx Mute Data Out: Input High, V_{IH} Input Low, V_{IL}	RxMUTE DOUT	LVTTL*	 2.1 0	 — —	 3.47 0.8	 V V
Parallel Data Outputs: Output High, V_{OH} Output Low, V_{OL} Differential Output Voltage Swing	RxDOUT[15:0]P/N	LVDS	 — 0.925 250	 — — —	 1.475 — 400	 mV mV mV
Reference Clock Input: Input Voltage Frequency Tolerance Input Duty Cycle Rise and Fall Times	RxREFCLKP/N	Differential ac-coupled LVDS or LVPECL	 100 –20 40 20	 — — 50 —	 800 20 60 TBD	 mVp-p ppm % ps
155 MHz Clock Output: Output High, V_{OH} Output Low, V_{OL} Output Voltage Swing Duty Cycle	RxMCLKP/N	LVDS	 — 0.925 250 45	 — — — —	 1.475 — 400 55	 mV mV mV %
Recovered Parallel Output Clock: Output High, V_{OH} Output Low, V_{OL} Output Voltage Swing Duty Cycle	RxPOCLKP/N	LVDS	 — 0.925 250 45	 — — — —	 1.475 — 400 55	 mV mV mV %

* Note that LVTTL input and output values are different. Input values take board signal losses into consideration.

Electrical/Optical Characteristics (continued)

Maximum and minimum values are specified over operating case temperature range at 50% duty cycle.

Table 9. Transmitter Electrical I/O Characteristics (T_C = 0 °C to 65 °C)

Parameter	Symbol	Logic	Min	Typ	Max	Unit
Laser Enable:[1]	LsENABLE	LVTTL[2]				
Input High, V_{IH}			2.1	—	3.47	V
Input Low, V_{IL}			0	—	0.8	V
Laser Bias Output	LsBIASMON	Analog	0	1650	3500	mV
Laser Degrade Alarm Output:[3]	LsBIASALM	LVTTL				
Output High, V_{OH}			2.4	—	3.47	V
Output Low, V_{OL}			0	—	0.5	V
Laser Power Monitor Output	LsPOWMON	Analog	—	500	1000	mV
Laser Temperature Monitor Output	LsTEMPMON	Analog	—	2500	—	mV
Laser Temperature Alarm Output:	LsTEMPALM	LVTTL		—		
Output High, V_{OH}			2.4		3.47	V
Output Low, V_{OL}			0	—	0.8	V
Lock Error of MUX PLL:[4]	TxLOCKERR	LVTTL				
Output High, V_{OH}			2.4	—	3.47	V
Output Low, V_{OL}			0	—	0.8	V
Reference Clock:	TxREFCLKP/N	Differential				
Differential Input Voltage Swing		ac-coupled	100	—	800	mVp-p
Frequency Tolerance		LVDS or	–20	—	20	ppm
Input Duty Cycle		LVPECL	40	50	60	%
Rise and Fall Times			20	—	TBD	ps
Input Data Signal Level:	TxDin[15:0]P/N	LVDS				
Input Voltage Range			0	1200	2400	mV
Differential Input Voltage Swing			100	—	400	mVp-p
Differential Input Impedance			80	100	120	Ω
Parallel Input Clock:	TxPICLKP/N	LVDS				
Frequency			—	622.08	—	MHz
Input Common Voltage Range			0	1200	2400	mV
Differential Input Voltage Swing			100	—	400	mVp-p
Differential Input Impedance			80	100	120	Ω
622 MHz Parallel Output Clock:	TxPCLKP/N	LVDS				
Output High, V_{OH}			—	—	1.475	mV
Output Low, V_{OL}			0.925	—	—	mV
Differential Output Voltage Swing			250	—	400	mV
Duty Cycle			45	—	55	%
155 MHz Output Clock:	TxMCLKP/N	LVDS				
Output High, V_{OH}			—	—	1.475	mV
Output Low, V_{OL}			0.925	—	—	mV
Diff. Output Voltage Swing			250	—	400	mV
Duty Cycle			45	—	55	%

1. The transmitter is normally enabled and requires only an active-high external voltage to disable.
2. Please note that LVTTL input and output values are different. Input values take board signal losses into consideration.
3. The alarm will go active low when the bias current to the laser increases by 50% or decreases by 50% from its beginning-of-life (BOL) value.
4. Active-low.

Electrical/Optical Characteristics (continued)

Maximum and minimum values are specified over operating case temperature range at 50% duty cycle.

Table 9. Transmitter Electrical I/O Characteristics (T_C = 0 °C to 65 °C) (continued)

Parameter	Symbol	Logic	Min	Typ	Max	Unit
TxREFCLK Reference Select:	TxREFSEL	LVTTL[2]				
Input High, V_{IH}			2.1	—	3.47	V
Input Low, V_{IL}			0	—	0.8	V
Diagnostic Loop Enable:	RxDLOOPENB	LVTTL[2]				
Input High, V_{IH}			2.1	—	3.47	V
Input Low, V_{IL}			0	—	0.8	V
Tx Reset:	TxRESET	LVTTL[2]				
Input High, V_{IH}			2.1	—	3.47	V
Input Low, V_{IL}			0	—	0.8	V
Alarm Interrupt:	ALMINT	LVTTL[5]				
Output High, V_{OH}			2.4	—	3.47	V
Output Low, V_{OL}			0	—	0.8	V
Tx Rate Select:	TxRATESEL[1:0]	LVTTL[2]				
Input High, V_{IH}			2.1	—	3.47	V
Input Low, V_{IL}			0	—	0.8	V

1. The transmitter is normally enabled and requires only an active-high external voltage to disable.
2. Please note that LVTTL input and output values are different. Input values take board signal losses into consideration.
3. The alarm will go active low when the bias current to the laser increases by 50% or decreases by 50% from its beginning-of-life (BOL) value.
4. Active-low.
5. Open drain output.

Electrical/Optical Characteristics (continued)

Minimum and maximum values specified over operating case temperature range at 50% duty cycle data signal.

Table 10. OC-192/STM-64 Transmitter Optical Characteristics (Tc = 0 °C to 65 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Average Output Power[1]	P_O	–1	—	2	dBm
Operating Wavelength	λ	1530	1550	1565	nm
Spectral Width[2]	—	—	—	1	nm
Side-mode Suppression Ratio (DFB laser)[3]	SMSR	30	—	—	dB
Extinction Ratio[4]	ER	8.2	—	—	dB
Optical Rise/Fall Times	t_R/t_F	—	—	40	ps
Optical Path Penalty (40 km)	P_P	—	—	2	dB
Eye Mask of Optical Output[5, 6]	Compliant with GR-253-CORE and ITU-T G.691				
Jitter Generation	Compliant with GR-253-CORE and ITU-T G.691				
Jitter Transfer	Compliant with GR-253-CORE and ITU-T G.691				
Jitter Tolerance	Compliant with GR-253-CORE and ITU-T G.691				

1. Output power definitions and measurements per ITU-T Recommendation G.691.
2. Full spectral width measured 20 dB down from the central wavelength peak under fully modulated conditions.
3. Ratio of the average output power in the dominant longitudinal mode to the power in the most significant side mode under fully modulated conditions.
4. Ratio of logic 1 output power to logic 0 output power under fully modulated conditions.
5. GR-253-CORE, *Synchronous Optical Network (SONET) OC-192 Transport Systems: Common Generic Criteria.*
6. Draft ITU-T Recommendation G.691, *Optical Interfaces for Single-Channel SDH Systems with Optical Amplifiers, and STM-64 Systems.*

Table 11. OC-192/STM-64 Receiver Optical Characteristics (Tc = 0 °C to 65 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Average Receiver Sensitivity (EOL)[1]	PR_{MIN}	–14	—	—	dBm
Average Receiver Overload (EOL)	—	–1	—	—	dBm
Receiver Reflectance	—	—	—	–27	dB

1. PIN receiver at 1550 nm, 1 x 10^{-12} BER, 2^{23} – 1 pseudorandom data input.

Table 12. Power Supply Characteristics* (T_C = 0 °C to 65 °C)

Parameter	Symbol	Min	Typ	Max	Unit
3.3 V Supply Voltage	V_{DD}	3.13	3.3	3.46	V
Supply Current Drain	I_{DD}	1.4	1.9	3.0	A
5. 0 V Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Supply Current Drain	I_{CC}	0.08	0.10	0.20	A
–5. 2 V Supply Voltage	V_{EE}	–4.94	–5.2	–5.46	V
Supply Current Drain	I_{EE}	0.3	0.4	0.5	A
Package Power Dissipation	P_{DISS}	6.0	8.0	12	W

* With reference clock filter included.

Functional Description

Receiver

The optical receiver in the CB64-Type transponder is optimized for the particular SDH/SONET application segment in which it was designed to operate and will have a PIN photodetector. The detected serial data output of the optical receiver is connected to a clock and data recovery circuit (CDR) that extracts a 9953.28 MHz clock signal for normal OC-192/STM-64 rate or 10.6642 GHz or 10.709 GHz at FEC rate. This recovered serial bit clock signal and a retimed serial data signal are presented to the 16-bit serial-to-parallel converter.

The receiver contains a lock-detect circuit that monitors the integrity of the serial data inputs. If the received serial data fails the frequency test, the PLL will be forced to lock to the local reference clock. This will maintain the correct frequency of the recovered clock output under loss-of-signal or loss-of-power conditions.

Table 13. CB64-Type Transponder Receiver Timing Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Clock Period	T0	—	1.608	—	ns
Duty Cycle	TW/T0	40	—	50	%
Rise/Fall Time (20%—80%)	t_R/t_F	—	—	300	ps
Data/Clock Skew	$T_{CQ\text{-}MIN}/T_{CQ\text{-}MAX}$	—	—	250/250	ps

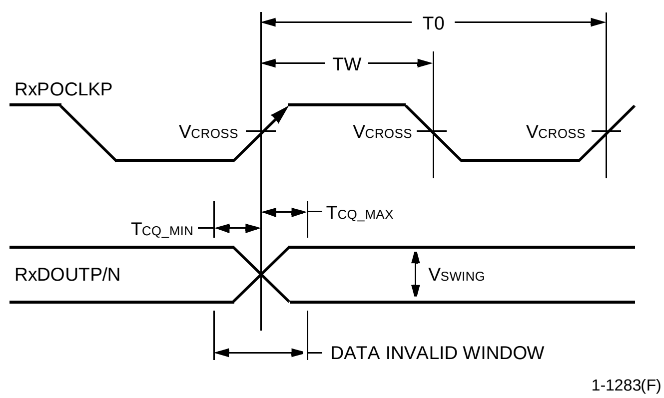


Figure 4. CB64-Type Transponder Receiver Timing Characteristics

Functional Description (continued)

Transmitter

The optical transmitter in the CB64-Type transponder is optimized for the particular SDH/SONET segment in which it is designed to operate. The transmitter has a cooled EML laser as the optical element and operates at the 1550 nm window. A serial data stream developed in the parallel-to-serial conversion logic input drives the transmitter.

The parallel-to-serial converter block shown in Figure 1 is comprised of two byte-wide registers. The first register latches the 16 bits of parallel input data (TxDin[15:0]) on the rising edge of TxPICLK. The second register is a 16-bit parallel load, serial-out shift register that is loaded from the input register. An internally generated byte clock, which is phase aligned to the 9953.28 MHz serial transmit clock, activates the data transfer between the input register and the parallel-to-serial register.

The clock-divider and phase-detect circuitry shown in Figure 1 generates internal reference clocks and timing functions for the transmitter. Therefore, it is important that the TxREFCLKP/N input is generated from a precise and stable source. It is required that the TxREFCLKP/N input be generated from a crystal oscillator or other source having a frequency accuracy better than ±20 ppm.

The timing generation circuitry provides two separate functions. One is a byte-rate clock that is synchronized to the 9953.28 MHz transmit serial clock, the other is a mechanism for aligning the phase between the incoming byte clock (TxPICLKP/N) and the clock that loads the parallel data from the input register into the parallel-to-serial shift register. The TxPCLKP/N output is a byte-rate (622 MHz) version of the serial transmit clock and is intended for use by upstream multiplexing and overhead processing circuits. Using TxPCLKP/N for upstream circuits will ensure a stable frequency and phase relationship between the parallel data coming into the transmitter and the subsequent parallel-to-serial timing functions.

Table 14. CB64-Type Transponder Transmitter Timing Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Clock Period	T0	—	1.608	—	ns
Duty Cycle	TW/T0	40	—	60	%
Rise/Fall Time (20%—80%)	t_R/t_F	100	—	300	ps
Setup Time/Hold Time	T_{SETUP}/T_{HOLD}	—	—	300/300	ps

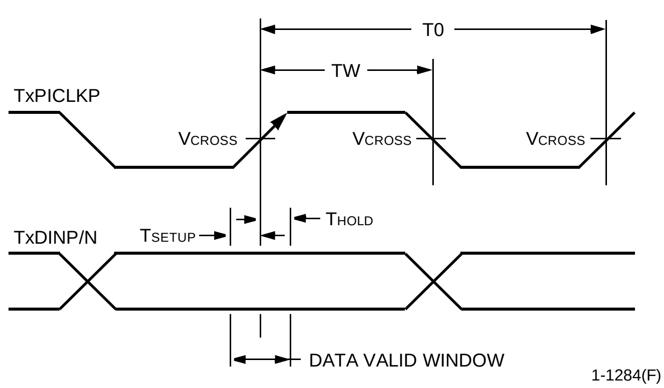


Figure 5. CB64-Type Transponder Transmitter Timing Characteristics

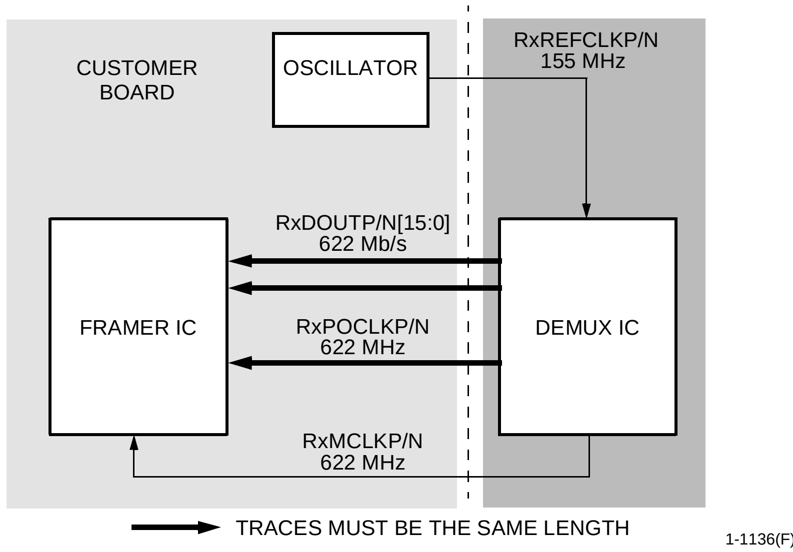
Transponder Interfacing

Receiver Interface Board Layout

All the receiver data outputs (RxDOUTP/N[15:0]) on the customer board should have equal trace lengths, and in most cases, be matched to that of the parallel output clock RxPOCLKP/N. The similar lengths ensure that these signals maintain the propagation delay time values.

It is not required to match the trace length of the RxMCLKP/N. RxMCLKP/N is derived from the RxREFCLKP/N, i.e., from a VCO inside the deMUX. This allows a clock signal to be delivered to the framer even if the RxPOCLKP/N is not locked to any incoming optical signal.

Figure 6 shows the CB64-Type receiver interface board layout.



Note: RxMCLKP/N may not be required for all framers.

Figure 6. CB64-Type Receiver Interface Board Layout

Transponder Interfacing (continued)

Transmitter Interface Board Layout

All the transmitter data inputs, (TxDINP/N[15:0]) should have equal trace lengths on the customer board. There should also be a certain phase relationship between TxDINP/N[15:0] and the parallel input clock (TxPICLKP/N) at the transponder electrical connector input to allow proper MUX operation, as shown by the setup and hold times (TSETUP/THOLD) in Table 14 on page 28. This phase relationship can be ensured if the trace length of the TxPICLKP/N is matched to the trace length of the TxDINP/N data inputs. For TxREFCLKP/N clock, a tolerance of ±20 ppm is required to meet SONET output frequency specifications. To ensure this, using VCXO/PLL circuit is recommended.

The VCO/VCXO chosen should be of an OC-192 SONET quality. The clock should have low phase noise and frequency stability of better than ±20 ppm.

Figure 7 shows the CB64-Type Transmitter Interface Board Layout. Please contact TriQuint Optoelectronics for more details.

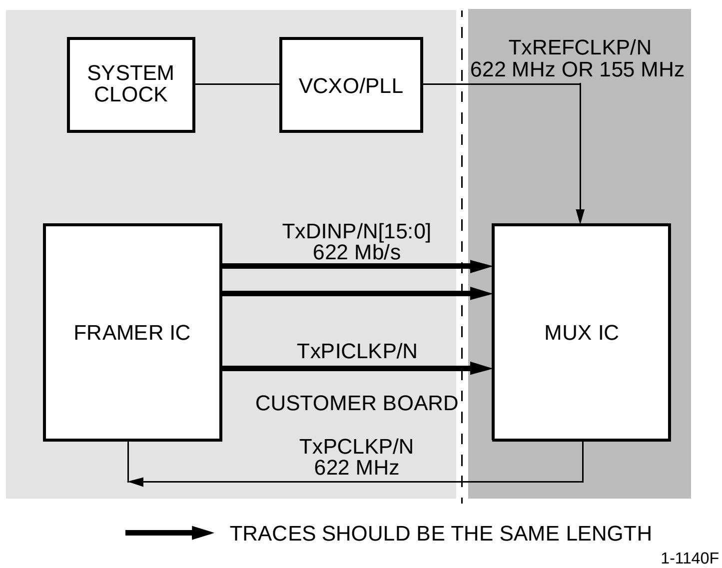


Figure 7. CB64-Type Transmitter Interface Board Layout

Transponder Grounding

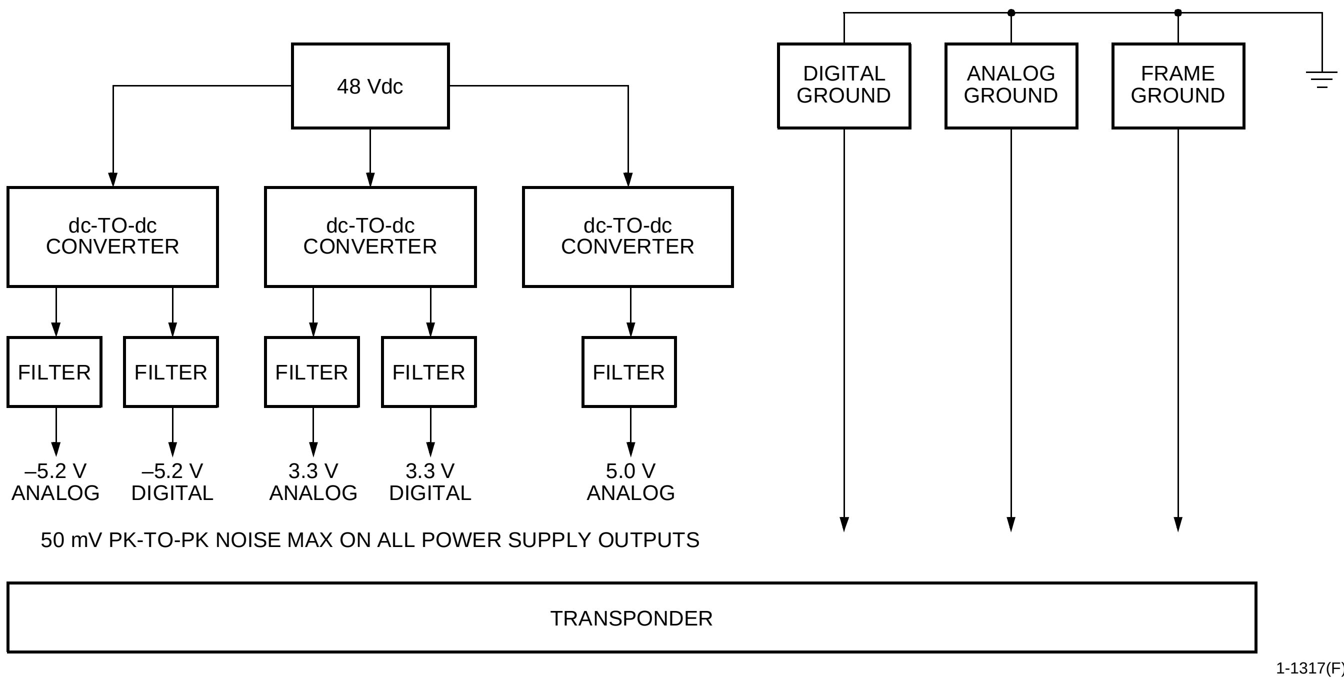


Figure 8. Recommended Grounding Scheme

Qualification and Reliability

To help ensure high product reliability and customer satisfaction, TriQuint Optoelectronics is committed to an intensive quality program that starts in the design phase and proceeds through the manufacturing process. Optoelectronics modules are qualified to our internal standards using MIL-STD-883 test methods and procedures and using sampling techniques consistent with *Telcordia Technologies* ™ requirements. This qualification program fully meets the intent of *Telcordia Technologies* reliability practices TR-NWT-000468 for optoelectronic parts, and the transponder as a subsystem meets NEBS GR63-CORE requirements In addition, our design, development, and manufacturing facility has been certified to be in full compliance with the latest *ISO* ® 9001 quality system standards.

Electrostatic Discharge

CAUTION: This device is susceptible to damage as a result of electrostatic discharge. Take proper precautions during both handling and testing. Follow guidelines such as JEDEC Publication No. 108-A (Dec. 1988).

TriQuint employs a human-body model (HBM) for ESD-susceptibility testing and protection-design evaluation. ESD voltage thresholds are dependent on the critical parameters used to define the model. A standard HBM (resistance = 1.5 kΩ, capacitance = 100 pF) is widely used and can be used for comparison purposes.

Regulatory and Voluntary Compliance

Table 15. Regulatory and Voluntary Compliance

Feature	Standard	Test Parameters/Performance
Electrostatic Discharge (ESD) to the Electrical Pins	Sensitivity Classification: MIL-STD-883E, Method 3015.7	TBD
Electrostatic Discharge (ESD) to Housing and Optical Connector	EN 61000-4-2, *IEC*® 61000-4-2	Full recovery following ±8 kV contact discharge and ±15 kV air discharge
Electromagnetic Compatibility: Radiated Emissions	FCC Part 15, Class B EN55022, Class B GR-1089_CORE*	Full compliance within the frequency range of 10 KHz—20 GHz
Immunity	EN 61000-4-3 GR-1089_CORE*	Full compliance within the frequency range of 10 KHz—10 GHz at a field strength of 8.5 V/m
Safety of Information Technology Equipment	*IEC* 60950 EN 60950 *UL*® 60950 CAN/*CSA*®-C22.2 No. 60950	CB Scheme: Test Report Reference No. 01RT14477-02252002, Reference Certificate No. US/5754/*UL*, *UL*/*CSA* Recognition File No. E225949
Laser Safety	21 CFR 1040.10 and 1040.11, includes Laser Notice No. 50, *IEC* 60825-1:1993, A1:1997, and A2:2001	CDRH Accession No. (872009-59) AEL Class 1
CE Mark	LVD 73/23/EEC EMC 89/336/EEC	EC Declaration of Conformity
Component Recognition	*UL* and *CSA* Joint Component Recognition for Information Technology Equipment	*UL* File Number: E225949
Compositional Analysis	Standard ICPS, GC/MS, FTIR Analytical Processes	Analytical test results: TBD

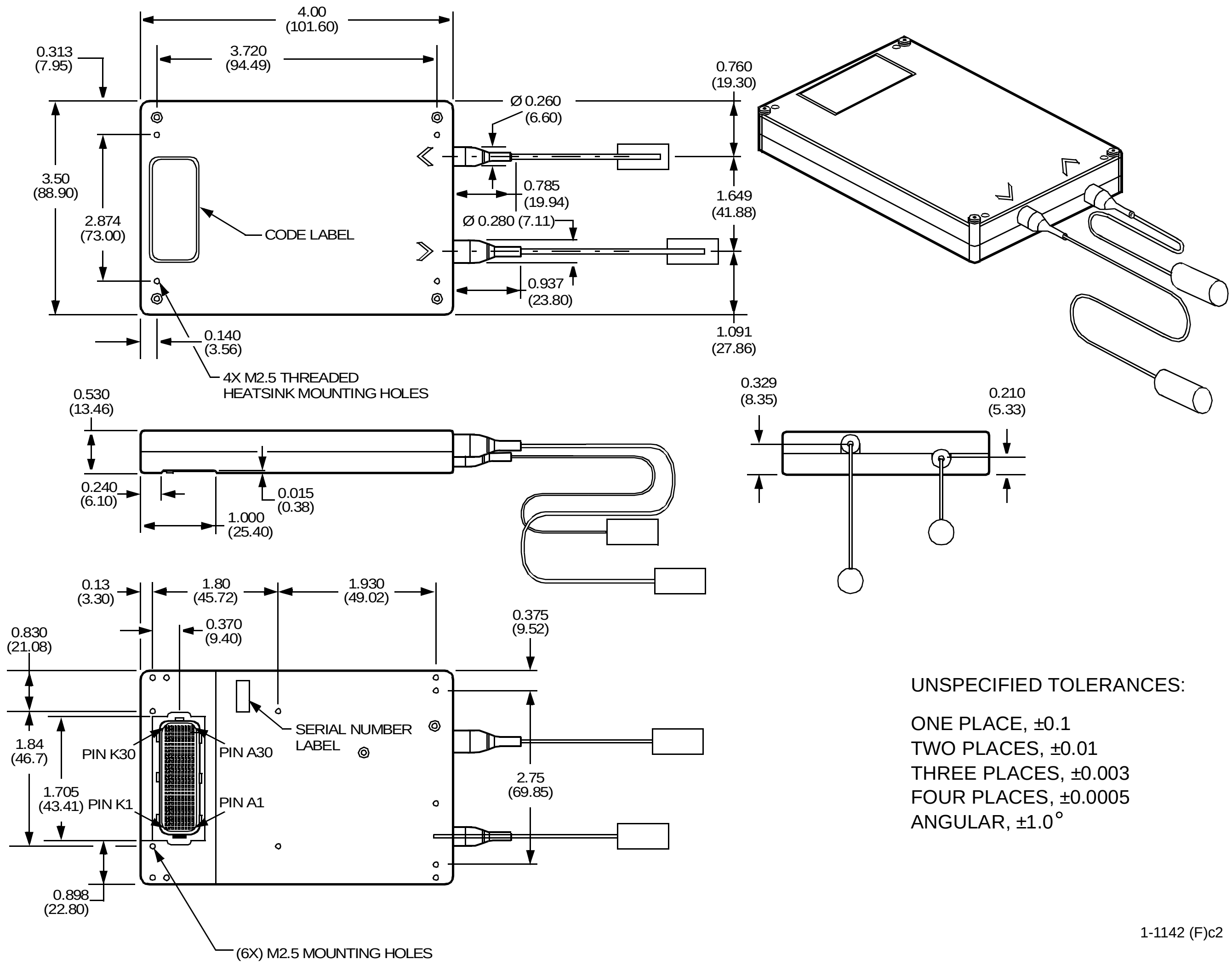
*Complies with applicable *Telcordia* NEBS Level 1—3 EMC requirements for components in a standalone configuration.

CAUTION: Use of controls, adjustments, and procedures other than those specified herein may result in hazardous laser radiation exposure.

NOTICE
Unterminated optical connectors can emit laser radiation.
Do not view with optical instruments.

Outline Diagram

Dimensions are in inches and (millimeters).



Notes:

Package properties:
— Material: aluminum alloy 6061-T6 per QQ-A-250/11.
— Finish: clear chromate (conductive) per MIL-C-5541, Class 3.

Four M2.5 threaded holes are to mount the transponder on the customer board:
—Transponder mounting holes (bottom cover): maximum screw depth = 0.071 in. (1.80 mm) (thread 0.080 in. [2 mm] deep).

Four M2.5 threaded holes are for possible mounting of an external heat sink:
— External heat sink mounting holes (top cover): maximum screw depth = 0.100 in. (2.54 mm) (thread 0.100 in. [2.54 mm] deep).

TriQuint Optoelectronics recommends that customers use a 300-pin plug FCI Berg #84500-102 (30 µin gold plated) that meets *Telcordia Technologies'* 100 insertions criterion.

TriQuint Optoelectronics also recommends that the distance between the Berg connector center-line and the nearest customer components behind the transponder be 0.8 in. minimum to ensure that future transponders are accommodated without any board layout change.

SC type optical connectors are standard on the CB64-Type.

The pigtails are 100 cm ± 10 cm in length (34.5 in. to 43.0 in.). A yellow sleeve *UL* ® approved (TBD, 94V-2) jacket is placed at the receiver end of the pigtail.

Figure 9. Mechanical Dimensions

Ordering Information

Table 16. Ordering Information

Reference Clock Filter	Wavelength (nm)	Code	Comcode
No Filter	1530—1565	CB64S2CAA	109120584
622 MHz VCO	1530—1565	CB6AS2CAA	109120592
155 MHz VCO	1530—1565	CB6BS2CAA	109120600
666 MHz VCO	1530—1565	CB6CS2CAA	109120618
166 MHz VCO	1530—1565	CB6DS2CAA	109120626

Additional Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

Web: www.triquint.com **Tel: (503) 615-9000**

E-mail: info_opto@tqs.com **Fax: (503) 615-8902**

For technical questions and additional information on specific applications:

E-mail: info_opto@tqs.com

TriQuint® OPTOELECTRONICS, INC.

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