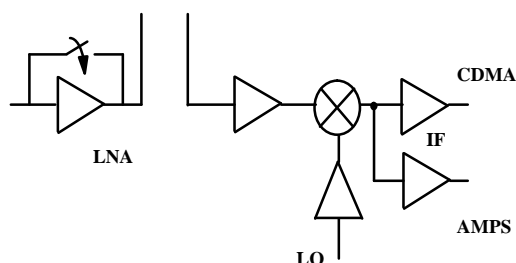


## Preliminary Datasheet

- High-Linearity, Cellular LNA/Mixer IC for use in TDMA and CDMA Mobile Phones
- Integrated bypass switch for LNA
- GaAs PHEMT Process
- Leadless 3.5 x 3.5 mm. SMT package
- LO Input power range: -12.0 to 0 dBm
- Operating voltage range: 2.7 to 4 V
- Total current consumption: 20 mA
- Adjustable Mixer Gain and IP3



ESD: Electrostatic discharge sensitive device  
Observe handling Precautions!

Type	Marking	Ordering code (tape and reel)	Package
CMH82	H82	TBD	VQFN-20

Maximum Ratings	Symbol	Value		Unit
		min	max	
Supply Voltage	V <sub>DD</sub>	0	4	V
DC-Voltage at RF Ports	V <sub>RF</sub>	- 0.3	0.3	V
DC-Voltage at GND Ports	V <sub>GND</sub>	- 0.3	0.3	V
DC-Voltage at CNTL Ports	V <sub>CNTL</sub>	0	0.3 + V <sub>DD</sub>	V
Power into LO Input	P <sub>in,LO</sub>		10	dBm
Operating Temperature	T <sub>a</sub>	-40	85	°C
Channel Temperature	T <sub>Ch</sub>		150	°C
Storage Temperature	T <sub>stg</sub>	-55	150	°C

Thermal Resistance			
Channel to Soldering Point (GND)	R <sub>thChS</sub>	102	°C /W

## Electrical Characteristics

Parameter,	min	typ	max	Unit
RF - Frequency	869	-	894	MHz
LO - Frequency <sup>(1)</sup>	919	-	1194	MHz
IF Frequency range	50	-	300	MHz
LO Power Input	-12.0	-	0.0	dBm
Supply Voltage (Vdd)	2.7	-	4.0	V
High Logic Level (H)	2.4	2.7	0.3 + V <sub>DD</sub>	V
Low Logic Level (L)	0.0	-	0.3	V

1) Low-side LO can be achieved using external tuning

## LNA – Performance of LNA:

Test conditions:  $T_a = 25^\circ\text{C}$ ,  $V_{DD} = 2.7\text{ V}$ ,  $f_{RF} = 869 - 894\text{ MHz}$

Mode – High Gain, High Linearity	min	typ	max	Unit
Operating Current		6.5		mA
Noise Figure		1.1		dB
Gain		12.5		dB
Input / Output return loss		10		dB
3rd Order Input Intercept Point		10.0		dBm
Mode – High Gain, Reduced Current	min	typ	max	Unit
Operating Current		4.5		mA
Noise Figure		1.2		dB
Gain		12.3		dB
Input / Output return loss		10		dB
3rd Order Input Intercept Point		8.0		dBm
Mode – Low Gain, By-Pass Mode	min	typ	max	Unit
Operating Current		0		mA
Noise Figure		4.5		dB
Gain		-4.5		dB
Input / Output return loss		10		dB
3rd Order Input Intercept Point		25		dBm

**MIXER - Electrical Characteristics of Mixer section**

**Test conditions:**  $T_a = 25^{\circ}\text{C}$ ;  $V_{DD} = 2.7\text{V}$ ,  $P_{LO} = -10\text{ dBm}$ ,  $f_{LO} = f_{RF} + f_{IF}$ ,  $f_{IF} = 85\text{MHz}$

<b>Mode – High Gain, High Linearity CDMA</b>	<b>min</b>	<b>typ</b>	<b>max</b>	<b>Unit</b>
Operating Current		13.5		mA
Conversion Gain <sup>(1)</sup>		15.5		dB
Noise Figure		4.5		dB
3rd Order Input Intercept Point		6.5		dBm
RF Input return loss		10		dB
LO Input return loss		10		dB
IF Output Impedance <sup>(2)</sup>		695+j*135		$\Omega$
<b>Mode – Reduced Current CDMA</b>	<b>min</b>	<b>typ</b>	<b>max</b>	<b>Unit</b>
Operating Current		11.0		mA
Conversion Gain <sup>(1)</sup>		15.2		dB
Noise Figure		4.7		dB
3rd Order Input Intercept Point		4.5		dBm
RF Input return loss		10		dB
LO Input return loss		10		dB
IF Output Impedance <sup>(2)</sup>		695+j*135		$\Omega$
<b>Mode – AMPS</b>	<b>min</b>	<b>typ</b>	<b>max</b>	<b>Unit</b>
Operating Current		11		mA
Conversion Gain		13.5		dB
Noise Figure		5.7		dB
3rd Order Input Intercept Point		2.5		dBm
RF Input return loss		10		dB
LO Input return loss		10		dB
IF Output Impedance <sup>(2)</sup>		172+j*78		$\Omega$

1) CDMA Mixer Gain may be varied from approximately 10 to 20 dB (typical) by choice of external components. See notes.

2) IF Output externally tuned to desired impedance

**FULL CHAIN – LNA / Downconverter Characteristics**

**Test conditions:**  $T_a = 25\text{ }^{\circ}\text{C}$ ,  $V_{DD} = 2.7\text{ V}$ ,  $P_{LO} = -10\text{ dBm}$ ,  $f_F = 85\text{ MHz}$

<b>Mode – High Gain, High Linearity CDMA</b>	<b>min</b>	<b>typ</b>	<b>max</b>	<b>Unit</b>
Total operating Current		20		mA
Conversion Gain <sup>(1)</sup>		25		dB
Noise Figure		1.9		dB
Input IP3		-3.5		dBm
LNA Input IP3		10.0		dBm
<b>Mode – High Gain, Reduced Current CDMA</b>	<b>min</b>	<b>typ</b>	<b>max</b>	<b>Unit</b>
Total operating Current		15.5		mA
Conversion Gain <sup>(1)</sup>		24.5		dB
Noise Figure		2.0		dB
Input IP3		-5		dBm
LNA Input IP3		8.0		dBm
<b>Mode – Low Gain (LNA bypass) CDMA<sup>(2)</sup></b>	<b>min</b>	<b>typ</b>	<b>max</b>	<b>Unit</b>
Total operating Current		11.0		mA
Conversion Gain <sup>(1)</sup>		7.7		dB
Noise Figure		12.0		dB
Input IP3		11.5		dBm
<b>Mode – AMPS<sup>(2)</sup></b>	<b>min</b>	<b>typ</b>	<b>max</b>	<b>Unit</b>
Total operating Current		15.5		mA
Conversion Gain <sup>(1)</sup>		22.8		dB
Noise Figure		2.3		dB
Input IP3		-6.5		dBm

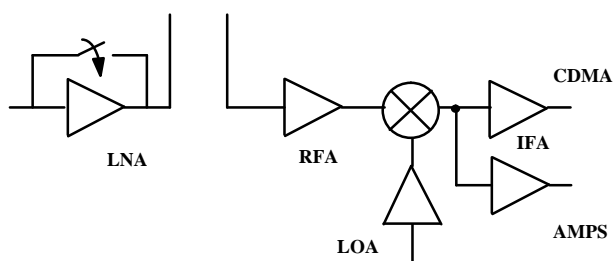
1) Assumes 3 dB loss for image filter

2) Assumes reduced current mode

**Truth Table**

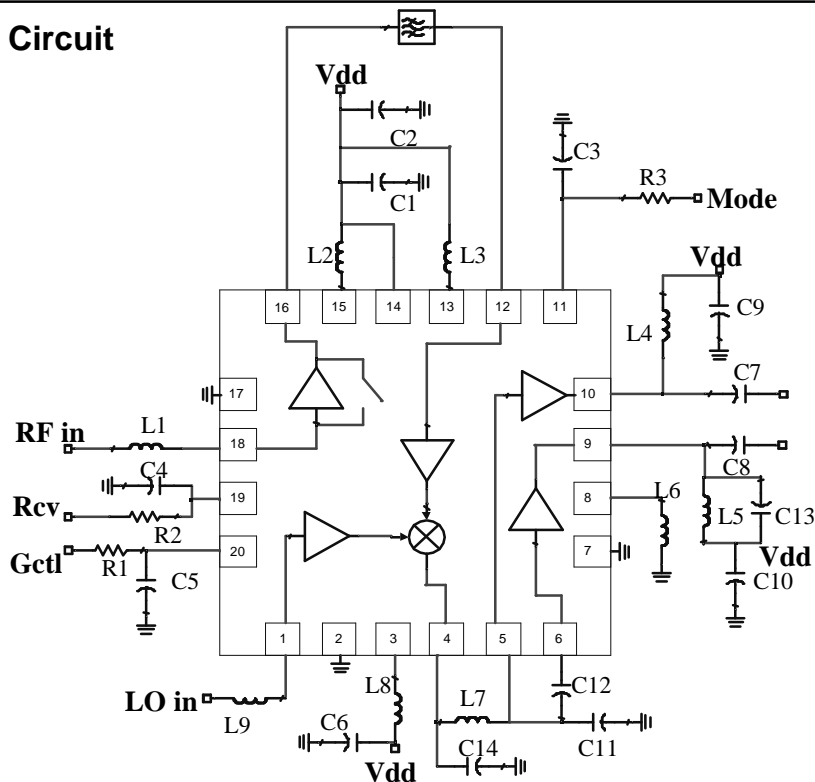
Operating Mode	Control Voltage		
	Mode Ctl	Gain Ctl	Rcv Only
High Gain & Linearity	H	H	H
High Gain, Low Current	H	H	L
Low Gain (LNA bypass)	H	L	L
AMPS	L	H	L

**PIN Assignments & Functional Block Diagram**



PIN	Symbol	Description
1	LO in	Mixer LO Input
2	GND	Ground
3	LO Vdd	Supply voltage for LO Buffer Amp
4	Mix out	Mixer output to IF Amplifier
5	AMPS in	AMPS IF Amplifier input
6	CDMA in	CDMA IF Amplifier input
7	GND	Ground
8	lfa src	IF Amplifier FET source ground
9	CDMA out	CDMA IF output
10	AMPS out	AMPS IF output
11	Mode	AMPS or CDMA IF mode control
12	RFA in	Downconverter input from image filter
13	RFA Vdd	Supply voltage for RFA
14	Vdd	Supply voltage
15	LNA Vdd	Supply voltage for LNA
16	LNA out	Output of LNA
17	GND	Ground
18	LNA in	RF Input to LNA
19	Rcv	Reduced current mode control
20	Gctl	Control voltage for LNA gain selection

## Application Circuit



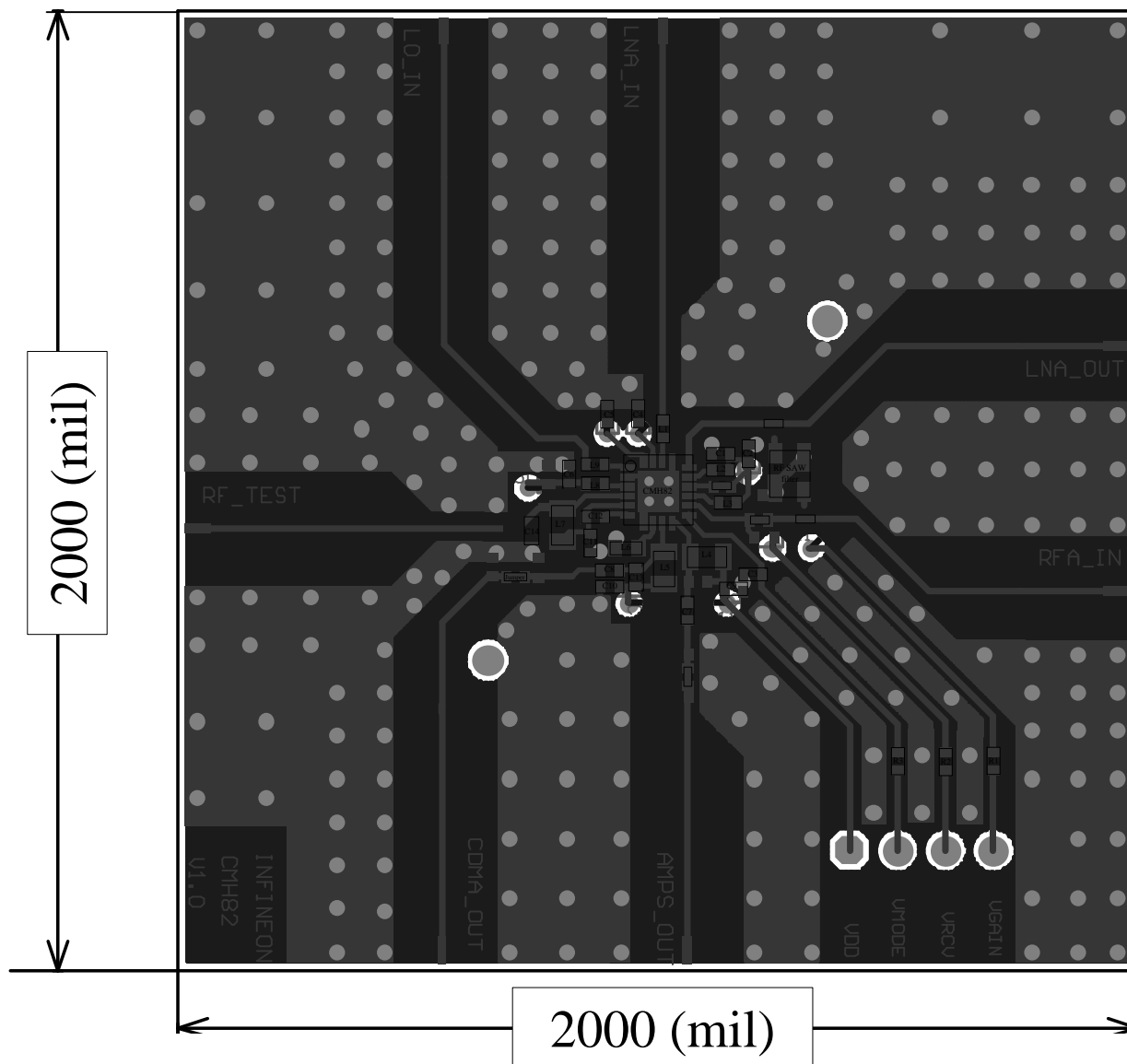
## External Components

Component values for IF = 85 MHz. LO = RF + IF .

Component	Description	Package Type	Component	Description	Package Type
C1	CAP, 47 PF	0402	L1	IND, 19 NH	0402
C2	CAP, 10K PF	0402	L2	IND, 12 NH	0402
C3	CAP, 100 PF	0402	L3	IND, 12 NH	0402
C4	CAP, 47 PF	0402	L4	IND, 330 NH	0805
C5	CAP, 47 PF	0402	L5	IND, 270 NH	0603
C6	CAP, 1000 PF	0402	L6	IND, 220 NH	0603
C7	CAP, 18 PF	0402	L7	IND, 270 NH	0603
C8	CAP, 10 PF	0402	L8	IND, 18 NH	0402
C9	CAP, 10K PF	0402	L9	IND, 12 NH	0402
C10	CAP, 10K PF	0402			
C11	CAP, 12 PF	0402	R1	RES, 47 KOHM	0402
C12	CAP, 100 PF	0402	R2	RES, 47 KOHM	0402
C13	CAP, 3.3 PF	0402	R3	RES, 47 KOHM	0402
C14	CAP, 0.5 PF	0402			

Figure 1: Dimensional drawings of the 20x0.08mm probe tip. The figure includes three views: a top view, a side view, and a cross-sectional view. The top view shows a square tip with a central circular feature, with dimensions 3.5±0.1, 3.3, 3.3, and 3.5±0.1. The side view shows the tip's profile with a 12° angle and a 0.9 MAX. height. The cross-sectional view shows the internal structure with dimensions 5 x 0.5 = 2.5, 0.5, 0.55±0.07, 1.9, 2.4, 1.9, 2.4, 0.25±0.05, and 20x. The cross-section also includes a table with columns A, B, and C, and a row with values 0.05, 0.05, and 0.05.

**Evaluation Board**





## CMH82 – Application Information

### DC Biasing:

#### Supply Voltage.

One regulated voltage source is needed for CMH82. On the evaluation board, it is labeled VDD.

#### Minimum LO Power for Proper Biasing

For proper biasing of the CMH82, a minimum LO input power is required. If the part is turned ON without any LO drive applied, all currents will be extremely high. The minimum LO required is approximately –12 dBm. Operation with LO input powers below the minimum value causes the current to increase in all amplifier stages. For higher LO input power levels the current stays relatively constant over a wide range of LO powers. Proper matching of the LO amplifier is also important to achieve the lowest current consumption and to minimize the required LO input power.

#### Adjustable Current Level

The CMH82 can operate in two different current/linearity modes: High Linearity (with higher current) and Reduced Current (lower linearity). To operate with reduced current the voltage on pin 19 (RCV) should be set LOW. Some additional current reduction can be achieved by reducing the voltage at pin 14 by inserting a resistor between VDD and pin 14. The current pulled by pin 14 is approximately 1 mA. Higher currents can be realized by using a higher VDD voltage.

### Tuning LO and IF Amplifiers:

The CMH82 can be tuned to utilize either high or low side LO frequencies and allows a wide range of IF frequencies. Depending on the chosen frequency plan the off chip components for the LO and IF amplifiers will need to be optimized. An application circuit with all component values is provided for high side LO injection with IF frequency of 85 MHz (RF freq 869 – 894 MHz).

Two external components (L9 and L8) are required for tuning the LO. L8 is critical for setting the minimum current and to achieve the constant DC current over the operating band. L9 sets the input match.

Components L7, C11 and C12 form the input match for the IF amplifiers and will vary depending on the chosen IF frequency. The inductor on pin 8 allows adjustment to the gain of the IF amplifiers. Output matching components shown in the application circuit provide a transformation for a 50 Ohm load impedance. The output impedance for the CDMA IFA (looking into pin 9) at 85 MHz is approximately  $(695 + j*135)$  Ohms. The AMPS output impedance is approximately  $(172 + j*78)$  Ohms at 85 MHz.

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### Downconverter Gain Adjustment:

The **Downconverter gain can be adjusted by changing the source feedback inductor L6 for the IFA**. Higher inductance will give lower downconverter gain and typically improve the IIP3.

### Gain/Current Control Pins:

LOW = 0 to 0.3 V

HIGH = Vdd to (Vdd – 0.3) V

VGAIN – select between high and low gain states in the LNA.

VGAIN = HIGH : LNA ON (~12 dB Gain, ~ 6 mA current)

VGAIN = LOW : LNA bypassed (~ 4 dB Loss, no current)

VRCV - selects Current/Linearity mode (changes current in LNA/RFA/IFA)

VRCV = LOW selects Reduced Current Mode

VRCV = HIGH selects High Linearity Mode.

VMODE - selects which IF amplifier is ON

VMODE = LOW selects AMPS mode

VMODE = HIGH selects CDMA mode

### Other Notes:

Inductor L1 is critical for setting the Noise Figure of the LNA. A high Q wire wound inductor (e.g. Coilcraft) is recommended to achieve minimum NF.

LNA current can be determined by subtracting the current in Low Gain mode from the current in High Gain mode (keeping VRCV and VMODE constant).

Capacitor C14 can be eliminated if a slightly higher (~0.5 dB) downconverter noise figure is tolerable.

Control lines (G\_CNTL, VRCV and VMODE) have an input impedance of > 1 M $\Omega$  when Vdd is ON. When VDD is off, they have approximately 20 K $\Omega$  input impedance.