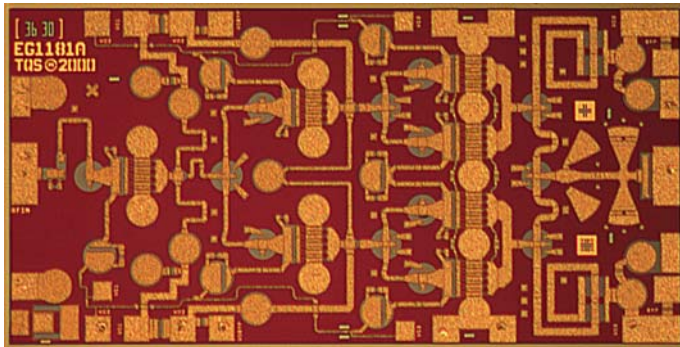


27 - 32 GHz 1W Power Amplifier

TGA1172-SCC



Chip Dimensions 2.7 mm x 1.4 mm x 0.1mm

Product Description

The TriQuint TGA1172-SCC is a three stage HPA MMIC design using TriQuint's proven 0.25 μ m Power pHEMT process. The TGA1172 is designed to support a variety of millimeter wave applications including point-to-point digital radio and LMDS/LMCS and Ka band satellite ground terminals.

The three stage design consists of a 600 μ m input stage driving a 2 x 600 μ m interstage followed by a 4 x 600 μ m output stage.

The TGA1172 provides 29 dBm nominal output power at 1dB compression across 27-32GHz. Typical small signal gain is 16 dB with typical Input/Output Return Loss of <-10dB.

The TGA1172 requires minimum off-chip components. Each device is 100% DC and RF tested on-wafer to ensure performance compliance. The device is available in chip form.

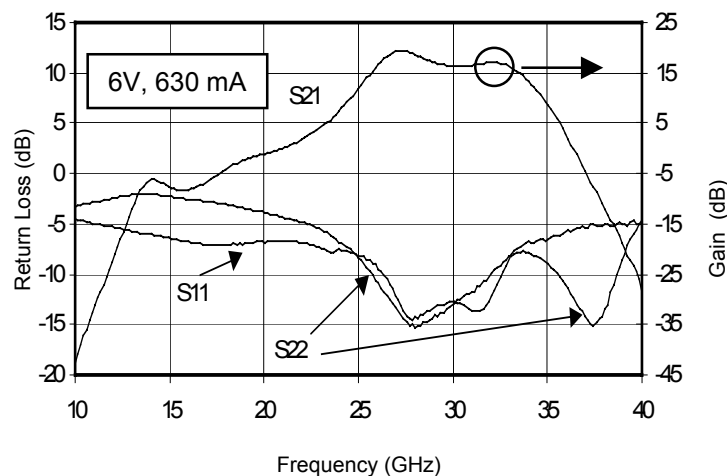
Key Features

- 0.25 μ m pHEMT Technology
- 16 dB Nominal Gain
- 29 dBm Nominal P1dB
- 36dBm OTOI typical at 28GHz
- Nominal Input/Output RL < -10 dB
- Bias 6 - 7V @ 630 mA

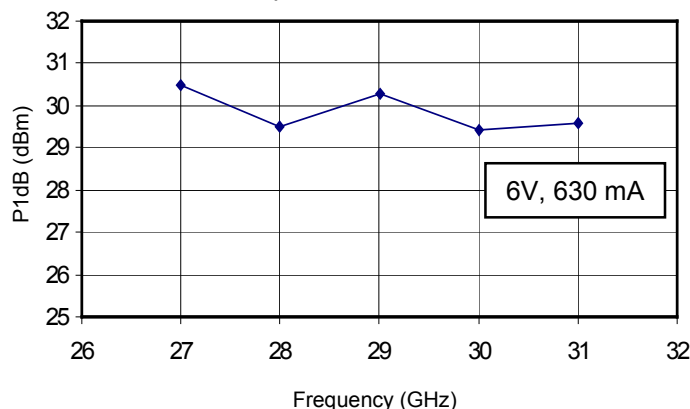
Primary Applications

- Point-to-Point Radio
- Point-to-Multipoint Communications
- Ka Band Sat-Com

Wideband Small Signal Gain



Output Power at P1dB



Output Third Order Intercept

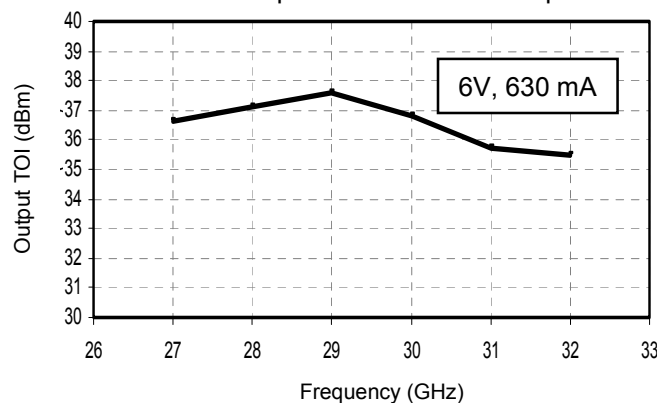


TABLE I
MAXIMUM RATINGS

SYMBOL	PARAMETER 4/	VALUE	NOTES
V ⁺	POSITIVE SUPPLY VOLTAGE	8 V	
I ⁺	POSITIVE SUPPLY CURRENT	840 mA	1/
I ⁻	NEGATIVE SUPPLY CURRENT	35.2 mA	1/
P _{IN}	INPUT CONTINUOUS WAVE POWER	23 dBm	
P _D	POWER DISSIPATION	5.0 W	
T _{CH}	OPERATING CHANNEL TEMPERATURE	150 °C	2/ 3/
T _M	MOUNTING TEMPERATURE (30 SECONDS)	320 °C	
T _{STG}	STORAGE TEMPERATURE	-65 to 150 °C	

- 1/ Total current for all stages.
- 2/ These ratings apply to each individual FET.
- 3/ Junction operating temperature will directly affect the device median time to failure (T_M). For maximum life, it is recommended that junction temperatures be maintained at the lowest possible levels.
- 4/ These ratings represent the maximum operable values for the device.

TABLE II
DC SPECIFICATIONS (100%)
(T_A = 25 °C Nominal)

NOTES	SYMBOL	TEST CONDITIONS 2/	LIMITS		UNITS
			MIN	MAX	
	I _{DSS1}	STD	60	282	mA
	G _{M1}	STD	132	318	mS
1/	V _{P1}	STD	0.5	1.5	V
1/	V _{P2-3}	STD	0.5	1.5	V
1/	V _{P4-7}	STD	0.5	1.5	V
1/	V _{BVGD1}	STD	13	30	V
1/	V _{BVGD2-3}	STD	13	30	V
1/	V _{BVGD4-7}	STD	13	30	V
1/	V _{BVGS1}	STD	13	30	V
1/	V _{BVGS2-3}	STD	13	30	V
1/	V _{BVGS4-7}	STD	13	30	V

- 1/ V_P, V_{BVGD}, and V_{BVGS} are negative.
- 2/ The measurement conditions are subject to change at the manufacture's discretion (with appropriate notification to the buyer).

TABLE IV
RF SPECIFICATIONS
(T_A = 25°C Nominal)

NOTE	TEST	MEASUREMENT CONDITIONS 6V @ 630mA	VALUE			UNITS
			MIN	TYP	MAX	
	SMALL-SIGNAL GAIN MAGNITUDE	27 – 32 GHz	13	16		dB
	POWER OUTPUT AT 1 dB GAIN COMPRESSION	28 – 32 GHz	27	29		dBm
	INPUT RETURN LOSS MAGNITUDE	27 – 32 GHz		10		dB
	OUTPUT RETURN LOSS MAGNITUDE	27 – 32 GHz		10		dB
	OUTPUT THIRD ORDER INTERCEPT	28 GHz		36		dBm

TABLE V
RELIABILITY DATA

PARAMETER	BIAS CONDITIONS		P _{DISS} (W)	R _{θJC} (C/W)	T _{CH} (°C)	T _M (HRS)
	V _D (V)	I _D (mA)				
R _{θJC} Thermal resistance (channel to backside of carrier plate)	6	630	3.78	21.35	135.7	3.5E6

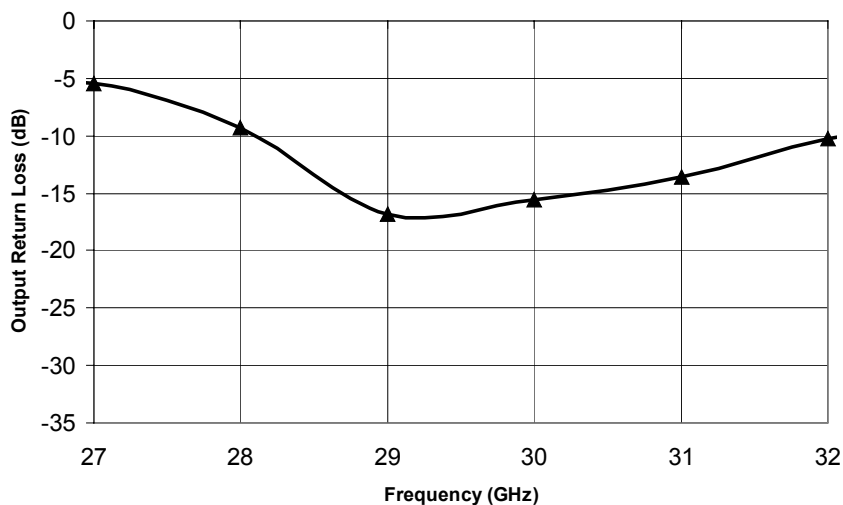
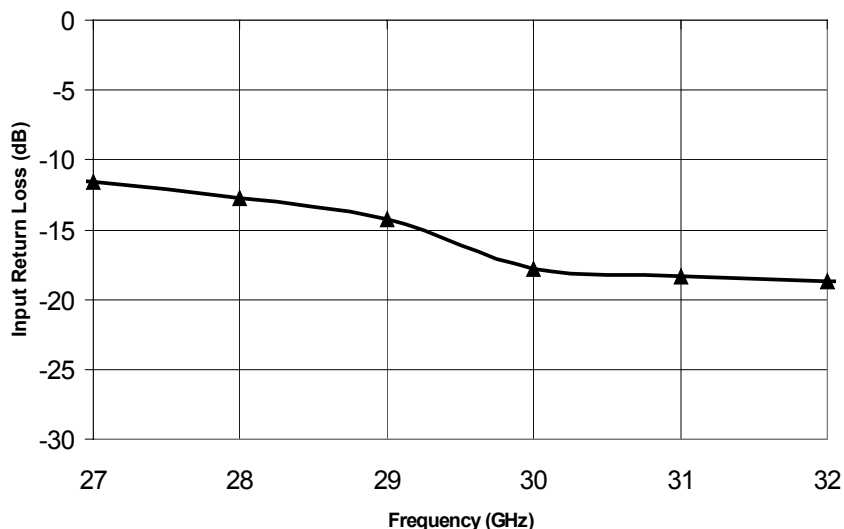
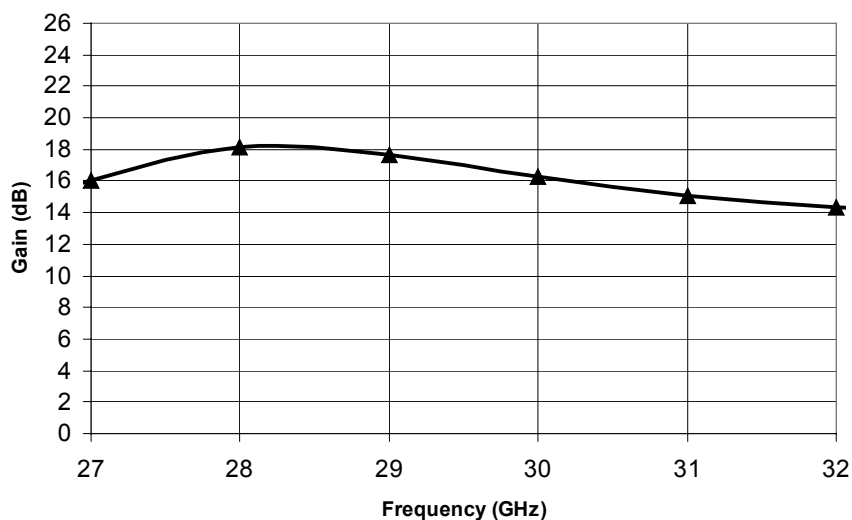
Note: Assumes eutectic attach using 1.5 mil 80/20 AuSn mounted to a 20 mil CuMo Carrier at 55°C baseplate temperature. Worst case condition with no RF applied, 100% of DC power is dissipated.

TriQuint Recommends the TGA4509-EPU be used for New Designs

TGA1172 Average On-Wafer Small Signal S-Parameters

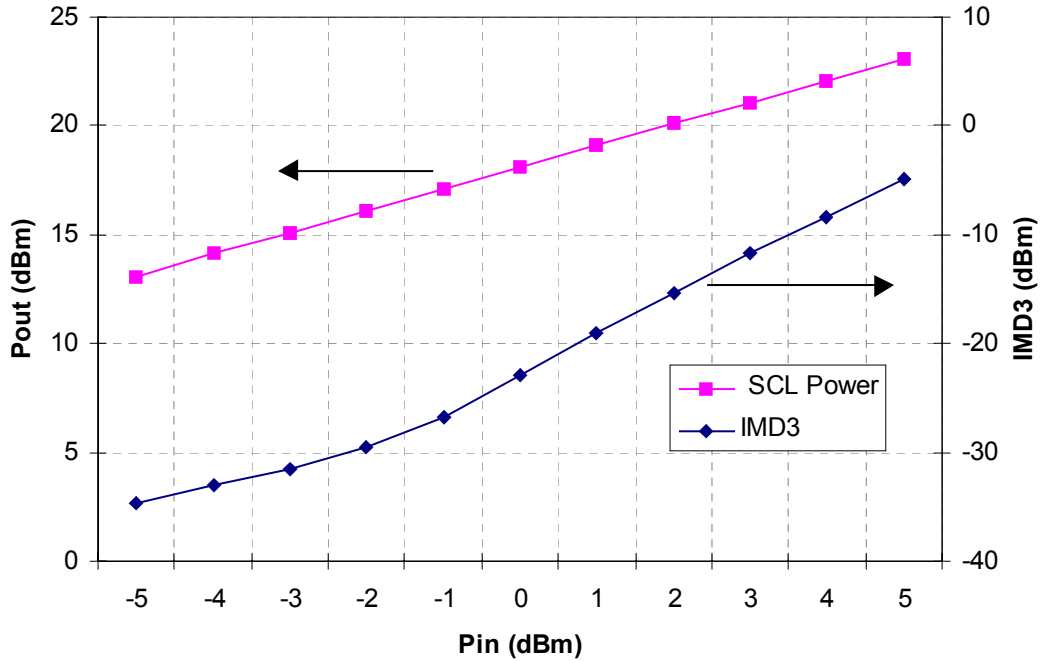
Sample Size = 23K devices

TGA1172-SCC



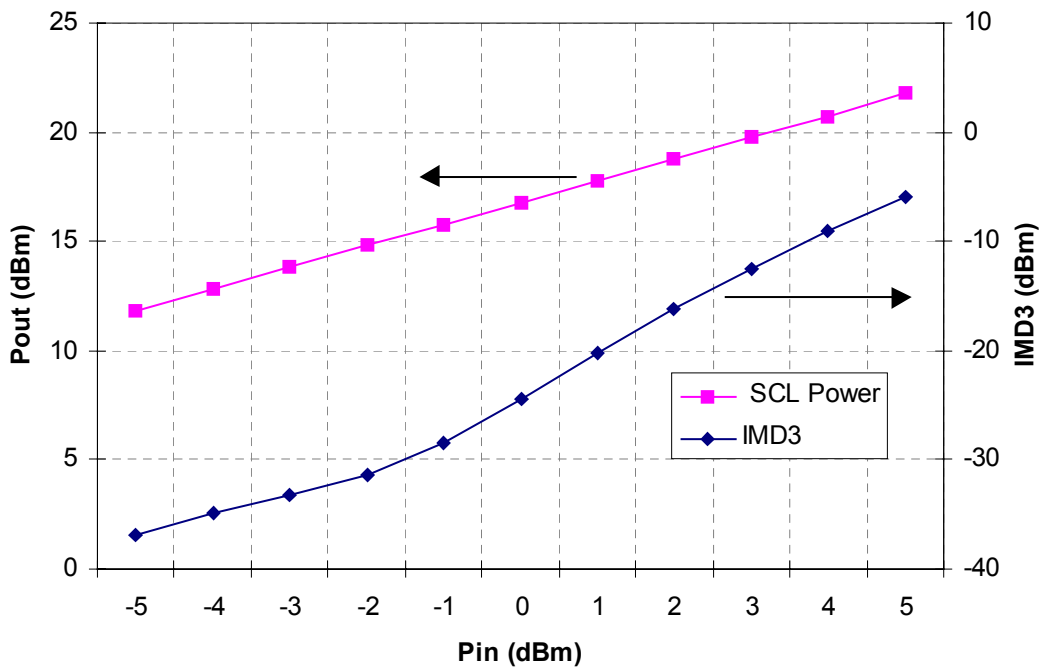
TGA1172 Single tone pout and IMD3 vs Pin

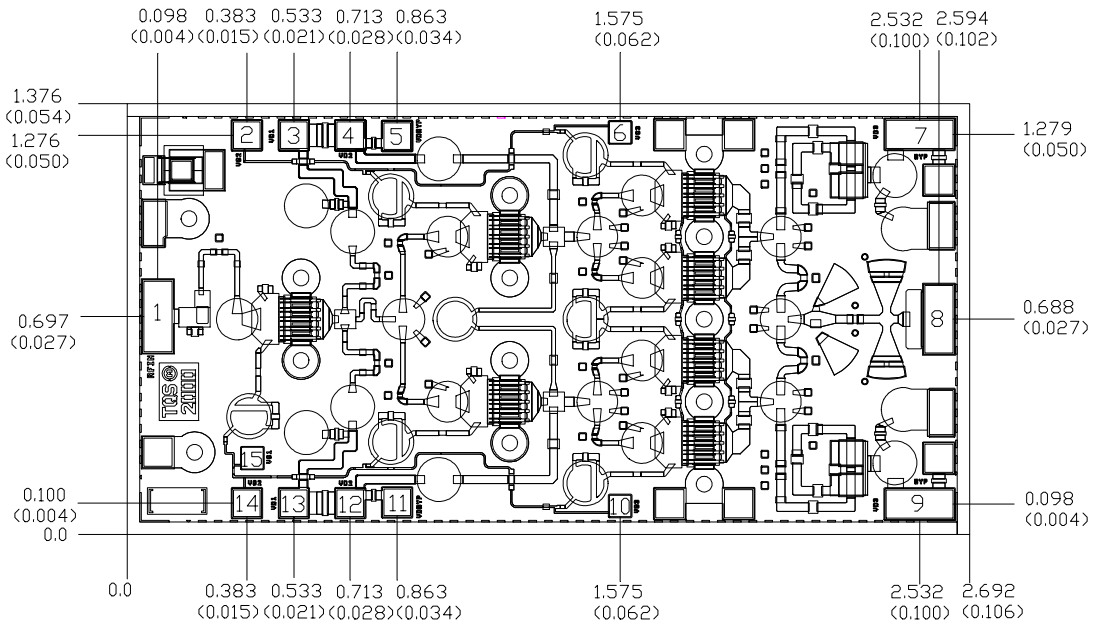
Frequency = 28GHz, 6V, 630 mA



TGA1172 Single tone pout and IMD3 vs Pin

Frequency = 31GHz, 6V, 630 mA





Units: millimeters (inches)

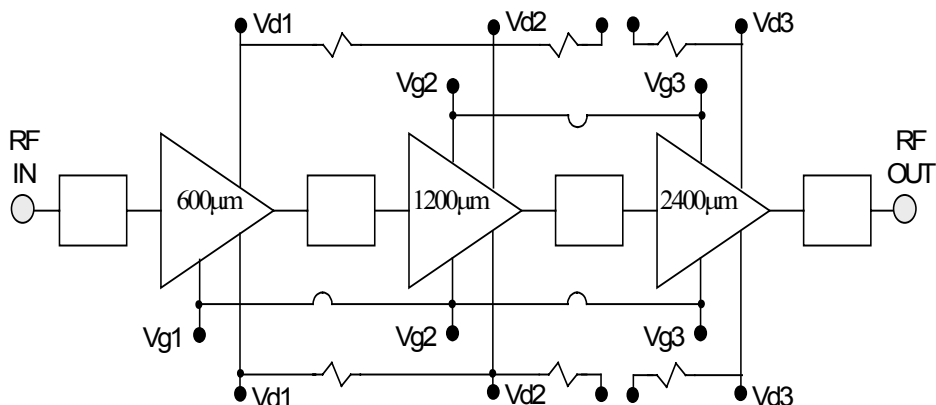
Thickness: 0.1016 (0.004)

Chip edge to bond pad dimensions are shown to center of bond pad

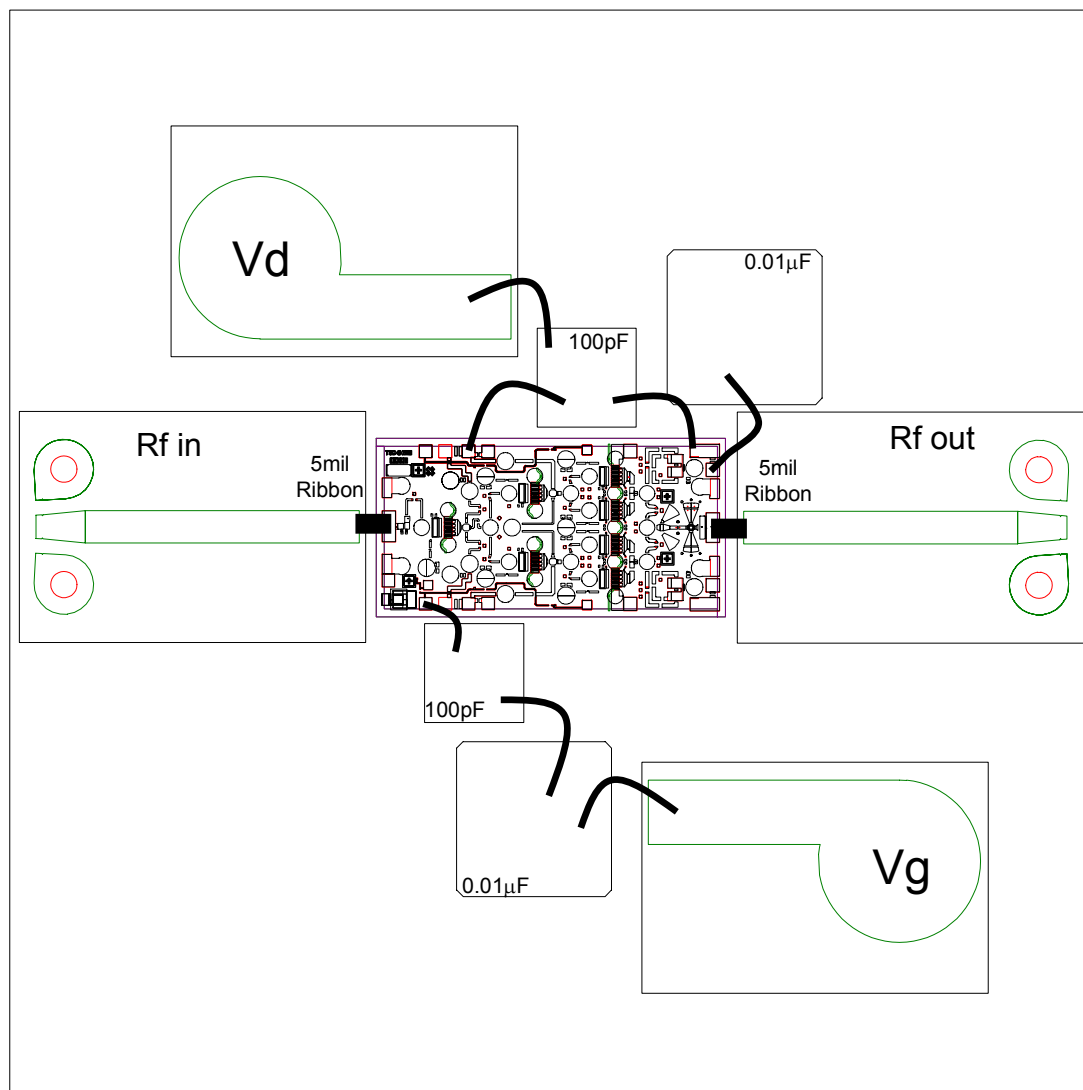
Chip size tolerance: +/- 0.051 (0.002)

Bond Pad #1 (RF Input)	0.105 x 0.240 (0.004 x 0.009)
Bond Pad #2,#14 (VG2)	0.100 x 0.100 (0.004 x 0.004)
Bond Pad #3,#13 (VD1)	0.100 x 0.100 (0.004 x 0.004)
Bond Pad #4,#12 (VD2)	0.100 x 0.100 (0.004 x 0.004)
Bond Pad #5,#11 (VDBYP)	0.100 x 0.100 (0.004 x 0.004)
Bond Pad #6,#10 (VG3)	0.075 x 0.075 (0.003 x 0.003)
Bond Pad #7,#9 (VD3)	0.105 x 0.228 (0.004 x 0.009)
Bond Pad #8 (RF Output)	0.100 x 0.225 (0.004 x 0.009)
Bond Pad #15 (VG1)	0.075 x 0.075 (0.003 x 0.003)

Mechanical Drawing



Amplifier Topology



Chip Assembly and Bonding Diagram

Assembly Process Notes

Reflow process assembly notes:

- Use AuSn (80/20) solder with limited exposure to temperatures at or above 300°C.
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- No fluxes should be utilized.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.
- Organic attachment can be used in low-power applications.
- Curing should be done in a convection oven; proper exhaust is a safety concern.
- Microwave or radiant curing should not be used because of differential heating.
- Coefficient of thermal expansion matching is critical.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonics are critical parameters.
- Aluminum wire should not be used.
- Discrete FET devices with small pad sizes should be bonded with 0.0007-inch wire.
- Maximum stage temperature is 200°C.