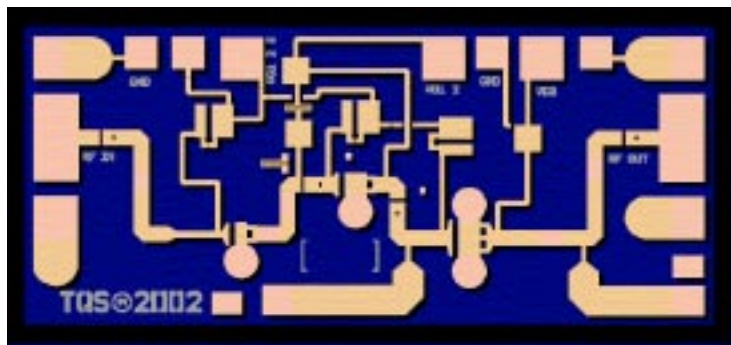


## Ka Band Low Noise Amplifier

## TGA4508

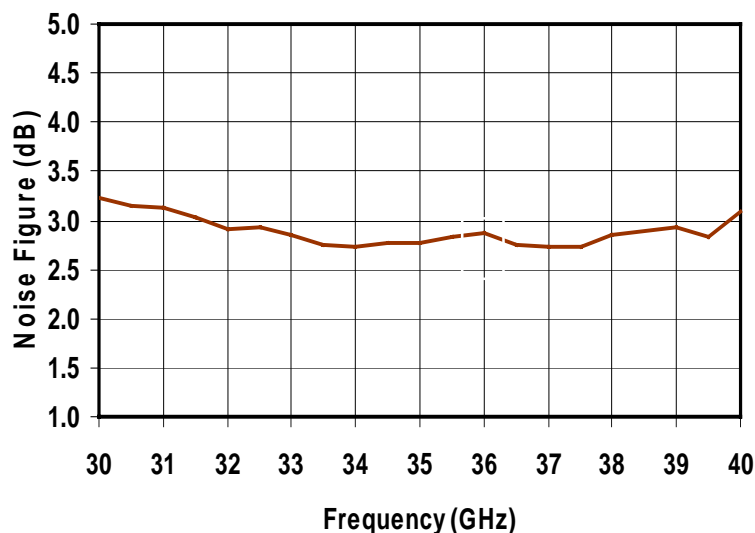
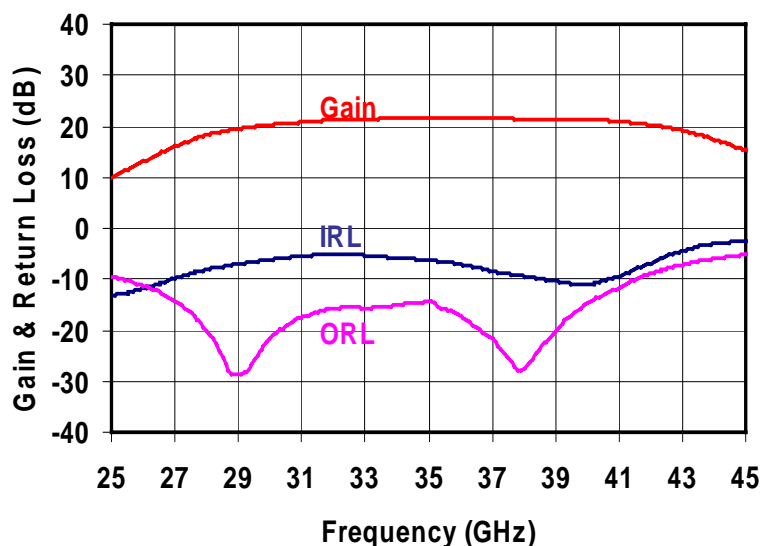


### Key Features

- Typical Frequency Range: 30 - 42 GHz
- 21 dB Nominal Gain
- 2.8 dB Nominal Noise Figure
- 14 dBm Nominal P1dB @ 38 GHz
- Bias 3 V, 40mA
- 0.15 um 3MI pHEMT Technology
- Chip Dimensions 1.7 x 0.8 x 0.1 mm  
(0.067 x 0.031 x 0.004) in

### Preliminary Measured Data

Bias Conditions:  $V_d = 3\text{ V}$ ,  $I_d = 40\text{ mA}$



### Primary Applications

- Point-to-Point Radio
- Point-to-MultiPoint Radio
- Ka Band VSAT

*Note: Devices designated as EPU are typically early in their characterization process prior to finalizing all electrical and process specifications. Specifications are subject to change without notice*

**TABLE I**  
**MAXIMUM RATINGS 1/**

SYMBOL	PARAMETER	VALUE	NOTES
V <sup>+</sup>	Positive Supply Voltage	5 V	<u>2/</u>
V <sub>G1</sub>	Gate 1 Supply Voltage Range	-1 V TO 0 V	
I <sup>+</sup>	Positive Supply Current	190 mA	<u>2/</u>
I <sub>G</sub>	Gate Supply Current	6 mA	
P <sub>IN</sub>	Input Continuous Wave Power	12 dBm	<u>2/</u>
P <sub>D</sub>	Power Dissipation	0.37 W	<u>2/</u> , <u>3/</u>
T <sub>CH</sub>	Operating Channel Temperature	117 °C	<u>4/</u> , <u>5/</u>
T <sub>M</sub>	Mounting Temperature (30 Seconds)	320 °C	
T <sub>STG</sub>	Storage Temperature	-65 to 117 °C	

- 1/ These ratings represent the maximum operable values for this device.
- 2/ Current is defined under no RF drive conditions. Combinations of supply voltage, supply current, input power, and output power shall not exceed P<sub>D</sub>.
- 3/ When operated at this power dissipation with a base plate temperature of 70 °C, the median life is 1 E+6 hours.
- 4/ Junction operating temperature will directly affect the device median time to failure (T<sub>M</sub>). For maximum life, it is recommended that junction temperatures be maintained at the lowest possible levels.
- 5/ These ratings apply to each individual FET.

**TABLE II**  
**DC PROBE TESTS**  
(T<sub>a</sub> = 25 °C, Nominal)

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNITS
V <sub>BVGS3</sub>	Breakdown Voltage gate-source	-30	-5	V
V <sub>BVGD3</sub>	Breakdown Voltage gate-drain	-30	-5	V
V <sub>P1,2,3</sub>	Pinch-off Voltage	-1.0	-0.1	V

Q1 is 100 um FET, Q2 is 200 um FET, Q3 is 300 um FET

**TABLE III**  
**ELECTRICAL CHARACTERISTICS**  
(Ta = 25 °C, Nominal)

PARAMETER	TYPICAL	UNITS
Drain Voltage, Vd	3	V
Drain Current, Id	40	mA
Gate Voltage, Vg	-0.5 to 0	V
Small Signal Gain, S21	21	dB
Input Return Loss, S11	8	dB
Output Return Loss, S22	15	dB
Noise Figure, NF	2.8	dB
Output Power @ 1 dB Compression Gain @ 38 GHz, P1dB	14	dBm

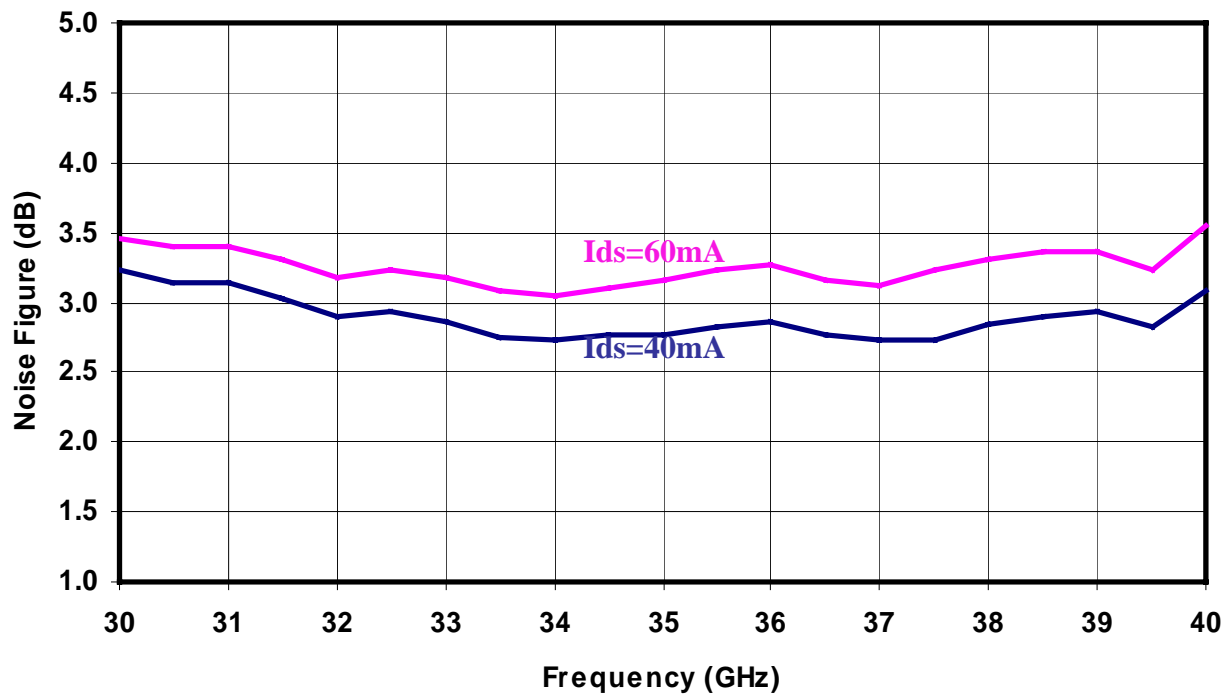
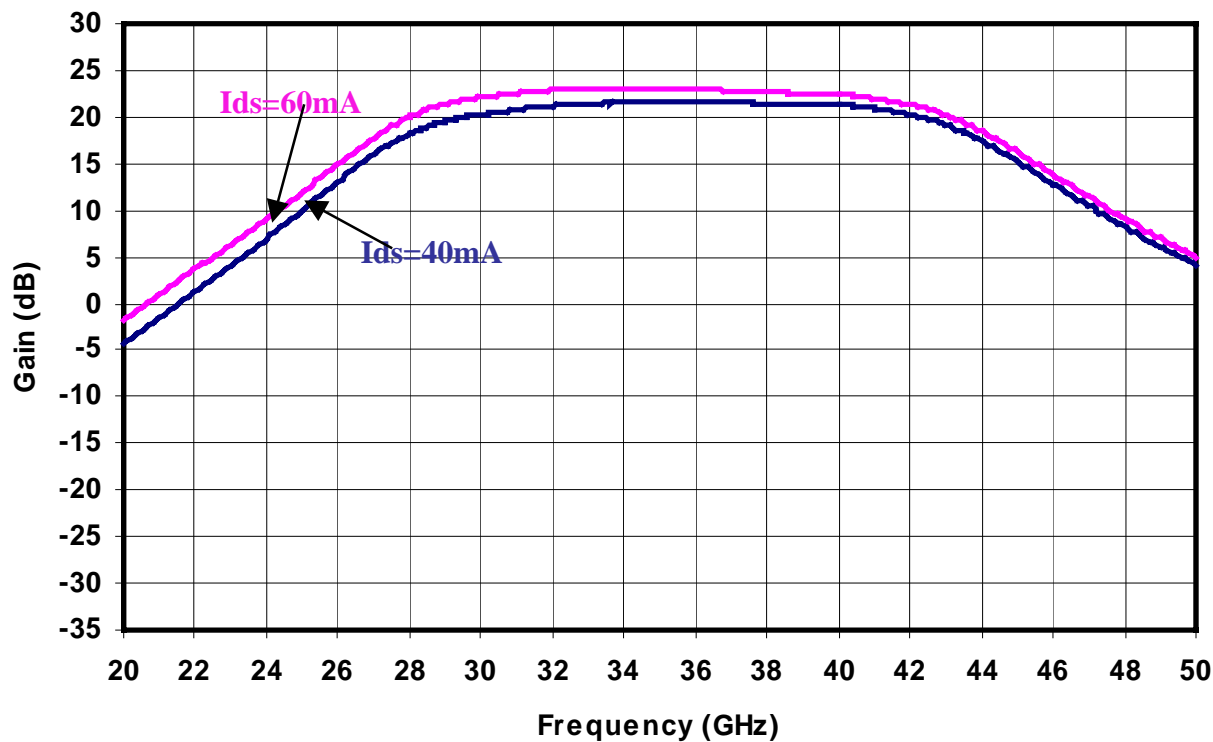
**TABLE IV**  
**THERMAL INFORMATION\***

PARAMETER	TEST CONDITIONS	T <sub>CH</sub> (°C)	R <sub>θJC</sub> (°C/W)	T <sub>M</sub> (HRS)
R <sub>θJC</sub> Thermal Resistance (channel to backside of carrier)	Vd = 3 V I <sub>D</sub> = 40 mA Pdiss = 0.12 W	85	125	2.2 E+13

Note: Assumes eutectic attach using 1.5 mil 80/20 AuSn mounted to a 20 mil CuMo Carrier at 70°C baseplate temperature. Worst case condition with no RF applied, 100% of DC power is dissipated.

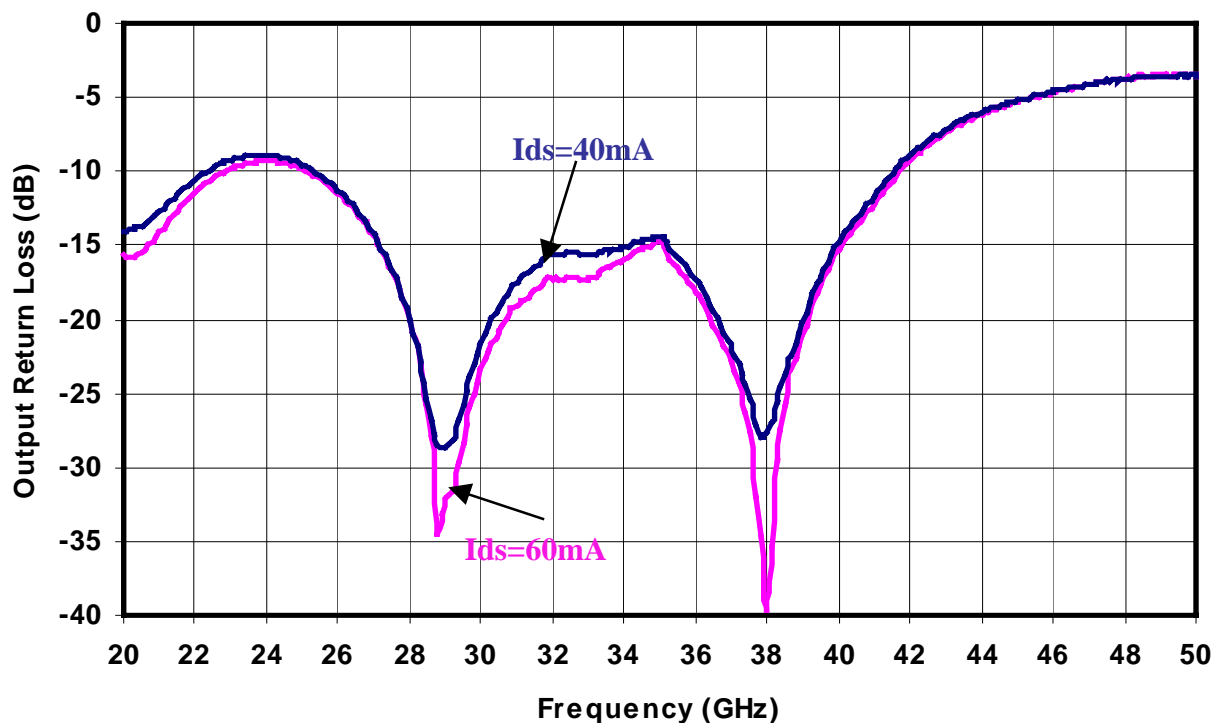
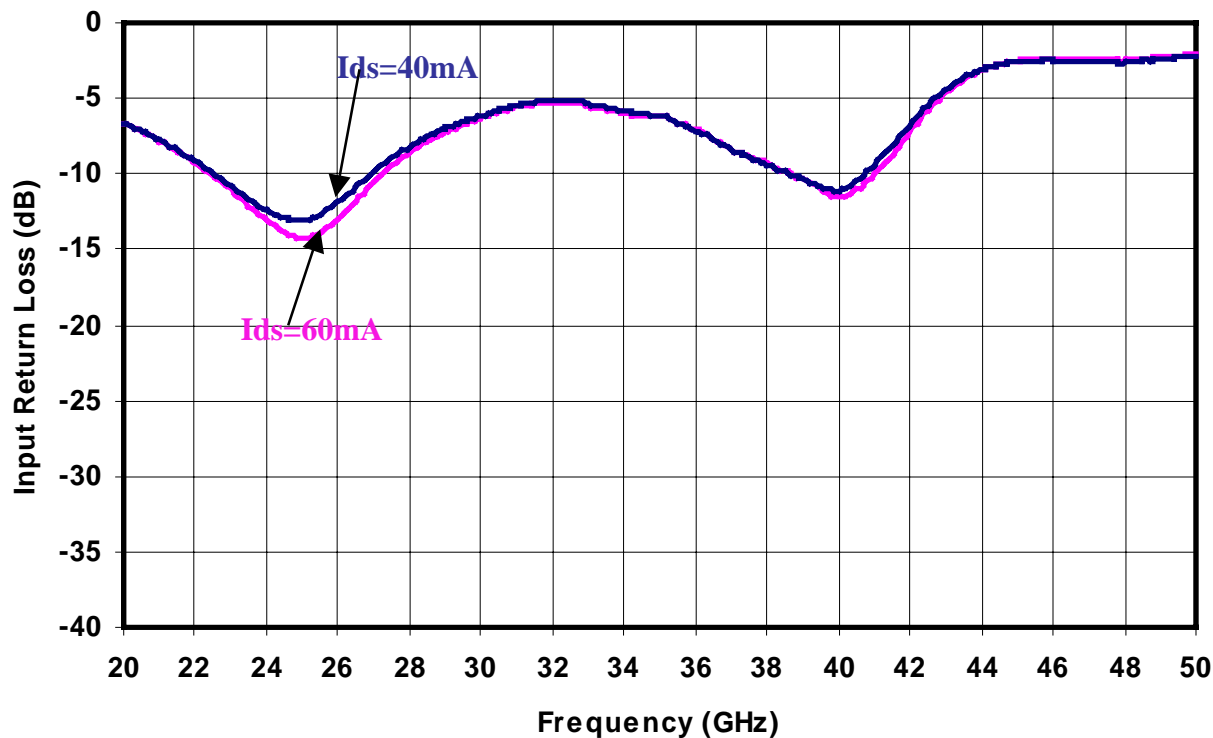
## Measured Data

Bias Conditions:  $V_d = 3\text{ V}$ ,  $I_d = 40\text{mA}/60\text{mA}$

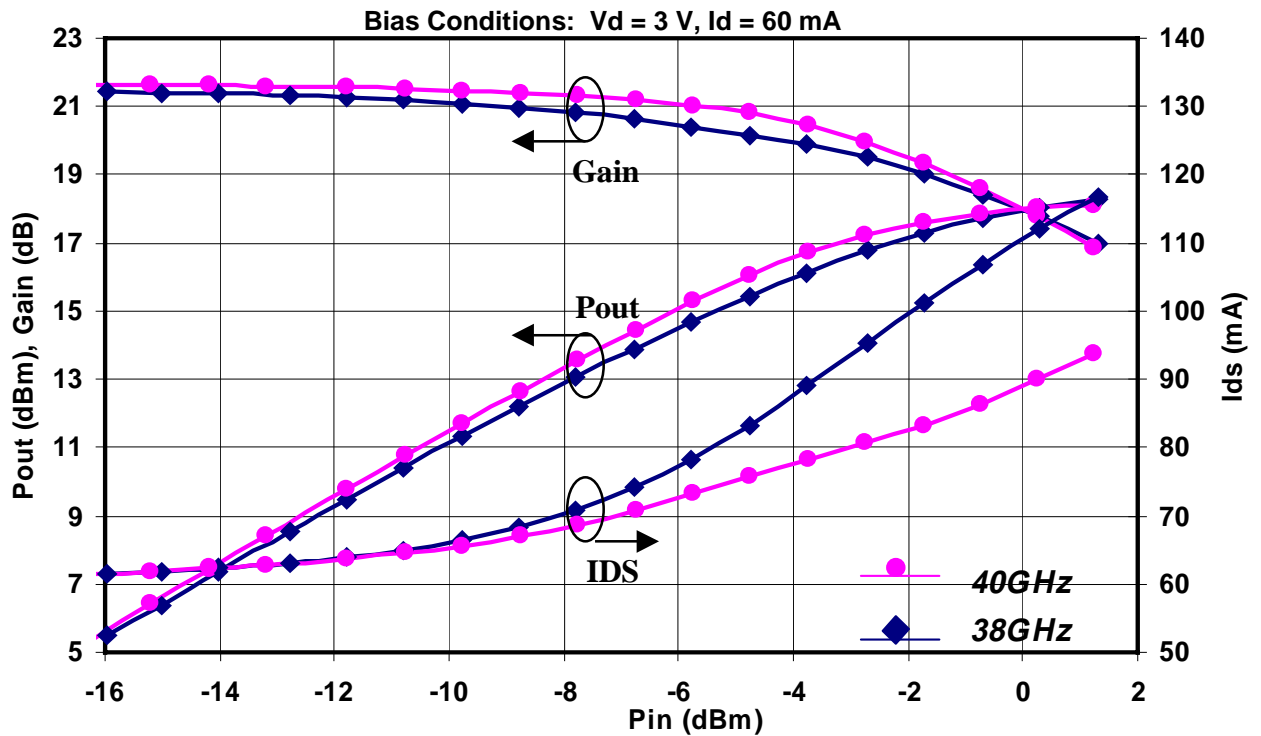
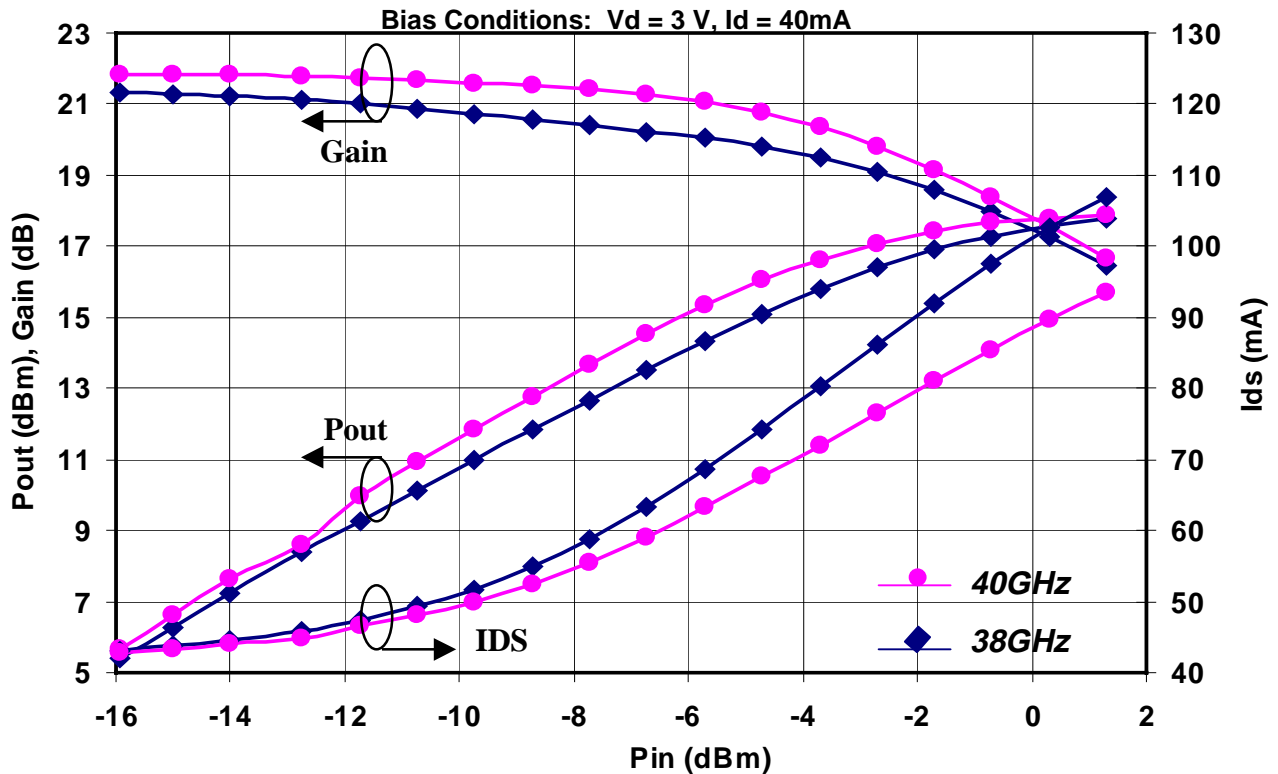


## Measured Data

Bias Conditions:  $V_d = 3\text{ V}$ ,  $I_d = 40\text{mA}/60\text{mA}$

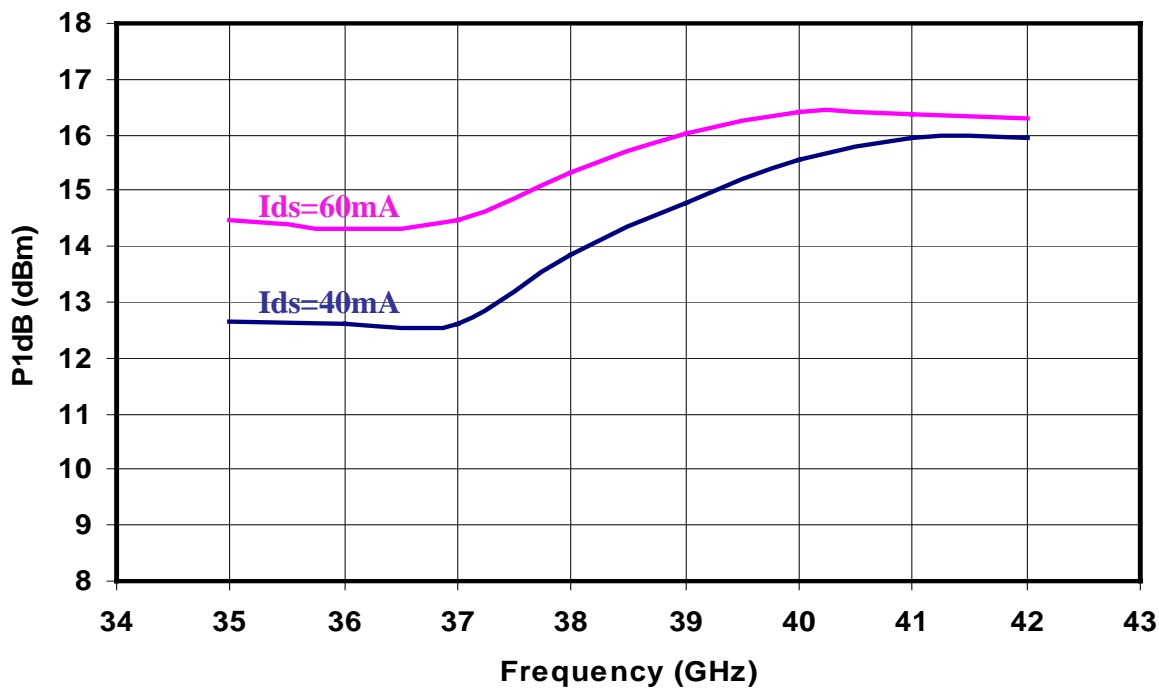


## Measured Data

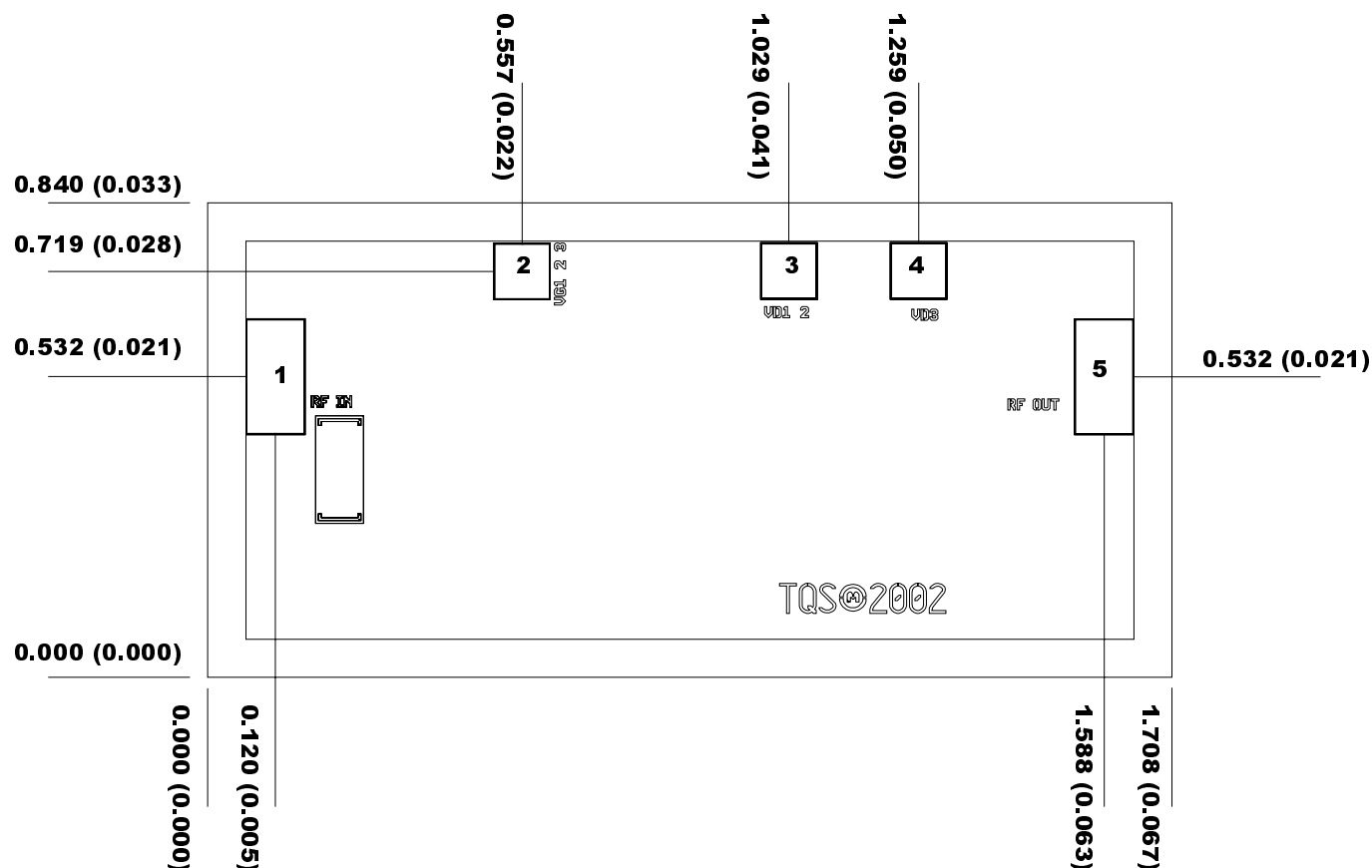


## Measured Data

Bias Conditions:  $V_d = 3\text{ V}$ ,  $I_d = 40\text{mA}/60\text{mA}$



## Mechanical Drawing



**Units: Millimeters (Inches)**

**Thickness: 0.100 (0.004)**

**Chip edge to bond pad dimensions are shown to center of bond pad**

**Chip size tolerance: +/- 0.051 (0.002)**

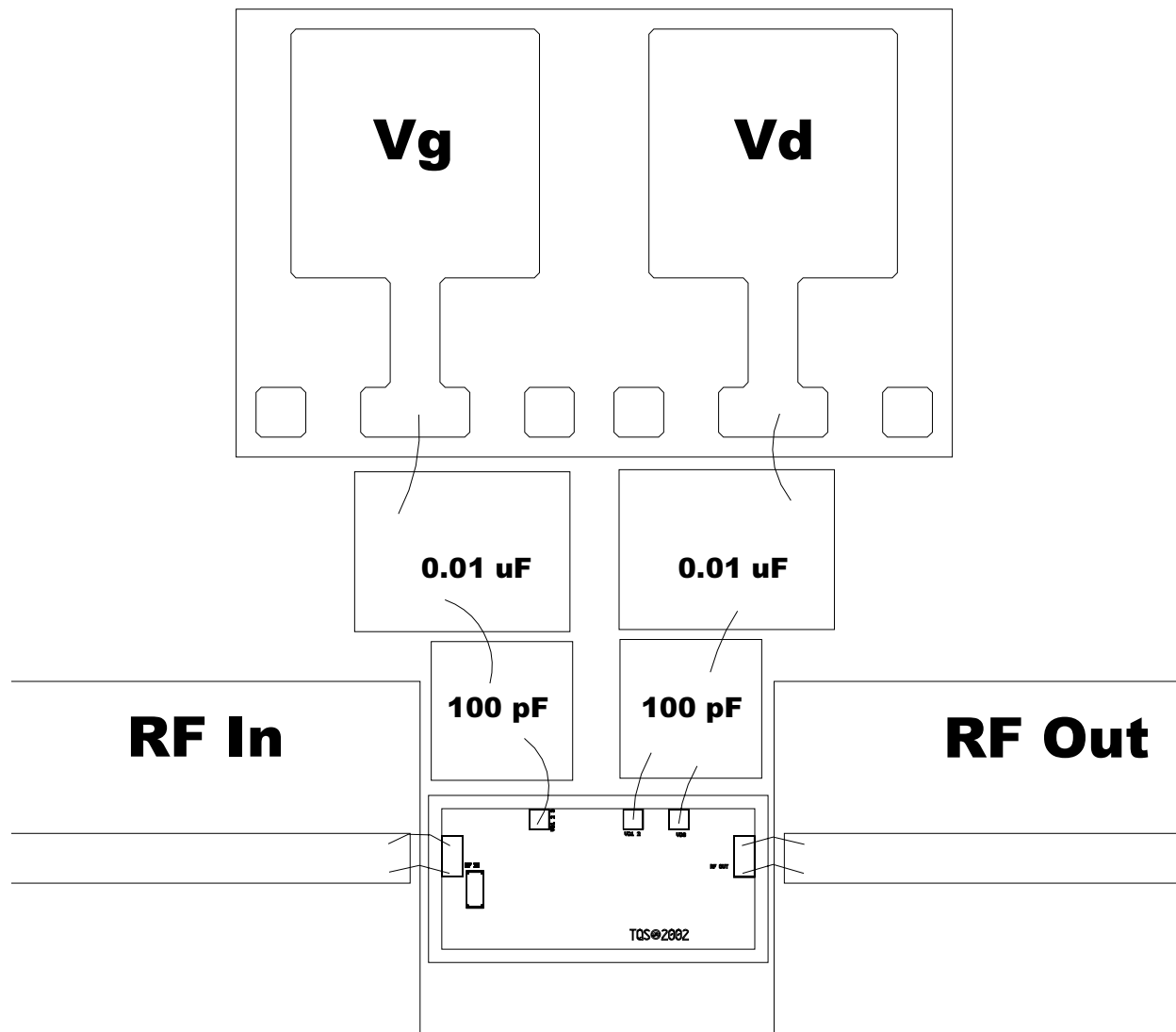
**GND IS BACKSIDE OF MMIC**

<b>Bond pad #1</b>	<b>(RF In)</b>	<b>0.100 x 0.200 (0.004 x 0.008)</b>
<b>Bond pad #2</b>	<b>(Vg)</b>	<b>0.100 x 0.100 (0.004 x 0.004)</b>
<b>Bond pad #3</b>	<b>(Vd1,2)</b>	<b>0.100 x 0.100 (0.004 x 0.004)</b>
<b>Bond pad #4</b>	<b>(Vd3)</b>	<b>0.100 x 0.100 (0.004 x 0.004)</b>
<b>Bond pad #5</b>	<b>(RF Out)</b>	<b>0.100 x 0.200 (0.004 x 0.008)</b>

*GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.*



## Chip Assembly Diagram



***GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.***

## **Assembly Process Notes**

Reflow process assembly notes:

- Use AuSn (80/20) solder with limited exposure to temperatures at or above 300 °C for 30 sec
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- No fluxes should be utilized.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.
- Organic attachment can be used in low-power applications.
- Curing should be done in a convection oven; proper exhaust is a safety concern.
- Microwave or radiant curing should not be used because of differential heating.
- Coefficient of thermal expansion matching is critical.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonics are critical parameters.
- Aluminum wire should not be used.
- Devices with small pad sizes should be bonded with 0.0007-inch wire.
- Maximum stage temperature is 200 °C.

***GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.***