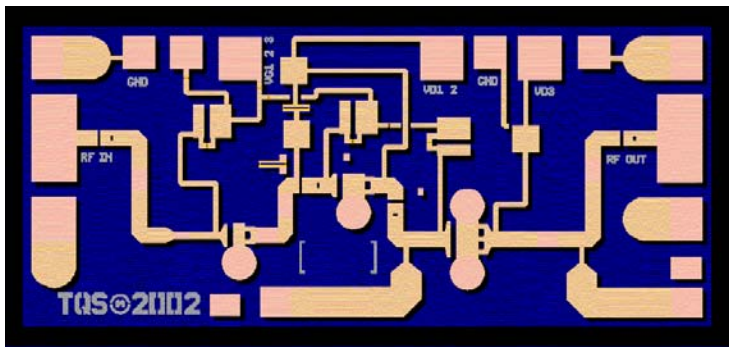


Ka Band Low Noise Amplifier

TGA4508-EPU

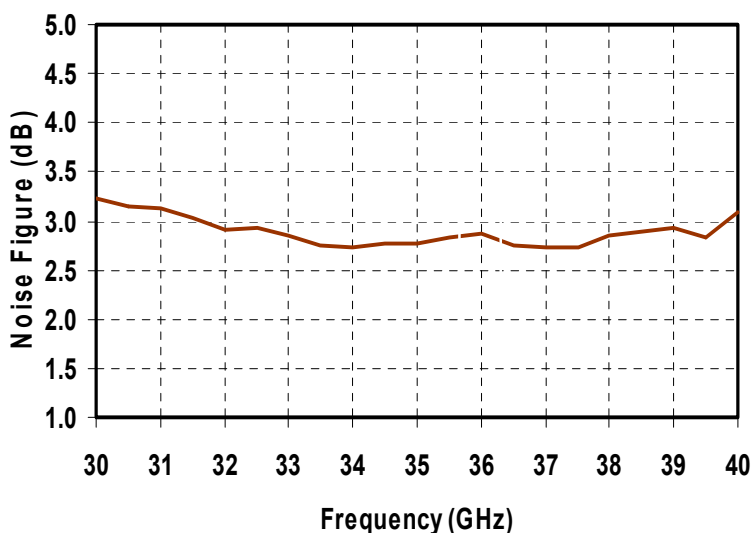
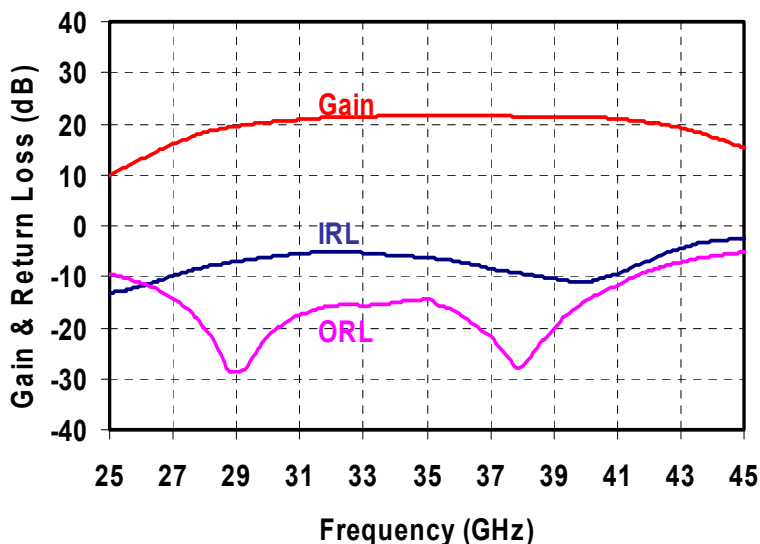


Key Features

- Typical Frequency Range: 30 - 42 GHz
- 21 dB Nominal Gain
- 2.8 dB Nominal Noise Figure
- 14 dBm Nominal P1dB @ 38 GHz
- Bias 3 V, 40mA
- 0.15 um 3MI pHEMT Technology
- Chip Dimensions 1.7 x 0.8 x 0.1 mm
(0.067 x 0.031 x 0.004) in

Preliminary Measured Data

Bias Conditions: $V_d = 3\text{ V}$, $I_d = 40\text{ mA}$



Primary Applications

- Point-to-Point Radio
- Point-to-MultiPoint Radio
- Ka Band VSAT

Note: Devices designated as EPU are typically early in their characterization process prior to finalizing all electrical and process specifications. Specifications are subject to change without notice

TABLE I
MAXIMUM RATINGS 1/

SYMBOL	PARAMETER	VALUE	NOTES
V _d	Drain Voltage	5 V	<u>2/</u>
V _g	Gate Voltage Range	-1 TO +0.5 V	
I _d	Drain Current	190 mA	<u>2/ 3/</u>
I _g	Gate Current	6 mA	<u>3/</u>
P _{IN}	Input Continuous Wave Power	TBD	
P _D	Power Dissipation	TBD	<u>2/ 4/</u>
T _{CH}	Operating Channel Temperature	150 °C	<u>5/ 6/</u>
T _M	Mounting Temperature (30 Seconds)	320 °C	
T _{STG}	Storage Temperature	-65 to 150 °C	

- 1/ These ratings represent the maximum operable values for this device.
- 2/ Combinations of supply voltage, supply current, input power, and output power shall not exceed P_D.
- 3/ Total current for the entire MMIC.
- 4/ When operated at this bias condition with a base plate temperature of TBD, the median life is reduced from TBD to TBD hrs.
- 5/ Junction operating temperature will directly affect the device median time to failure (MTTF). For maximum life, it is recommended that junction temperatures be maintained at the lowest possible levels.
- 6/ These ratings apply to each individual FET.

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TABLE II
DC PROBE TESTS
(Ta = 25 °C, Nominal)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
I _{DSS3}	Saturated Drain Current		38		mA
G _{M3}	Transconductance		164		mS
V _{BVGS3}	Breakdown Voltage gate-source			-5	V
V _{BVGD3}	Breakdown Voltage gate-drain			-5	V
V _{P1,2,3}	Pinch-off Voltage	-1.0		-0.1	V

Q1 is 100 um FET, Q2 is 200 um FET, Q3 is 300 um FET

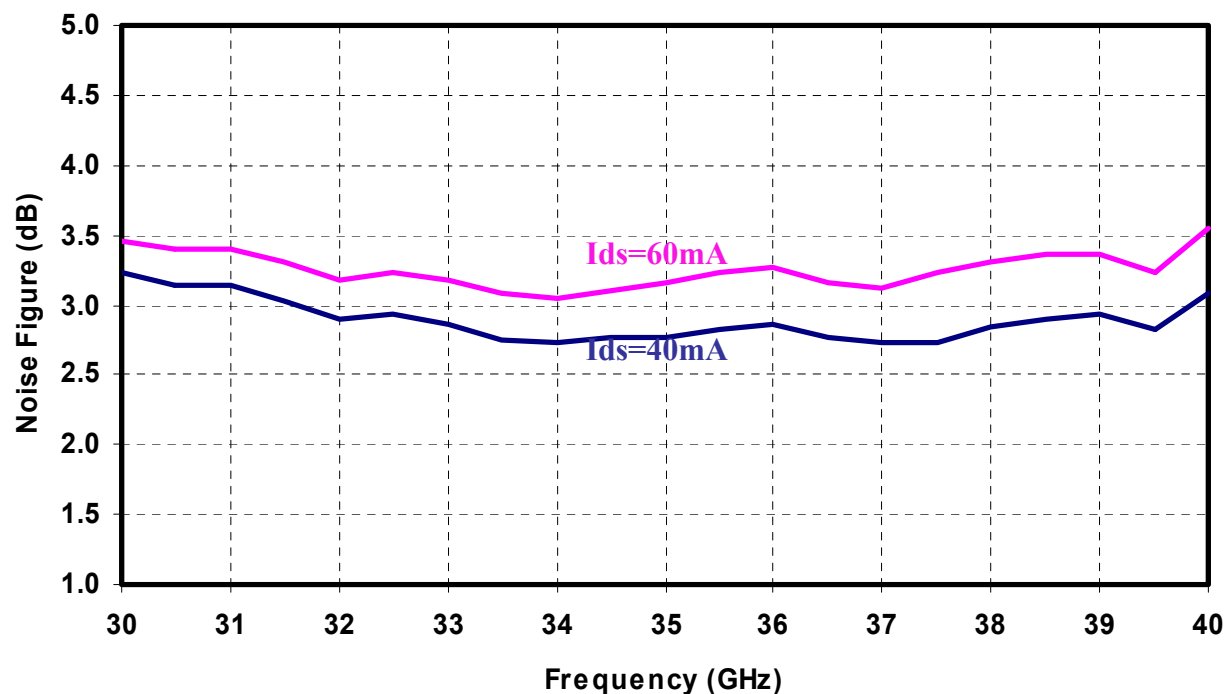
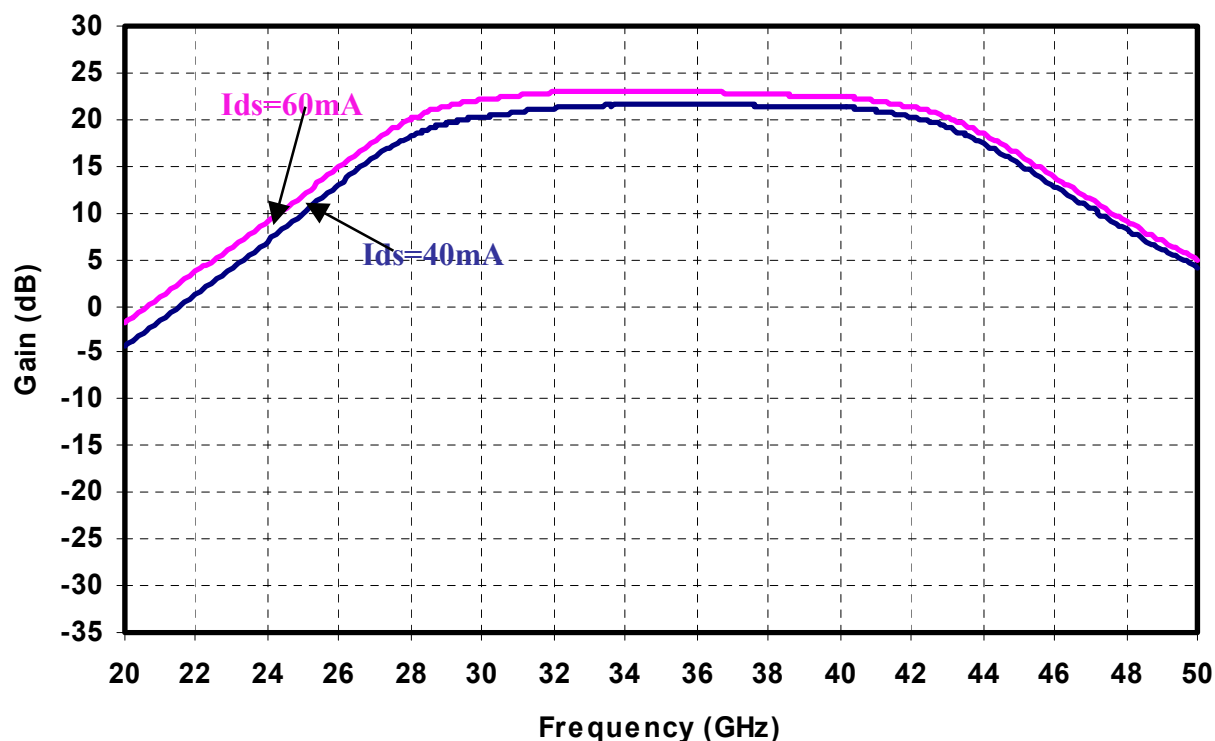
TABLE III
ELECTRICAL CHARACTERISTICS
(Ta = 25 °C, Nominal)

PARAMETER	TYPICAL	UNITS
Drain Voltage, Vd	3	V
Drain Current, Id	40	mA
Gate Voltage, Vg	-0.5 to +0.5	V
Small Signal Gain, S21	21	dB
Input Return Loss, S11	8	dB
Output Return Loss, S22	15	dB
Noise Figure, NF	2.8	dB
Output Power @ 1 dB Compression Gain @ 38 GHz, P1dB	14	dBm

Note: Devices designated as EPU are typically early in their characterization process prior to finalizing all electrical and process specifications. Specifications are subject to change without notice

Preliminary Measured Data

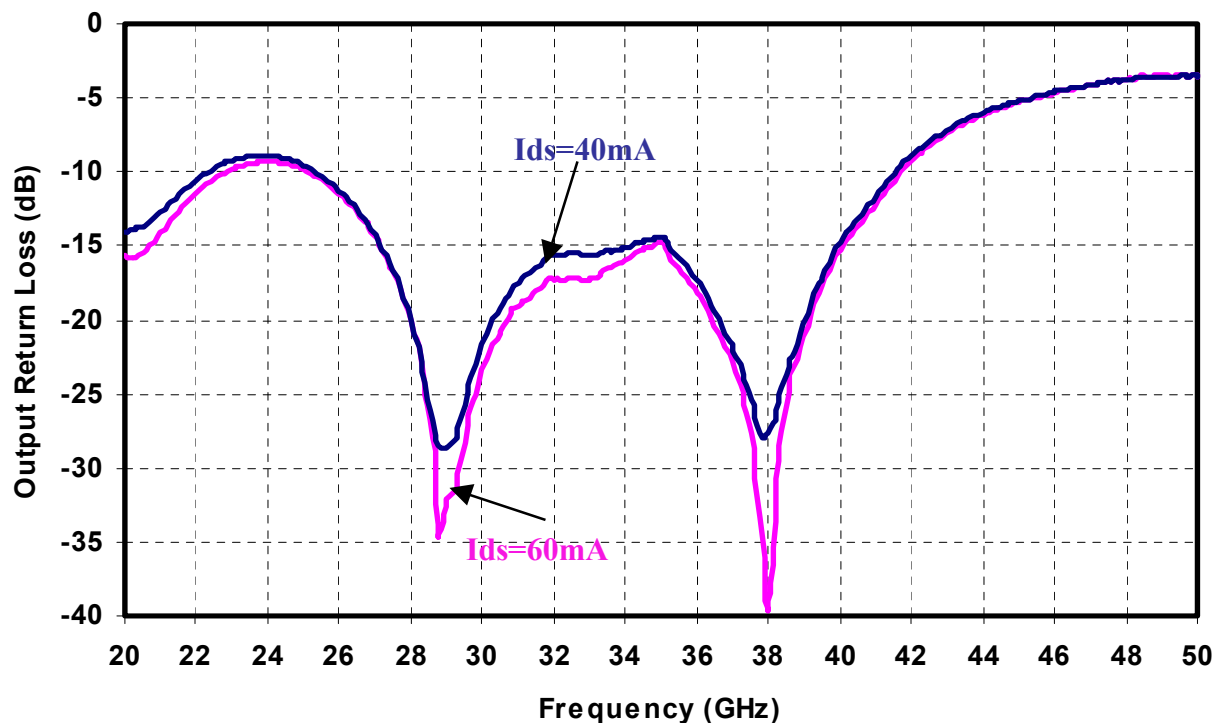
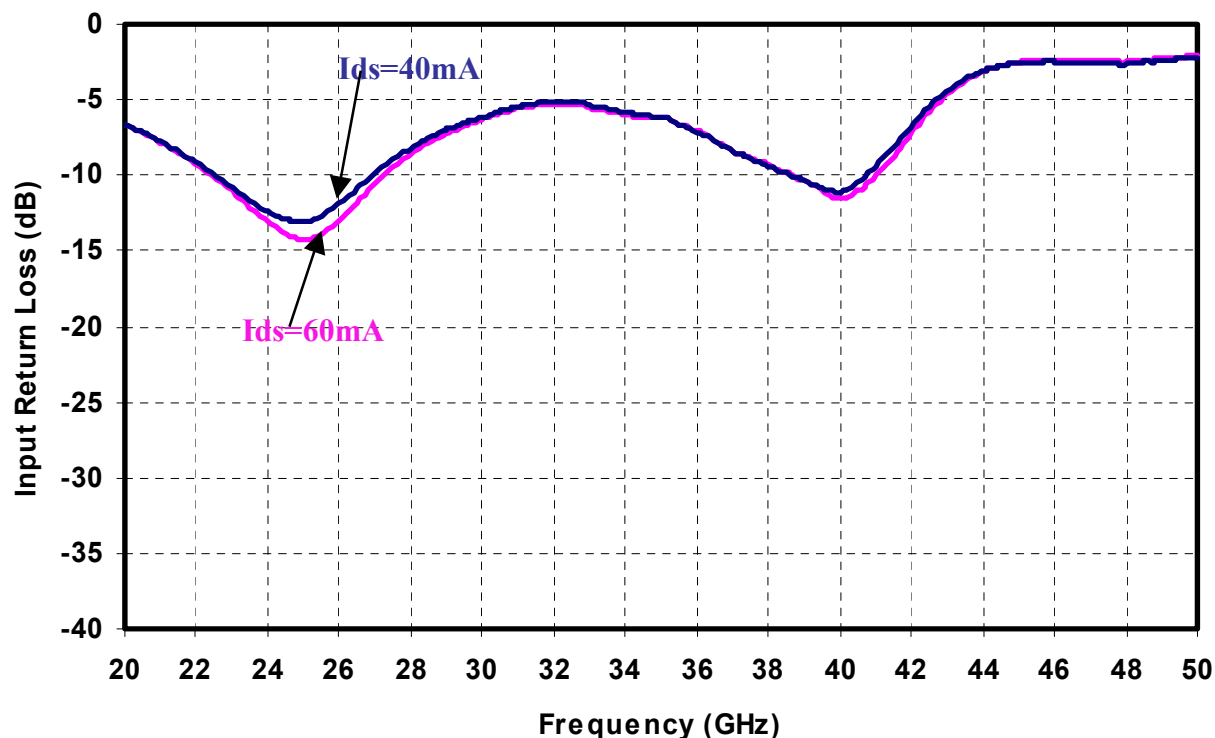
Bias Conditions: $V_d = 3\text{ V}$, $I_d = 40\text{ mA}/60\text{ mA}$



Note: Devices designated as EPU are typically early in their characterization process prior to finalizing all electrical and process specifications. Specifications are subject to change without notice

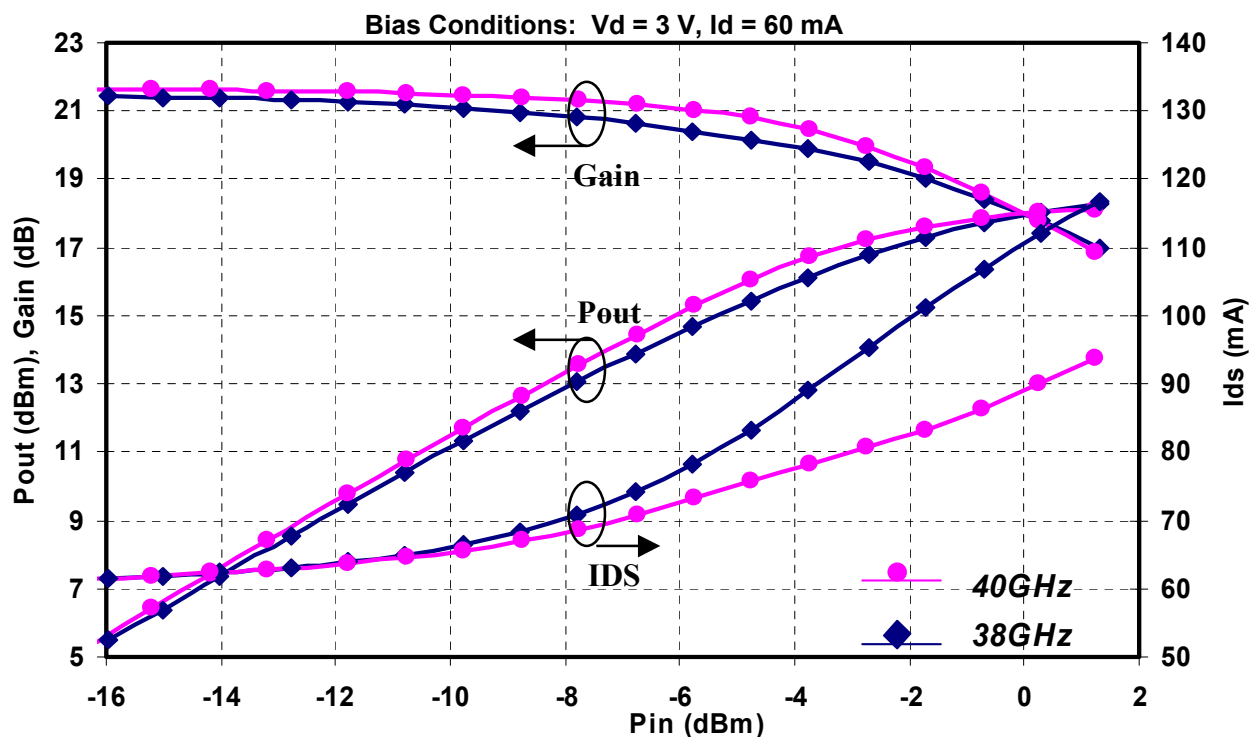
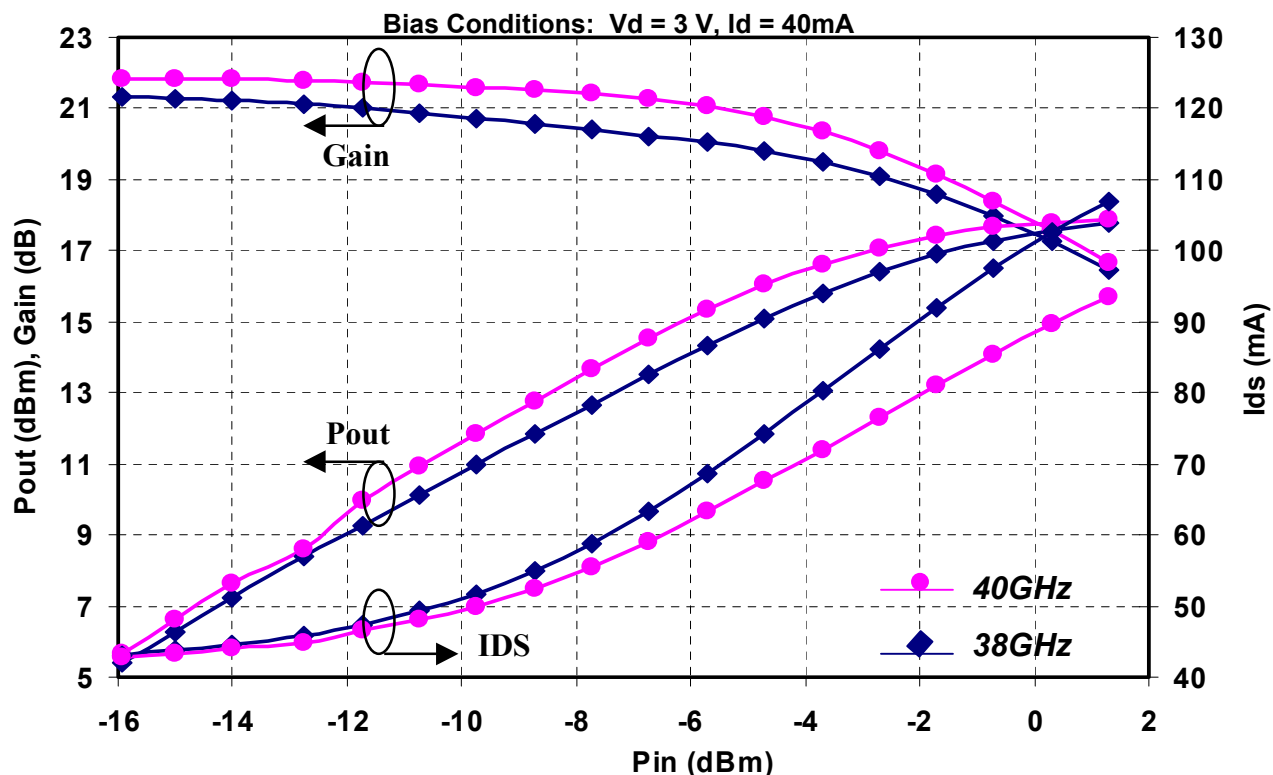
Preliminary Measured Data

Bias Conditions: $V_d = 3\text{ V}$, $I_d = 40\text{ mA}/60\text{ mA}$



Note: Devices designated as EPU are typically early in their characterization process prior to finalizing all electrical and process specifications. Specifications are subject to change without notice

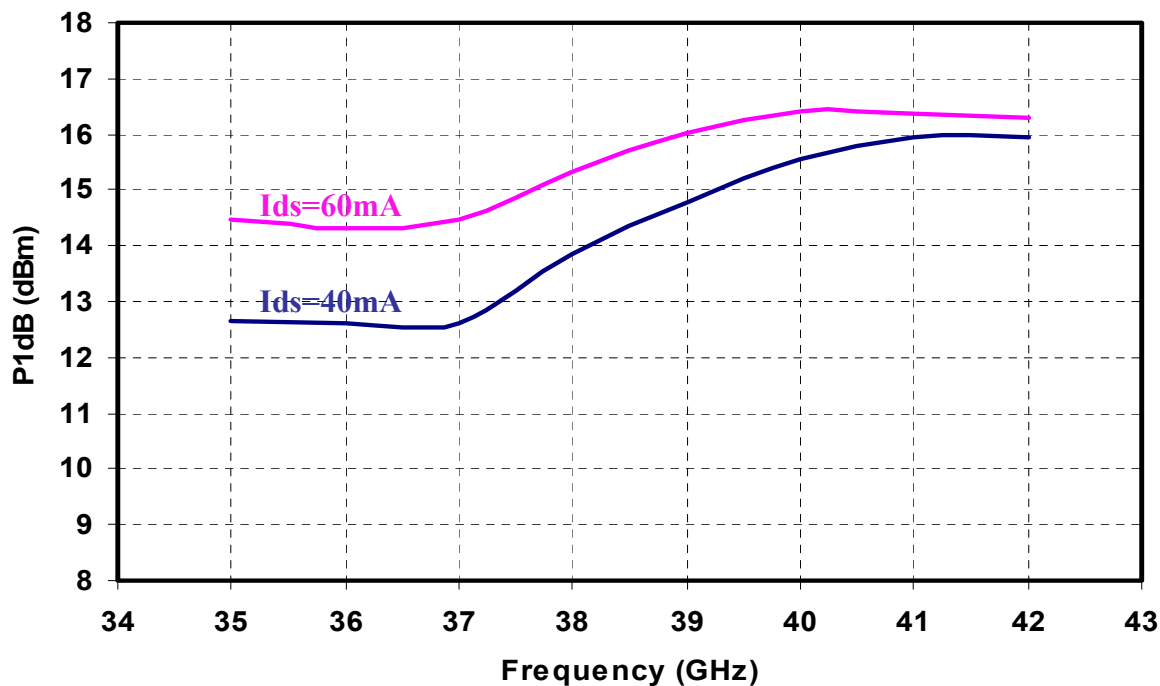
Preliminary Measured Data



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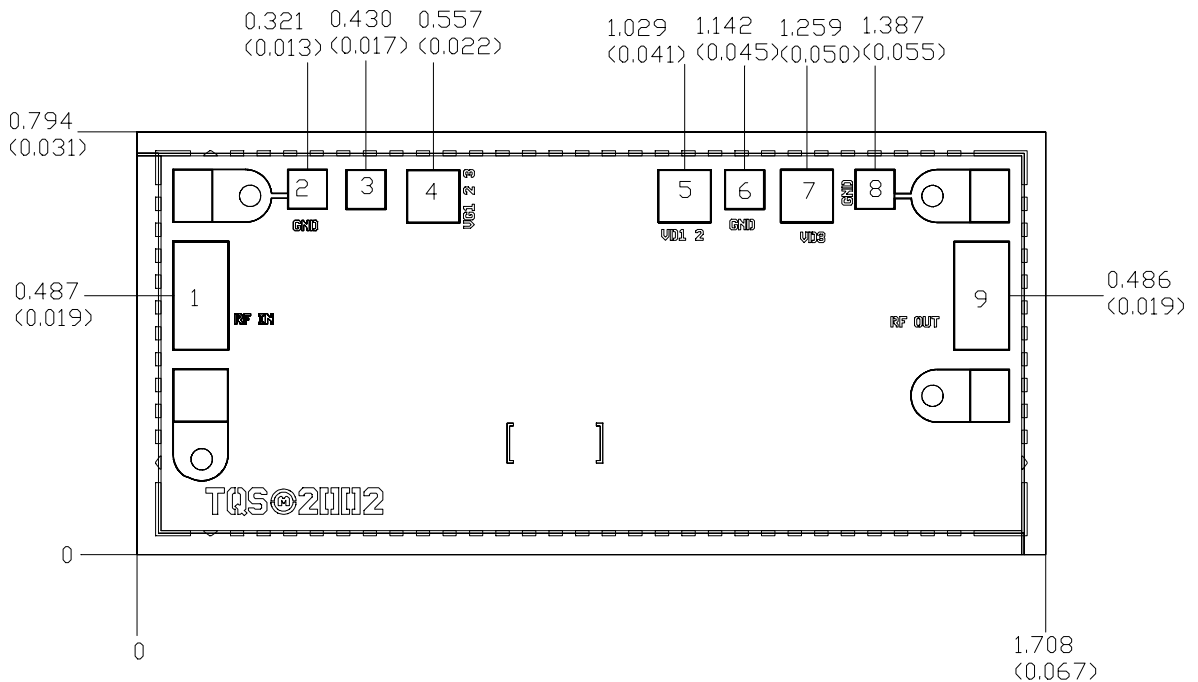
Preliminary Measured Data

Bias Conditions: $V_d = 3\text{ V}$, $I_d = 40\text{mA}/60\text{mA}$



Note: Devices designated as EPU are typically early in their characterization process prior to finalizing all electrical and process specifications. Specifications are subject to change without notice

Mechanical Drawing



Units: Millimeters (Inches)

Thickness: 0.100 (0.004)

Chip edge to bond pad dimensions are shown to center of bond pad

Chip size tolerance: +/- 0.051 (0.002)

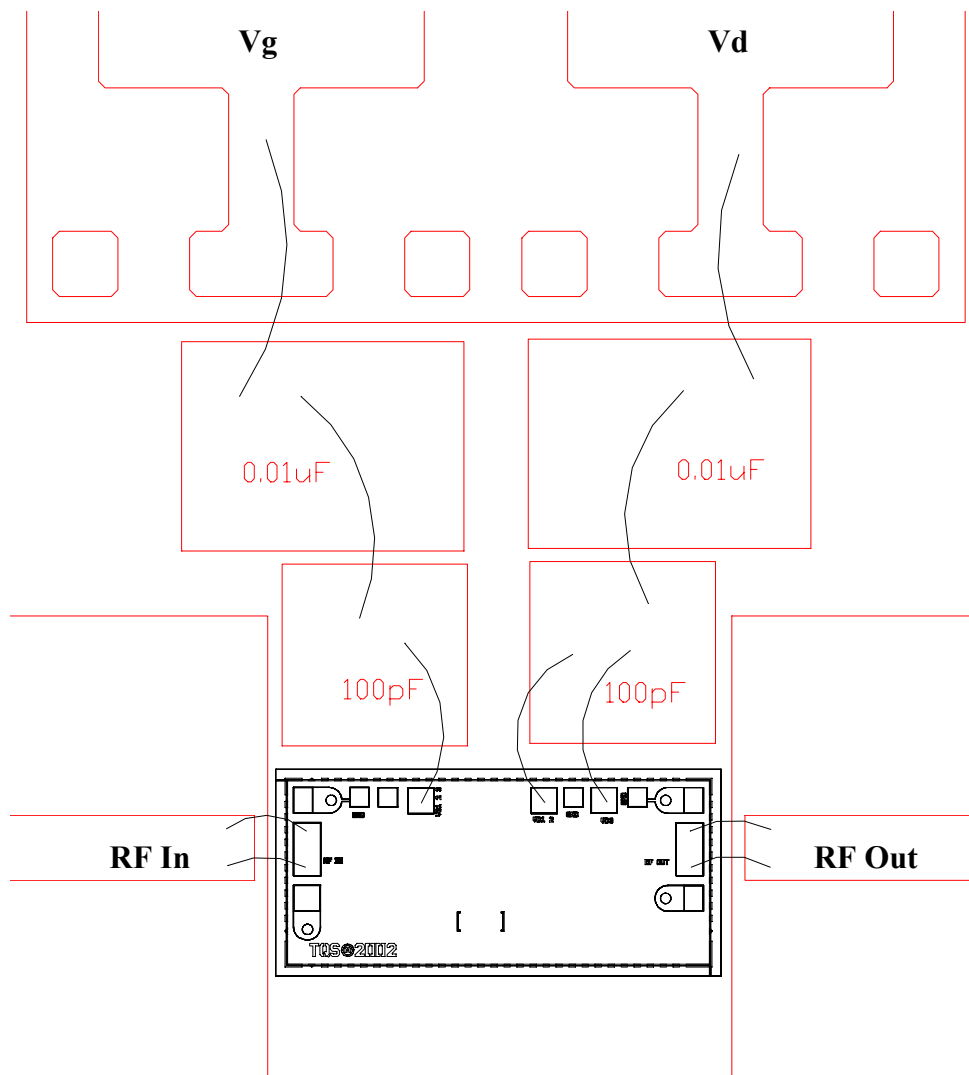
GND is back side of MMIC

Bond pad #1	(RF In)	0.105 x 0.205 (0.004 x 0.008)
Bond pad #2, 3, 6, 8	(N/C)	0.075 x 0.075 (0.003 x 0.003)
Bond pad #4	(Vg)	0.100 x 0.100 (0.004 x 0.004)
Bond pad #5	(Vd1,2)	0.100 x 0.100 (0.004 x 0.004)
Bond pad #7	(Vd3)	0.100 x 0.100 (0.004 x 0.004)
Bond pad #9	(RF Out)	0.105 x 0.205 (0.004 x 0.008)

GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

Note: Devices designated as EPU are typically early in their characterization process prior to finalizing all electrical and process specifications. Specifications are subject to change without notice

Chip Assembly Diagram



Note: Positive or Negative Gate bias may be required to achieve recommended Operating Point, $(-0.5\text{ V} < V_g < +0.5\text{ V})$.

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Assembly Process Notes

Reflow process assembly notes:

- Use AuSn (80/20) solder with limited exposure to temperatures at or above 300°C (30 seconds max).
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- No fluxes should be utilized.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.
- Organic attachment can be used in low-power applications.
- Curing should be done in a convection oven; proper exhaust is a safety concern.
- Microwave or radiant curing should not be used because of differential heating.
- Coefficient of thermal expansion matching is critical.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonics are critical parameters.
- Aluminum wire should not be used.
- Maximum stage temperature is 200°C.

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