

DC-18GHz MPA with AGC

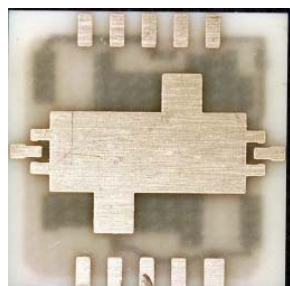
OC-192 12.5Gb/s LN/MZ Driver and Receive AGC Applications

Surface Mount Package

TGA8652-EPU



Top View



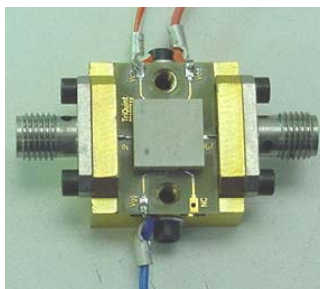
Bottom View

Description

The TriQuint TGA8652EPU is a medium power wideband AGC amplifier combined with off chip circuitry assembled in a Surface Mount Package. The TGA8652EPU typically provides 16dB small signal gain with 6dB AGC range. Typical input and output return loss is <10dB. Typical Noise Figure is 2.5dB at 3GHz. Typical saturated output power is 25dBm. Small signal 3dB BW is 14GHz with saturated power performance to 18GHz. RF ports are DC coupled enabling the user to customize system corner frequencies. Applications include OC192 12.5Gbit/s NRZ Lithium Niobate Modulator and receive AGC amplifier.

Drain bias may be applied thru the on-chip drain termination resistor for low drive applications or thru the RF output port for high drive applications. A cascaded pair demonstrated 8Vpp output voltage swing with 500mVpp at the input when stimulated with 10Gbit/s. 2³¹-1prbs. NRZ data.

The TGA8652EPU is available on an evaluation board.



Evaluation Board

Key Features and Performance

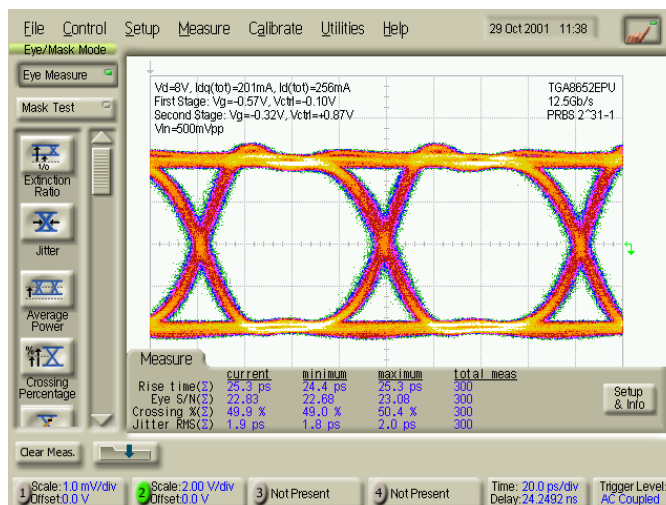
- 0.5um pHEMT Dual Gate Technology
- DC - 14GHz Linear BW
- DC - 18GHz Saturated Power BW
- 16dB small signal gain
- 6 dB AGC Range
- 25ps Edge Rates (10/90)
- 8Vpp 12.5Gb/s NRZ PRBS
- Low Power Dissipation
- Package size: .350 x .350 x .084 inches.
- Evaluation Board Available.

Primary Applications

- 12.5Gb/s NRZ Modulator Driver
- Receiver AGC

Measured Performance

Cascaded 8652 Evaluation Boards
12.5Gb/s Performance
Output = 8Vpp, Input = 500mVpp
Scale: 2V/div, 20ps/div



Note: Devices designated as EPU are typically early in their characterization process prior to finalizing all electrical and process specifications. Specifications are subject to change without notice.

MAXIMUM RATINGS

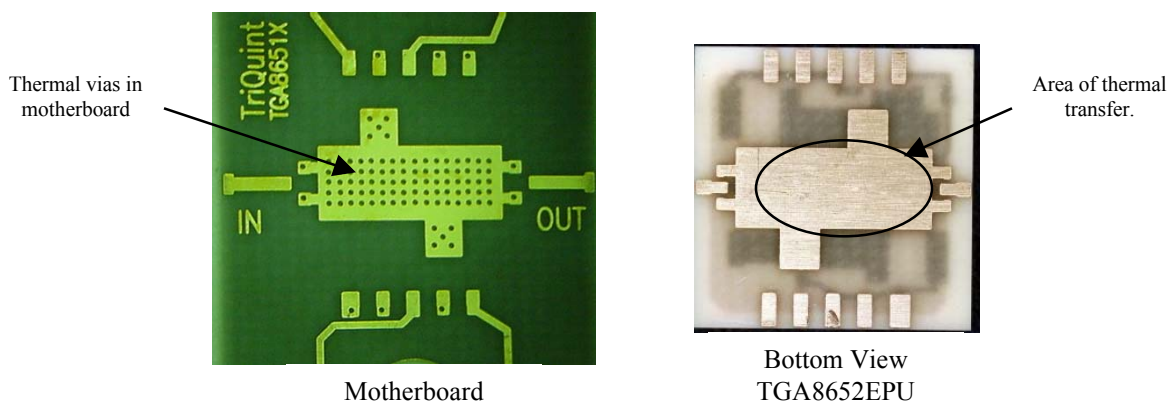
SYMBOL	PARAMETER <u>5/</u>	VALUE	NOTES
V^+	POSITIVE SUPPLY VOLTAGE	10 V	
I^+	POSITIVE SUPPLY CURRENT	250 mA	<u>1/</u>
P_{IN}	INPUT CONTINUOUS WAVE POWER	23 dBm	<u>4/</u>
P_D	POWER DISSIPATION	2.6 W	
T_{CH}	OPERATING CHANNEL TEMPERATURE	150 °C	<u>2/ 3/</u>
T_{STG}	STORAGE TEMPERATURE	-20 to 150 °C	

- 1/ Total current .
- 2/ These ratings apply to each individual FET.
- 3/ Junction operating temperature directly affects the device median time to failure (T_M). For maximum life and best performance, it is recommended that junction temperatures be maintained at the lowest possible levels.
- 4/ This value reflects an estimate.
- 5/ These ratings represent the maximum operable values for the device.

THERMAL INFORMATION

Parameter	Test Condition	T_{CH} (°C)	$R_{\theta JC}$ (°C/W)	T_M (HRS)
$R_{\theta JC}$ Thermal Resistance (channel to backside of package)	$V_{dft} = 6\text{ V}$, $V_{ctrl} = 1\text{ V}$, $I_D = 170\text{ mA} \pm 5\%$	115	45	> 1E+7

NOTE: Thermal transfer is conducted thru the bottom of the TGA8652-EPU package into the motherboard. Design the motherboard to assure adequate thermal transfer to the base plate. An array of filled thermal vias is recommended as shown in the example below.



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RF SPECIFICATIONS

(T_A = 25°C ± 5°C)

NOTE	TEST	MEASUREMENT CONDITIONS 8V @ 175mA	VALUE			UNITS
			MIN	TYP	MAX	
<u>1</u> /	SMALL SIGNAL BANDWIDTH			12		GHz
	SATURATED POWER BW			18		GHz
<u>1</u> /	SMALL-SIGNAL GAIN MAGNITUDE	2.5GHz		16		dB
	AGC RANGE	Midband		6		dB
	NOISE FIGURE	3GHz		2.5		dB
	SATURATED OUTPUT VOLTAGE	10Gb/s with Vin-2Vpp		8		Vpp
<u>1</u> /	SATURATED OUTPUT POWER	DC-10GHz		25		dBm
<u>2</u> /	INPUT RETURN LOSS MAGNITUDE	DC-10GHz		-12		dB
<u>2</u> /	OUTPUT RETURN LOSS MAGNITUDE	DC-10GHz		-12		dB
	GROUP DELAY	DC-10GHz		+/- 20		ps
	RISE TIME			< 30		ps

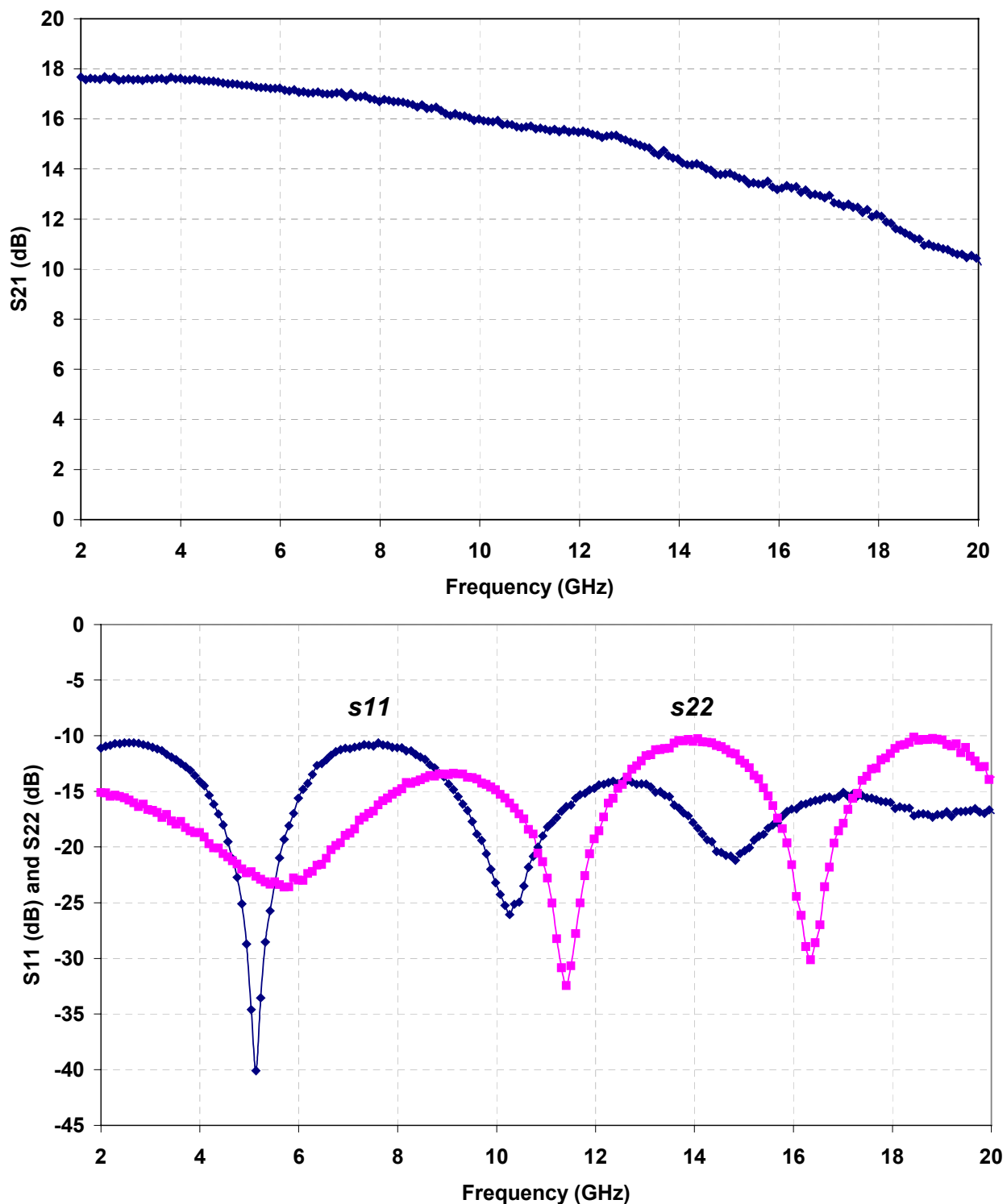
Notes:

1/ Measured at wafer RF probe

2/ Measured at package RF probe

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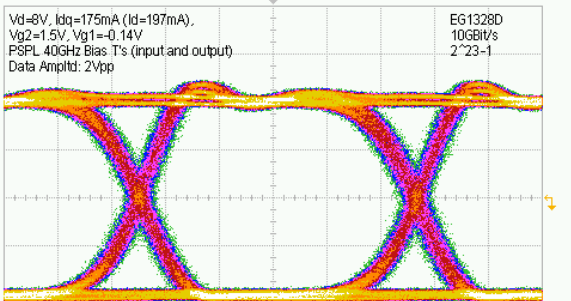
TGA8652 Typical Measured S-parameters



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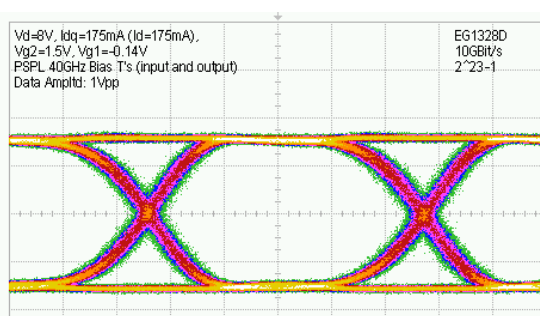
Measured Performance

8V P-P (Saturated)



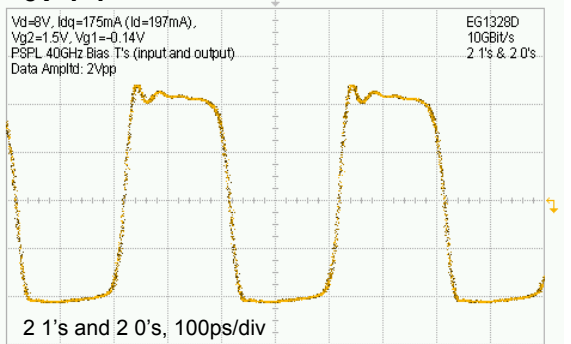
10Gbit/s Performance
Output = 8V P-P, Input = 2V P-P
scale 2V/div, 20ps/div

6V P-P (Near Small Signal)



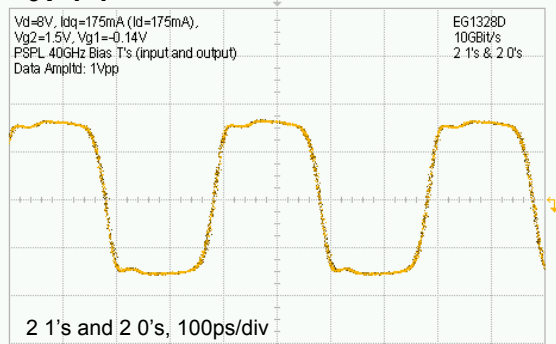
10Gbit/s Performance
Output = 6V P-P, Input = 1V P-P
scale 2V/div, 20ps/div

8V P-P

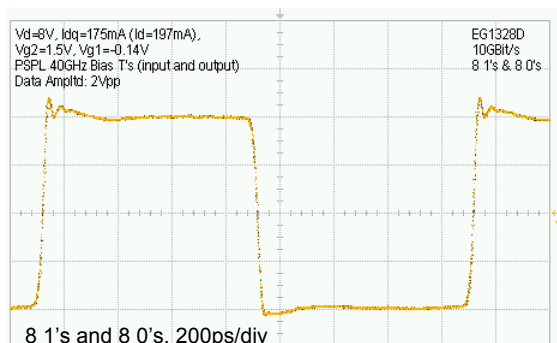


2 1's and 2 0's, 100ps/div

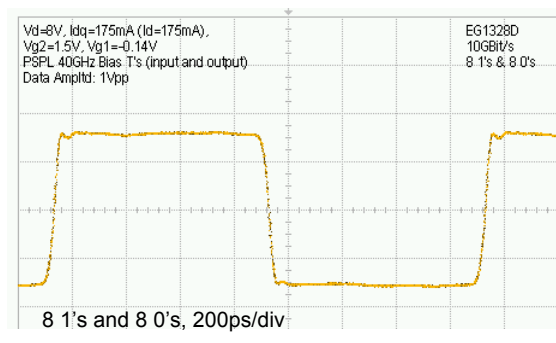
6V P-P



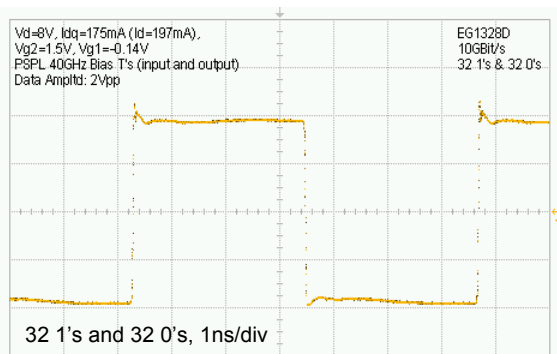
2 1's and 2 0's, 100ps/div



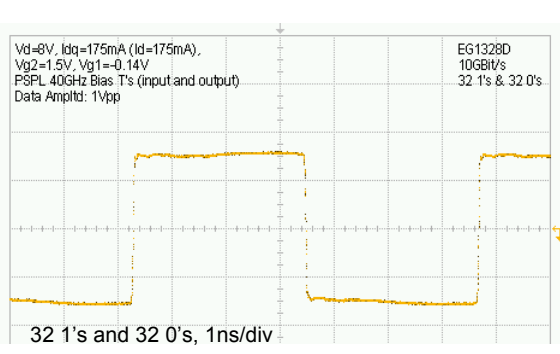
8 1's and 8 0's, 200ps/div



8 1's and 8 0's, 200ps/div

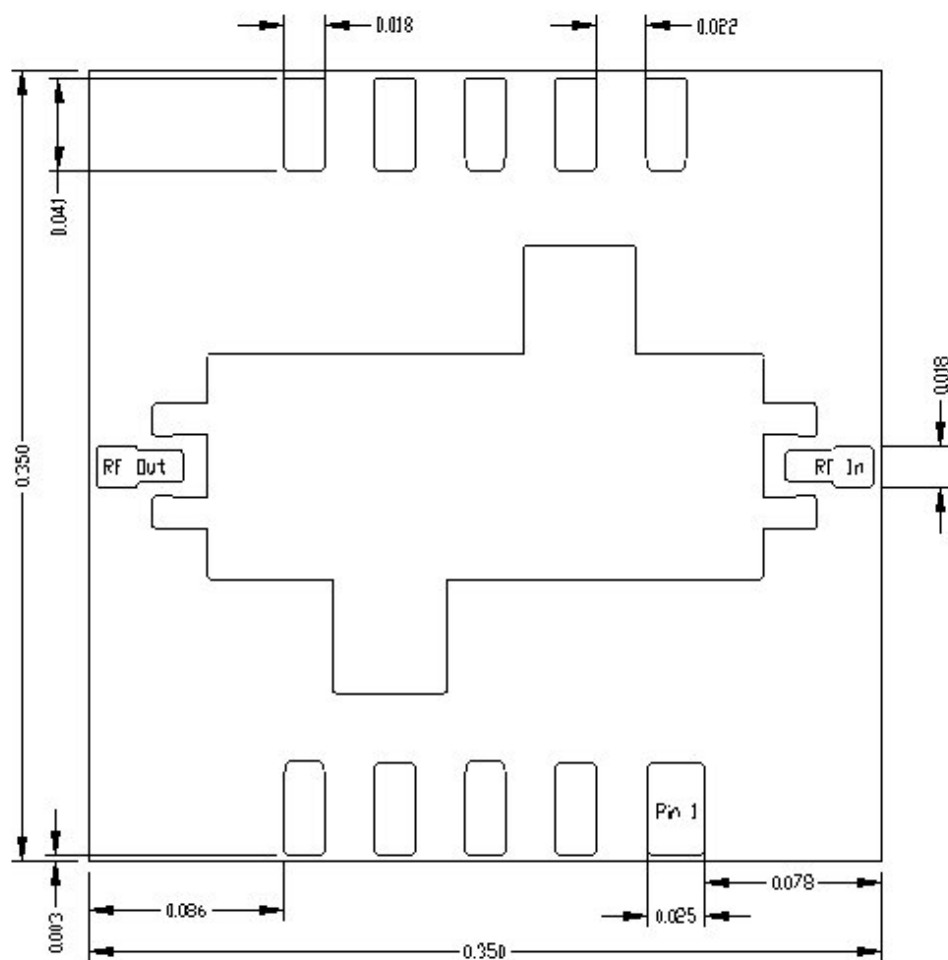


32 1's and 32 0's, 1ns/div

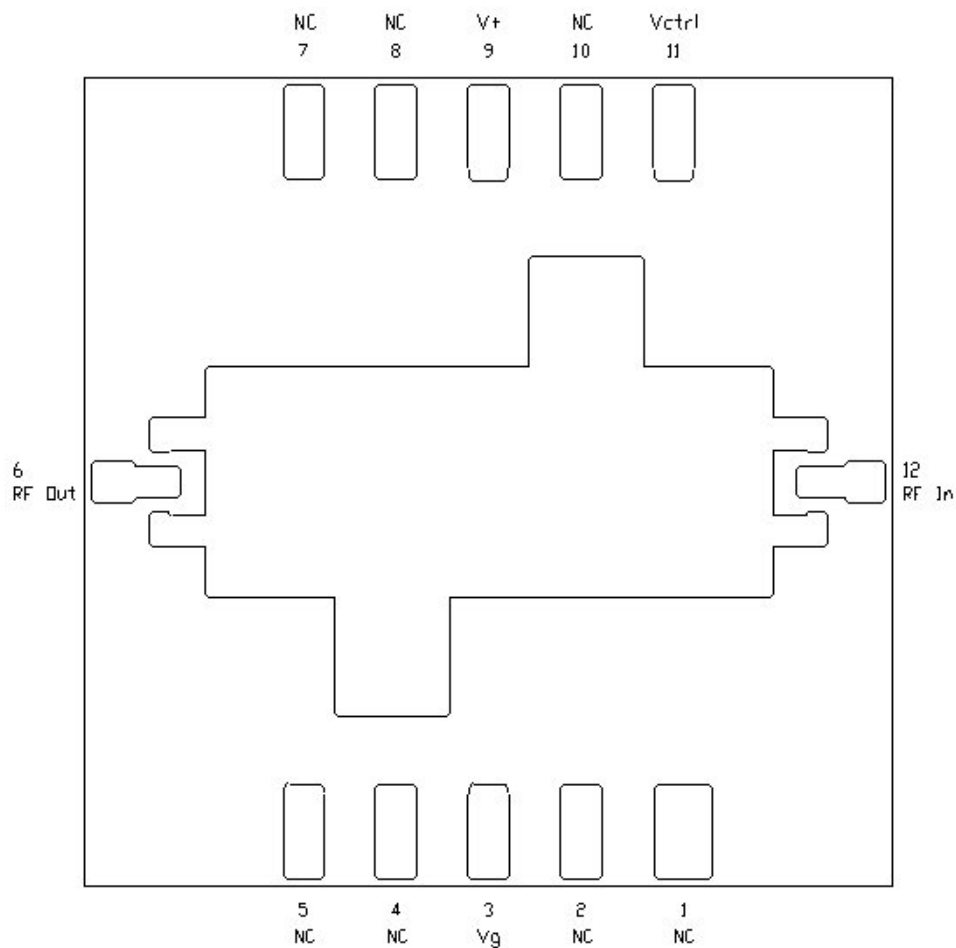


32 1's and 32 0's, 1ns/div

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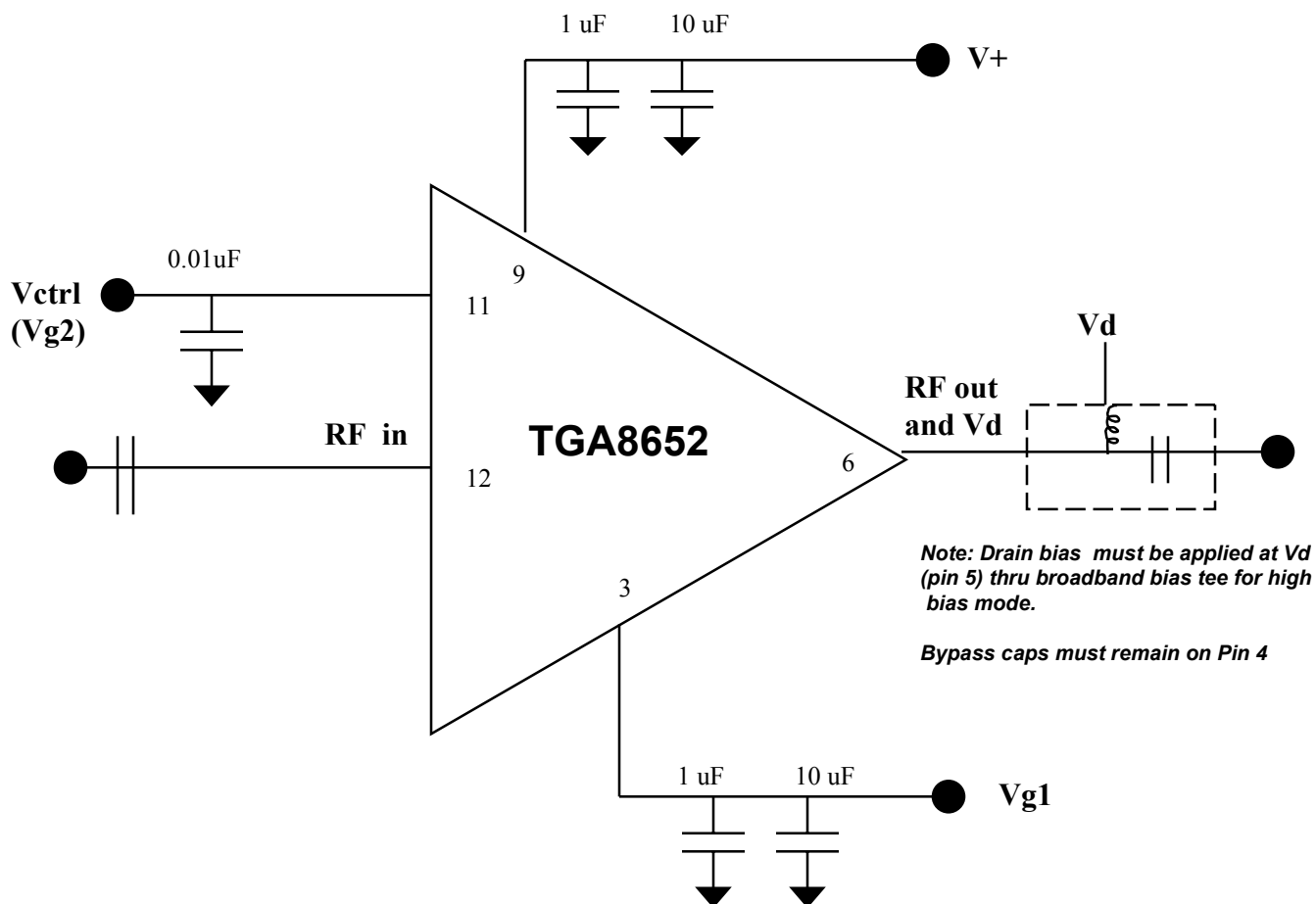


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PIN	FUNCTION	PIN	FUNCTION
1	NC	7	NC
2	NC	8	NC
3	Vg	9	V+
4	NC	10	NC
5	NC	11	Vctrl
6	OUT	12	IN

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Bias Procedure

- 1) Make sure no RF power is applied to the device before continuing.
- 2) Pinch off device by setting V_{G1} to $-2.5V$.
- 3) Raise V_D to $8.0V$ while monitoring drain current. Current should be zero.

NOTE: V_D bias should be applied to the RF output port via a bias tee for high power bias.

- 4) Raise V_{G2} to $1.5V$ (no greater than $1.5V$).
- 5) Make V_{G1} more positive until drain current reaches $175mA$. ($80mA$ for low noise bias)
- 6) Apply RF power.

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Assembly of a TGA8652EPU Surface Mount Package onto a Motherboard

Manual Assembly for Prototypes

1. Clean the motherboard or the similar module with Acetone and rinse with alcohol and DI water. Allow the circuit to fully dry.
2. Dispense Kester SN63 R-593 solder paste dots of 5 to 15mil in diameter to the motherboard as shown in the example motherboard in Figure 1 below. Assure that there is a minimum of 5mils and a maximum of 10 mils between the edge of each solder paste area and the closest edge of the ground pad.
3. Manually place a TGA8652EPU on the motherboard with correct orientation and good alignment. The alignment can be determined manually by centering the package on the motherboard. The RF traces are located in the center of the package and so are the center traces of the DC bias (Fig. 2)
4. Reflow the assembly on a hot plate with the surface temperature of the plate about 230°C for 5 to 6 seconds.
5. Let the assembly completely cool down. *This package has little or no tendency to self-align during the reflow.*
6. Clean the assembly with acetone and rinse with alcohol and DI water.

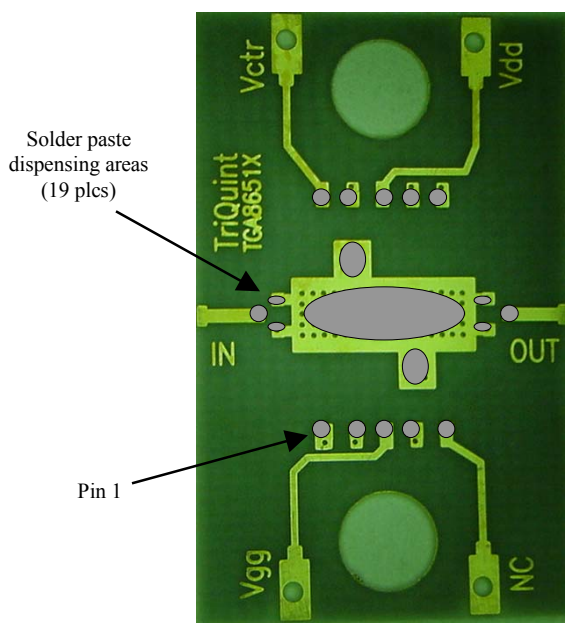


Figure 1: Solder paste dispensing pattern used on the evaluation board motherboard.

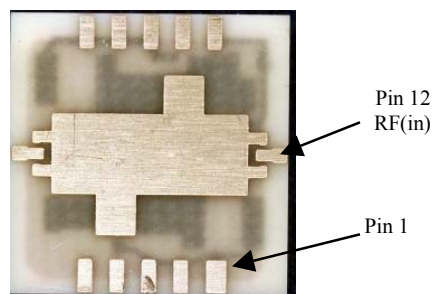


Figure 2: Bottom View [TGA8652-EPU]

High Volume Assembly of the Package

The TGA8652EPU is a standard surface mount component. High volume assembly can be performed using standard assembly processes including solder printing such as stencil solder printing. Pick-and-place using a standard machine such as a MRSI machine, and solder reflow using a "Sikama Reflow System" using typical zone temperatures: 120, 175, 195, and 215 degrees Celsius at 15 second intervals.

CAUTION: The TGA8652EPU contains GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

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