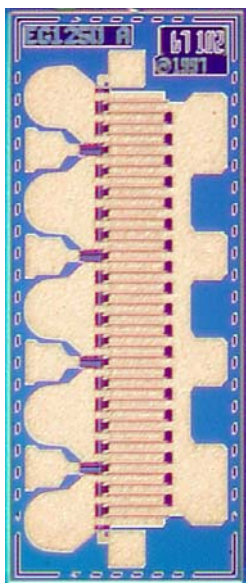


**DC - 10.5 GHz Discrete HFET****TGF4250-SCC****Key Features and Performance**

- Nominal Pout of 34 dBm at 8.5 GHz
- Nominal Gain of 8.5 dB at 8.5 GHz
- Nominal PAE of 53% at 8.5 GHz
- Suitable for high reliability applications
- 4800  $\mu\text{m}$  x 0.5  $\mu\text{m}$  FET
- Chip dimensions: 0.61 x 1.37 x 0.1 mm (0.024 x 0.054 x 0.004 in)
- Bias at 8 Volts, 384 mA

**Primary Applications**

- Cellular Base Stations
- High-reliability space
- Military

**Description**

The TriQuint TGF4250-SCC is a single gate 4.8 mm discrete GaAs Heterostructure Field Effect Transistor (HFET) designed for high efficiency power applications up to 10.5 GHz in Class A and Class AB operation. Typical performance at 2 GHz is 34 dBm power output, 13 dB gain, and 53% PAE.

Bond pad and backside metallization is gold plated for compatibility with eutectic alloy attach methods as well as thermocompression and thermosonic wire bonding processes. The TGF4250-SCC is readily assembled using automatic equipment.

For an Application Note on the use of HFETs, refer to the TriQuint website for the Millimeter Wave Division.



**TABLE I**  
**MAXIMUM RATINGS**

<b>SYMBOL</b>	<b>PARAMETER <u>1/</u></b>	<b>VALUE</b>	<b>NOTES</b>
$V_{DS}$	Drain to Source Voltage	12 V	
$V_{GS}$	Gate to Source Voltage Range	0 to -5.0 Volts	
$P_D$	Power Dissipation	See Thermal Data	
$T_{CH}$	Operating Channel Temperature	150°C	<u>2/</u> , <u>3/</u>
$T_{STG}$	Storage Temperature	-65 to 200°C	
$T_M$	Mounting Temperature (30 seconds)	320°C	

1/ These ratings represent the maximum values for this device. Stresses beyond those listed under “Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “DC Probe Characteristics” and “RF Probe Characteristics” is not implied. Exposure to maximum rated conditions for extended periods may affect device reliability.

2/ Junction temperature will directly affect the device Mean Time to Failure (MTTF). For maximum life, it is recommended that junction temperatures be maintained at the lowest possible levels.

3/ These ratings apply to each individual FET



**TABLE II**  
**DC PROBE CHARACTERISTICS**  
(T<sub>A</sub> = 25 °C, Nominal)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Note
I <sub>DSS</sub>	Saturated Drain Current	--	1176	--	mA	1/
G <sub>M</sub>	Transconductance	--	792	--	mS	1/
V <sub>P</sub>	Pinch-off Voltage	1	1.85	3	V	2/
V <sub>BGS</sub>	Breakdown Voltage Gate-Source	17	22	30	V	2/
V <sub>BGD</sub>	Breakdown Voltage Gate-Drain	17	22	30	V	2/

1/ Total for Four FETS

2/ V<sub>P</sub>, V<sub>BGS</sub>, and V<sub>BGD</sub> are negative.

**TABLE III**  
**ELECTRICAL CHARACTERISTICS**  
(T<sub>A</sub> = 25 °C, Nominal)  
Bias Conditions: V<sub>d</sub> = 8V, I<sub>d</sub> = 200mA +/- 10%

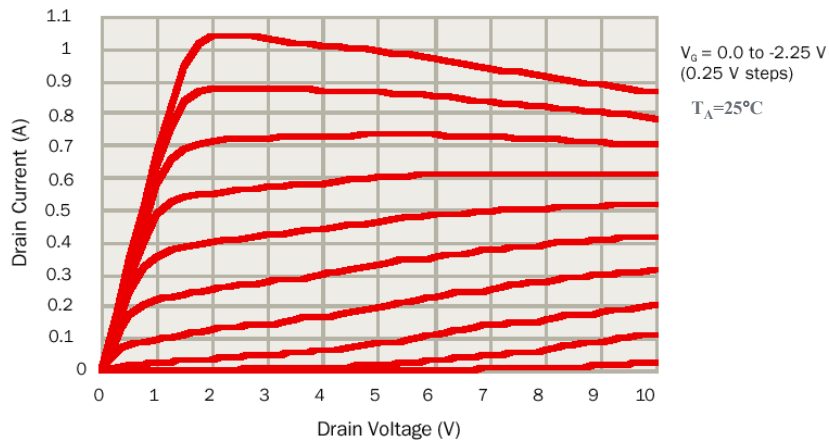
Symbol	Parameter	Typical	Unit
P <sub>out</sub>	Output Power	34	dBm
G <sub>p</sub>	Power Gain	8.5	dB
PAE	Power Added Efficiency	53	%

Note: The recommended bias current for HFETs is 80 mA/mm. For this 4.8 mm HFET I<sub>Q</sub> is 384 mA.

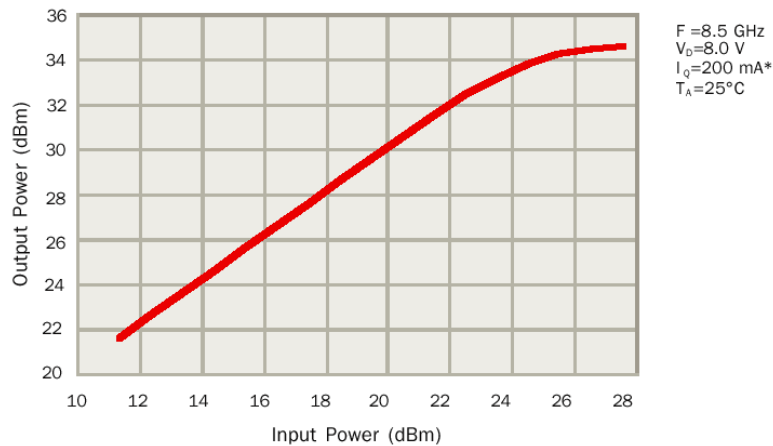


TYPICAL PERFORMANCE

EXAMPLE OF  
DC I-V CURVES

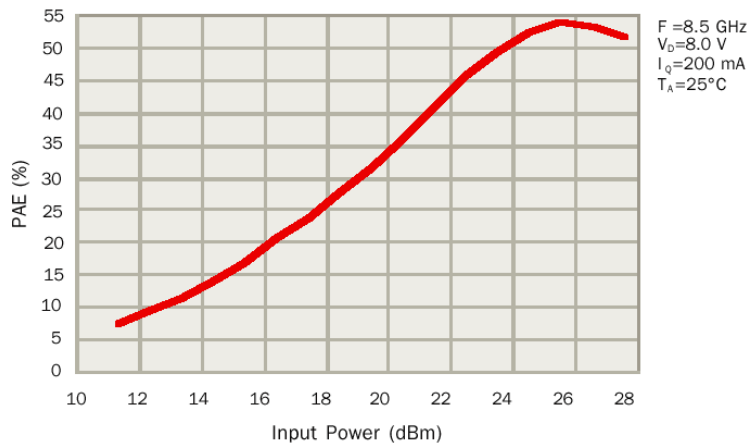


OUTPUT POWER  
VS. INPUT POWER



\*  $I_Q$  is defined as the drain current before application of RF signal at the input.

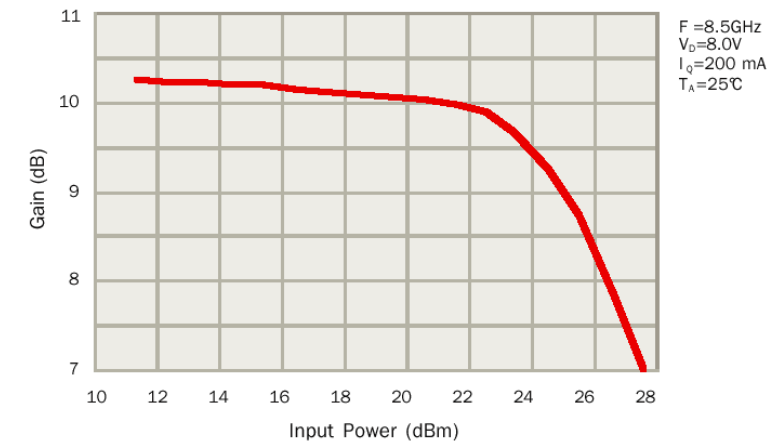
POWER ADDED  
EFFICIENCY VS.  
INPUT POWER



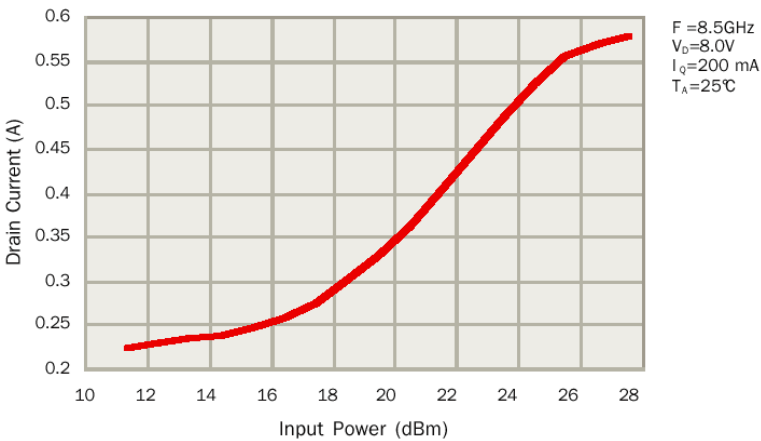


TYPICAL PERFORMANCE

GAIN VS.  
INPUT POWER



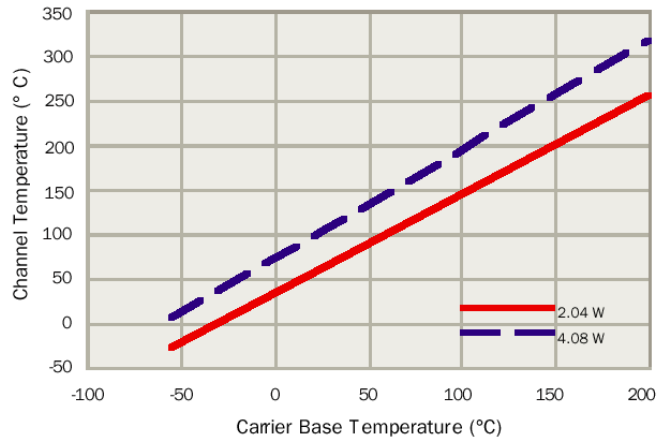
DRAIN CURRENT  
VS. INPUT POWER





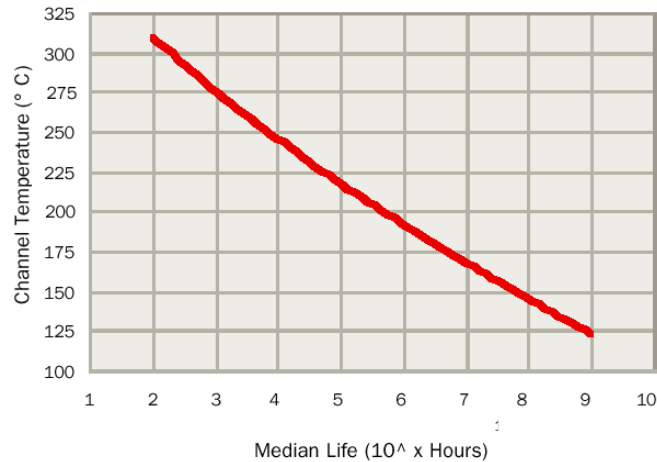
THERMAL INFORMATION

**PREDICTED CHANNEL  
TEMPERATURE VS.  
CARRIER BASE  
TEMPERATURE**  
at 2.04 W and 4.08 W  
dissipated power



38  $\mu$ m AuSn solder attach to 0.5 mm CuMo Carrier.

**HFET CHANNEL  
TEMPERATURE VS.  
MEDIAN LIFE**



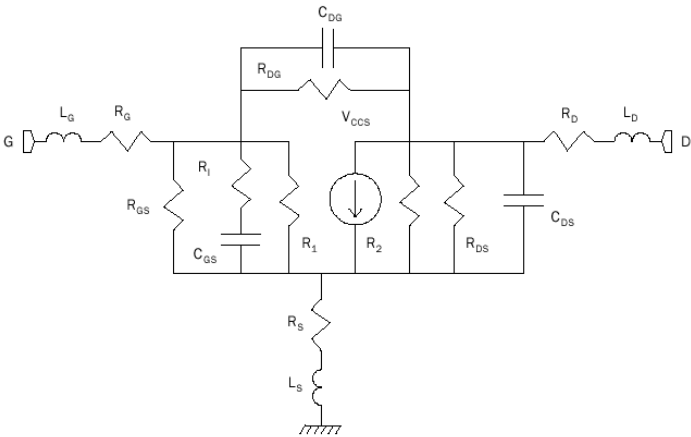


MODELED S-PARAMETERS

Frequency (GHz)	S <sub>11</sub>		S <sub>21</sub>		S <sub>12</sub>		S <sub>22</sub>	
	MAG	ANG(°)	MAG	ANG(°)	MAG	ANG(°)	MAG	ANG(°)
0.5	0.943	-106.98	9.887	122.68	0.026	35.10	0.533	-163.66
1.0	0.932	-139.41	5.725	103.61	0.030	19.75	0.591	-168.52
1.5	0.929	-152.35	3.935	94.21	0.031	13.81	0.608	-170.21
2.0	0.928	-159.14	2.978	87.84	0.031	10.87	0.617	-170.66
2.5	0.928	-163.31	2.386	82.79	0.031	9.25	0.625	-170.60
3.0	0.929	-166.14	1.984	78.43	0.030	8.38	0.633	-170.31
3.5	0.929	-168.18	1.694	74.50	0.030	8.00	0.641	-169.91
4.0	0.930	-169.74	1.474	70.85	0.029	7.98	0.650	-169.49
4.5	0.931	-170.97	1.302	67.41	0.029	8.27	0.659	-169.07
5.0	0.932	-171.97	1.163	64.14	0.028	8.84	0.668	-168.69
5.5	0.933	-172.82	1.048	61.02	0.028	9.67	0.678	-168.35
6.0	0.935	-173.54	0.952	58.01	0.027	10.77	0.688	-168.07
6.5	0.936	-174.17	0.870	55.13	0.026	12.13	0.698	-167.84
7.0	0.937	-174.73	0.800	52.35	0.026	13.74	0.708	-167.66
7.5	0.938	-175.23	0.738	49.67	0.025	15.62	0.718	-167.54
8.0	0.940	-175.69	0.684	47.09	0.025	17.75	0.728	-167.47
8.5	0.941	-176.12	0.637	44.61	0.024	20.12	0.738	-167.44
9.0	0.942	-176.51	0.594	42.22	0.024	22.72	0.748	-167.46
9.5	0.944	-176.88	0.556	39.92	0.024	25.51	0.757	-167.52
10.0	0.945	-177.23	0.521	37.70	0.024	28.46	0.767	-167.61
10.5	0.946	-177.57	0.490	35.58	0.023	31.54	0.776	-167.73

V<sub>DS</sub> = 8 V and 30% I<sub>DSS</sub> at T<sub>A</sub> = 25°C

LINEAR MODEL



V<sub>DS</sub> = 8.0 V and 30% I<sub>DSS</sub> at T = 25°C

FET Elements

L<sub>G</sub> = 0.010525 nH  
R<sub>G</sub> = 0.21075  
R<sub>GS</sub> = 20425  
R<sub>I</sub> = 0.3025  
C<sub>GS</sub> = 4.84 pF  
C<sub>DG</sub> = 0.4015 pF

R<sub>DG</sub> = 51000

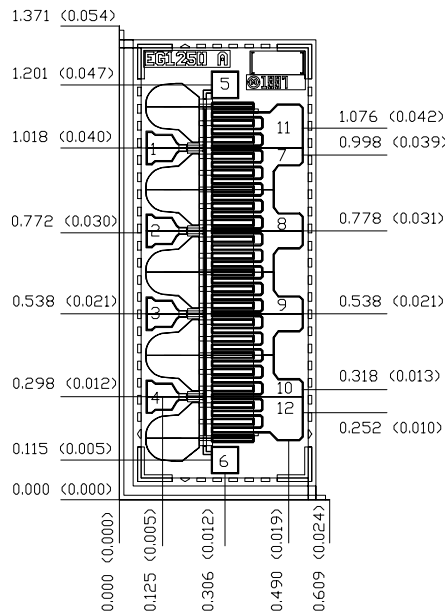
R<sub>S</sub> = 0.1  
L<sub>S</sub> = 0.011 nH  
R<sub>DS</sub> = 24.5025  
C<sub>DS</sub> = 1.013 pF  
R<sub>D</sub> = 0.165  
L<sub>D</sub> = 0.0055 nH

VCCS Parameters

M = 531.6 mS  
A = 0  
R1 = 1E19  
R2 = 1E19  
F = 0  
T = 5.49 pS



## Mechanical Drawing



Units: millimeters (inches)

Thickness: 0.1016 (0.004)

Chip edge to bond pad dimensions are shown to center of bond pad

Chip size tolerance: +/- 0.051 (0.002)

GND IS BACKSIDE OF MMIC

Bond Pad #1 (Gate 1)	0.075 x 0.075 (0.003 x 0.003)
Bond Pad #2 (Gate 2)	0.075 x 0.075 (0.003 x 0.003)
Bond Pad #3 (Gate 3)	0.075 x 0.075 (0.003 x 0.003)
Bond Pad #4 (Gate 4)	0.075 x 0.075 (0.003 x 0.003)
Bond Pad #5 (Gate) *	0.075 x 0.075 (0.003 x 0.003)*
Bond Pad #6 (Gate) *	0.075 x 0.075 (0.003 x 0.003)*
Bond Pad #7 (Drain 1)	0.089 x 0.089 (0.004 x 0.004)
Bond Pad #8 (Drain 2)	0.102 x 0.089 (0.004 x 0.004)
Bond Pad #9 (Drain 3)	0.102 x 0.089 (0.004 x 0.004)
Bond Pad #10 (Drain 4)	0.089 x 0.089 (0.004 x 0.004)
Bond Pad #11 (Drain) **	0.089 x 0.089 (0.004 x 0.004)**
Bond Pad #12 (Drain) **	0.089 x 0.089 (0.004 x 0.004)**

Minimum connections to Bond Pads 1 to 4 and 7 to 10.

\* Gate pad used when paralleling HFETS

\*\* Drain pad used paralleling HFETS

NOTE: Gate bias supplies should be designed to sink or source gate current.

The magnitude and direction of the gate current is a function of bias point, load impedance, and drive level.

**GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.**



## **Assembly Process Notes**

Reflow process assembly notes:

- Use AuSn (80/20) solder with limited exposure to temperatures at or above 300 °C for 30 sec
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- No fluxes should be utilized.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.
- Organic attachment can be used in low-power applications.
- Curing should be done in a convection oven; proper exhaust is a safety concern.
- Microwave or radiant curing should not be used because of differential heating.
- Coefficient of thermal expansion matching is critical.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonics are critical parameters.
- Aluminum wire should not be used.
- Discrete FET devices with small pad sizes should be bonded with 0.0007-inch wire.
- Maximum stage temperature is 200 °C.

***GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.***

***Note: Die are shipped in gel pack unless otherwise specified.***