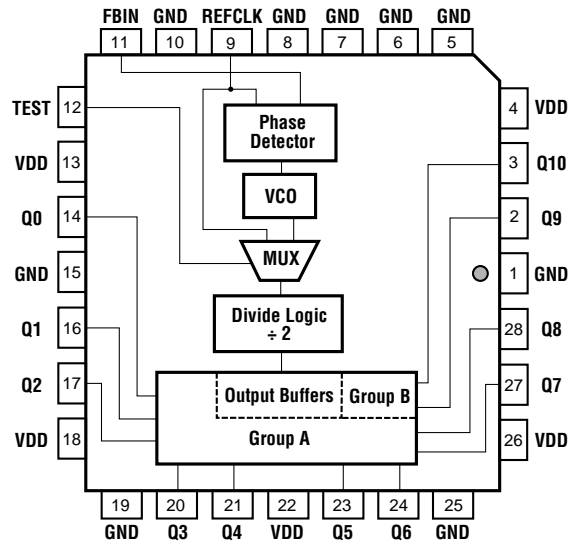


Figure 1. Block Diagram



TriQuint's TQ1089 is a configurable clock buffer which generates 11 outputs, operating over a wide range of frequencies from 65 MHz to 90 MHz and from 130 MHz to 180 MHz. The outputs are available at either 1x and 2x or at 1x and  $\frac{1}{2}$  x the reference clock frequency,  $f_{REF}$ . When one of the Group A outputs (Q0–Q8) is used as feedback to the PLL, all Group A outputs will be at  $f_{REF}$ , and all Group B outputs (Q9, Q10) will be at  $2 \times f_{REF}$ . When one of the Group B outputs is used as feedback to the PLL, all Group A outputs will be at  $\frac{1}{2} \times f_{REF}$  and all Group B outputs will be at  $f_{REF}$ .

A very stable internal Phase-Locked Loop (PLL) provides low-jitter operation. This completely self-contained PLL requires no external capacitors or resistors. The PLL's Voltage-Controlled Oscillator (VCO) has a frequency range from 260 MHz to 360 MHz. By feeding back one of the output clocks to FBIN, the PLL continuously maintains frequency and phase synchronization between the reference clock (REFCLK) and each of the outputs.

TriQuint's patented output buffer design delivers a very low output-to-output skew of 150 ps (max). The TQ1089's symmetrical TTL outputs are capable of sourcing and sinking 30 mA.

## TQ1089

### 11-Output Configurable Clock Buffer

#### Features

- Wide frequency range:  
65 MHz to 90 MHz and  
130 MHz to 180 MHz
- Output configurations:  
eight outputs at  $f_{REF}$   
two outputs at  $2 \times f_{REF}$  or  
nine outputs at  $\frac{1}{2} \times f_{REF}$   
one output at  $f_{REF}$
- Low output-to-output skew:  
150 ps (max) within a group
- Near-zero propagation delay  
 $-350 \text{ ps} \pm 500 \text{ ps (max)}$  or  
 $-350 \text{ ps} \pm 700 \text{ ps (max)}$
- TTL-compatible with 30 mA  
output drive
- 28-pin J-lead surface-mount  
package
- Ideal for PowerPC™-based  
designs

## Functional Description

The core of the TQ1089 is a Phase-Locked Loop (PLL) that continuously compares the reference clock (REFCLK) to the feedback clock (FBIN), maintaining a zero frequency difference between the two. Since one of the outputs is always connected to FBIN, the PLL keeps the propagation delay between the outputs and the reference clock within  $-350 \text{ ps} \pm 500 \text{ ps}$  for the TQ1089-MC500, and within  $-350 \text{ ps} \pm 700 \text{ ps}$  for the TQ1089-MC700.

The internal Voltage-Controlled Oscillator (VCO), has an operating range of 260 MHz to 360 MHz, as shown in Table 1. The combination of the VCO and the Divide Logic enables the TQ1089 to operate between 65 MHz and 90 MHz and from 130 MHz to 180 MHz.

In the test mode, the PLL is bypassed and REFCLK is connected directly to the Divide Logic block via the MUX, as shown in Figure 1. This mode is useful for debug and test purposes. The test mode is outlined in Table 2.

The maximum rise and fall time at the output pins is 1.4 ns. All outputs of the TQ1089 are TTL-compatible with 30 mA symmetric drive and a minimum  $V_{OH}$  of 2.4 V.

## Power Up/Reset Synchronization

After power up or reset, the PLL requires time before it achieves synchronization lock. The maximum time required for synchronization (TSYNC) is 500 ms.

**Table 1. Frequency Mode Selection**

Test	Output Feedback	Mode	Reference Clock Frequency Range	Output Frequency Range	
				Group A: Q0–Q8	Group B: Q9, Q10
0	Group B	$\div 2$	130 MHz – 180 MHz	65 MHz – 90 MHz	130 MHz – 180 MHz
0	Group A	$\div 4$	65 MHz – 90 MHz	65 MHz – 90 MHz	130 MHz – 180 MHz

**Table 2. Test Mode Selection**

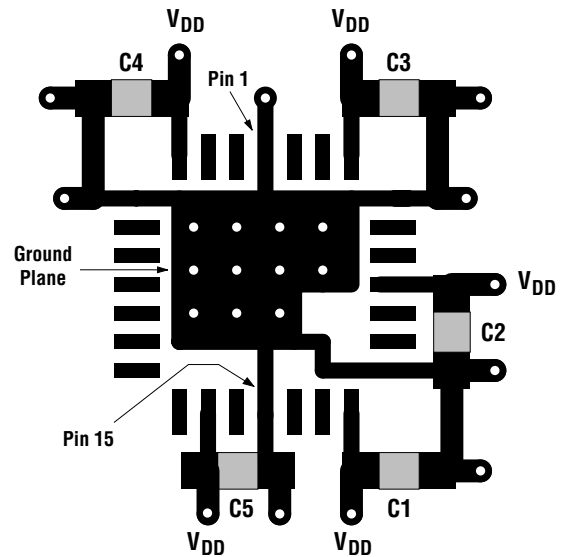
Test	Mode	Ref. Clock	Group A	
			Outputs Q0–Q8	Group B Outputs Q9, Q10
1	$\div 2$	$f_{REF}$	$f_{REF} \div 4$	$f_{REF} \div 2$

### Layout Guidelines

Multiple ground and power pins on the TQ1089 reduce ground bounce. Good layout techniques, however, are necessary to guarantee proper operation and to meet the specifications across the full operating range. TriQuint recommends bypassing each of the  $V_{DD}$  supply pins to the nearest ground pin, as close to the chip as possible.

Figure 2 shows the recommended power layout for the TQ1089. The bypass capacitors should be located on the same side of the board as the TQ1089. The  $V_{DD}$  traces connect to an inner-layer  $V_{DD}$  plane. All of the ground pins (GND) are connected to a small ground plane on the surface beneath the chip. Multiple through holes connect this small surface plane to an inner-layer ground plane. The capacitors (C1–C5) are 0.1 mF. TriQuint's test board uses X7R temperature-stable capacitors in 1206 SMD cases.

**Figure 2. Top Layer Layout of Power Pins**  
(Approx. 3.3x)



## TQ1089

### Absolute Maximum Ratings <sup>1</sup>

Storage temperature	–65 °C to +150 °C
Ambient temperature with power applied <sup>2</sup>	–55 °C to +100 °C
Supply voltage to ground potential	–0.5 V to +7.0 V
DC input voltage	–0.5 V to +(V <sub>DD</sub> + 0.5)V
DC input current	–30 mA to +5 mA
Package thermal resistance (MQuad)	θ <sub>JA</sub> = 45 °C/W
Die junction temperature	T <sub>J</sub> = 150 °C

### DC Characteristics

(V<sub>DD</sub> = +5 V ± 5%, T<sub>A</sub> = 0 °C to +70 °C) <sup>3</sup>

Symbol	Description	Test Conditions	Min	Limits <sup>4</sup> Typ	Max	Unit
V <sub>OHT</sub>	Output HIGH voltage	V <sub>DD</sub> = Min I <sub>OH</sub> = –30 mA V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	2.4	3.4		V
V <sub>OHC</sub>	Output HIGH voltage	V <sub>DD</sub> = Min I <sub>OH</sub> = –1 mA V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	3.2	4.1		V
V <sub>OL</sub>	Output LOW voltage	V <sub>DD</sub> = Min I <sub>OL</sub> = 30 mA V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>		0.27	0.5	V
V <sub>IH</sub> <sup>5</sup>	Input HIGH level	Guaranteed input logical HIGH Voltage for all Inputs	2.0			V
V <sub>IL</sub> <sup>5</sup>	Input LOW level	Guaranteed input logical LOW Voltage for all inputs			0.8	V
I <sub>IL</sub>	Input LOW current	V <sub>DD</sub> = Max V <sub>IN</sub> = 0.40 V		–156	–400	μA
I <sub>IH</sub>	Input HIGH current	V <sub>DD</sub> = Max V <sub>IN</sub> = 2.7 V		0	25	μA
I <sub>I</sub>	Input HIGH current	V <sub>DD</sub> = Max V <sub>IN</sub> = 5.5 V		2	1000	μA
I <sub>DD</sub> <sup>6</sup>	Power supply current	V <sub>DD</sub> = Max		119	170	mA
V <sub>I</sub>	Input clamp voltage	V <sub>DD</sub> = Min I <sub>IN</sub> = –18 mA		–0.70	–1.2	V

### Capacitance

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
C <sub>IN</sub> <sup>3,7</sup>	Input capacitance	V <sub>IN</sub> = 2.0 V at f = 1 MHz		6		pF

- Notes: 1. Exceeding these parameters may damage the device.  
2. Maximum ambient temperature with device not switching and unloaded.  
3. These values apply to both TQ1089-MC500 and TQ1089-MC700.  
4. Typical limits are at V<sub>DD</sub> = 5.0 V and T<sub>A</sub> = 25 °C.  
5. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.  
6. This parameter is measured with device not switching and unloaded.  
7. These parameters are not 100% tested, but are periodically sampled.

**AC Characteristics**

( $V_{DD} = +5\text{ V} \pm 5\%$ ,  $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ )

Symbol	Input Clock (REFCLK)	Test Conditions (Figure 3) <sup>1</sup>	Min	Typ	Max	Unit
$t_{CPWH}$	CLK pulse width HIGH	Figure 4	3	---	---	ns
$t_{CPWL}$	CLK pulse width LOW	Figure 4	3	---	---	ns
$t_{IR}$	Input rise time (0.8 V - 2.0V)		---	---	2.0	ns

Symbol	Output Clocks (Q0–Q10)	Test Conditions (Figure 3) <sup>1</sup>	Min	Typ	Max	Unit
$t_{OR}, t_{OF}$	Rise/fall time (0.8 V – 2.0V)	Figure 4	350	---	1400	ps
$t_{PD1}$ <sup>2</sup>	CLK $\uparrow$ to FBIN $\uparrow$ (TQ1089-MC500)	Figure 4	–850	–350	+150	ps
$t_{PD2}$ <sup>2</sup>	CLK $\uparrow$ to FBIN $\uparrow$ (TQ1089-MC700)	Figure 4	–1050	–350	+350	ps
$t_{SKEW1}$ <sup>3</sup>	Rise–rise, fall–fall (within group)	Figure 5	---	60	150	ps
$t_{SKEW2}$ <sup>3</sup>	Rise–rise, fall–fall (group-to-group, aligned)	Figure 6 (skew 2 takes into account skew 1)	---	75	350	ps
$t_{SKEW3}$ <sup>3</sup>	Rise–rise, fall–fall (group-to-group, non-aligned)	Figure 7 (skew 3 takes into account skews 1, 2)	---	---	650	ps
$t_{SKEW4}$ <sup>3</sup>	Rise–fall, fall–rise	Figure 8 (skew 4 takes into account skew 3)	---	---	1200	ps
$t_{CYC}$ <sup>4</sup>	Duty-cycle Variation	Figure 4	–1000	0	+1000	ps
$t_{JP}$ <sup>5</sup>	Period-to-Period Jitter	Figure 4	---	80	200	ps
$t_{JR}$ <sup>5</sup>	Random Jitter	Figure 4	---	190	400	ps
$t_{SYNC}$ <sup>6</sup>	Synchronization Time		---	10	500	$\mu\text{s}$

Notes: 1. All measurements are tested with a REFCLK having a rise time of 0.5 ns (0.8 V to 2.0 V).

2. The PLL maintains alignment of CLK and FBIN at all times. This specification applies to the rising edge only because the input duty cycle can vary while the output duty cycle is typically 50/50. The delay  $t_{PD}$  is measured at the 1.5 V level between CLK and FBIN.

3. Skew specifies the width of the window in which outputs switch, and is measured at 1.5 V.

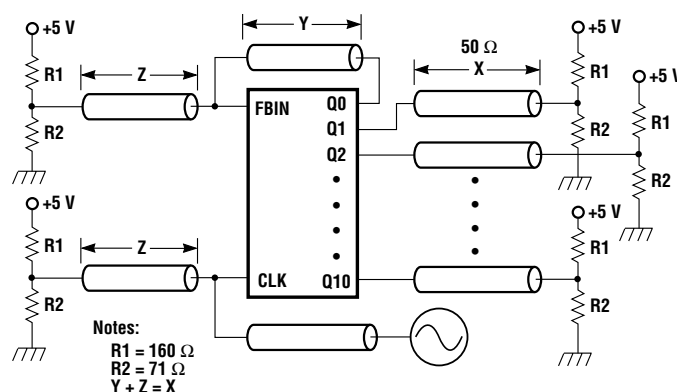
4. This specification represents the deviation from 50/50 on the outputs.

5. Jitter specifications refer to peak-to-peak value.  $t_{JR}$  is the jitter on the output with respect to the reference clock.

$t_{JP}$  is the jitter on the output with respect to the output's previous rising edge.

6.  $t_{SYNC}$  is the time required for the PLL to synchronize; this assumes the presence of a CLK signal and a connection from one of the outputs to FBIN.

**Figure 3. AC Test Circuit**



## Switching Waveforms

Figure 4. General Timing

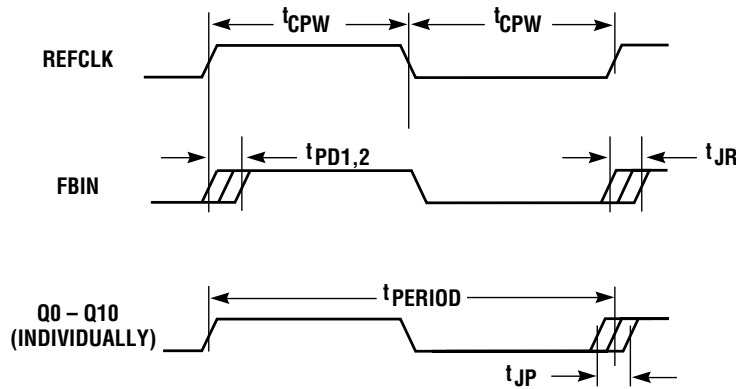


Figure 5.  $t_{SKEW1}$

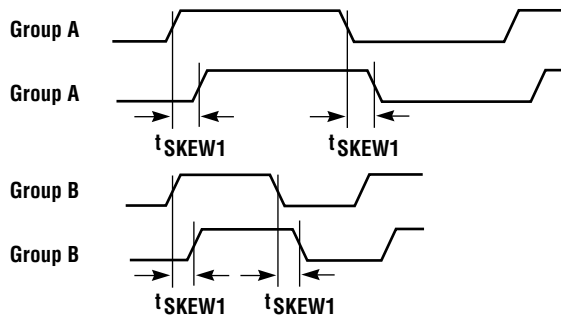


Figure 7.  $t_{SKEW3}$

(For Group A Feedback)

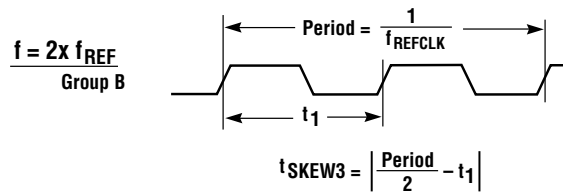


Figure 6.  $t_{SKEW2}$

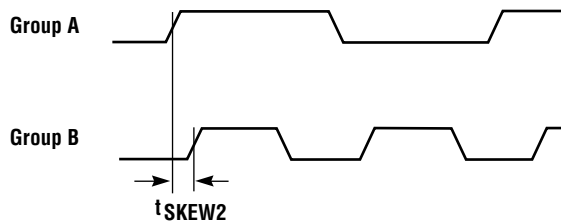
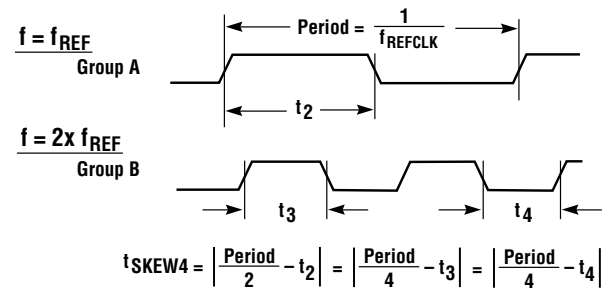
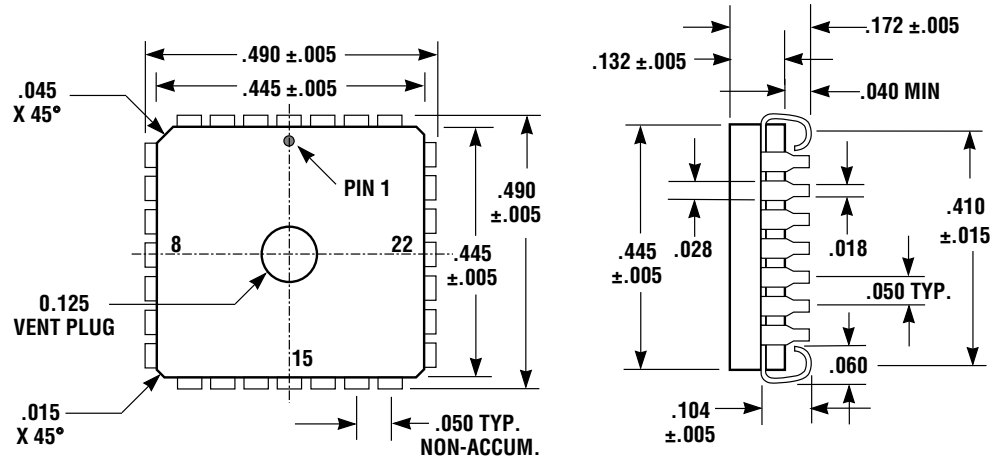


Figure 8.  $t_{SKEW4}$



## 28-Pin MQuad J-Leaded Package Mechanical Specification

(All dimensions are in inches)



## 28-Pin MQuad Pin Description

Pin #	Pin Name	Description	I/O
1	GND	Ground	—
2	Q9	Output Clock 9 (B1)	O
3	Q10	Output Clock 10 (B2)	O
4	VDD	+5 V	—
5	GND	Ground	—
6	GND	Ground	—
7	GND	Ground	—
8	GND	Ground	—
9	REFCLK	Reference Clock	I
10	GND	Ground	—
11	FBIN	Feedback In	I
12	TEST	Test	I
13	VDD	+5 V	—
14	Q0	Output Clock 0 (A1)	O

Pin #	Pin Name	Description	I/O
15	GND	Ground	—
16	Q1	Output Clock 1 (A2)	O
17	Q2	Output Clock 2 (A3)	O
18	VDD	+5 V	—
19	GND	Ground	—
20	Q3	Output Clock 3 (A4)	O
21	Q4	Output Clock 4 (A5)	O
22	VDD	+5 V	—
23	Q5	Output Clock 5 (A6)	O
24	Q6	Output Clock 6 (A7)	O
25	GND	Ground	—
26	VDD	+5 V	—
27	Q7	Output Clock 7 (A8)	O
28	Q8	Output Clock 8 (A9)	O

SYSTEM TIMING  
PRODUCTS

## Output Characteristics

The IV characteristics, transition times, package characteristics, device and bond wire characteristics for the TQ1089 are described in Tables 4 through 9 and Figures 9 through 11.

These output characteristics are provided for modelling purposes only. TriQuint does not guarantee the information in these tables and figures.

Figure 9.  $I_{OH}$  vs.  $V_{OH}$

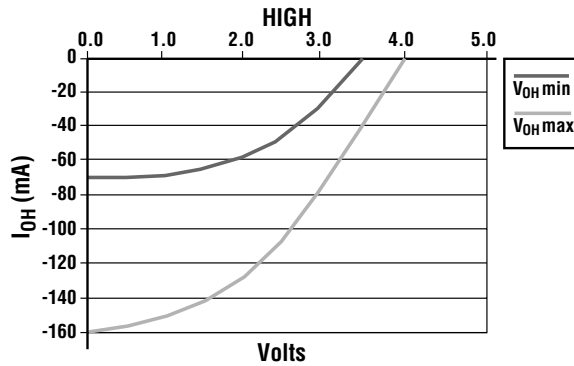


Table 4.  $I_{OH}$  vs.  $V_{OH}$

$V_{OH}$	$I_{OH} \text{ min (mA)}$	$I_{OH} \text{ max (mA)}$
0.0	-70	-160
0.5	-70	-157
1.0	-68	-152
1.5	-65	-142
2.0	-59	-130
2.5	-48	-106
3.0	-29	-79
3.5	0	-42
4.0	0	0
4.5	0	0
5.0	0	0
5.5	40	120
6.0	90	265
6.5	115	350
7.0	135	410
7.5	145	435

Figure 10.  $I_{OL}$  vs.  $V_{OL}$

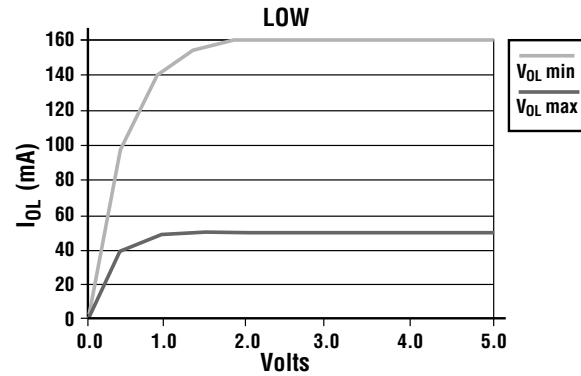


Table 5.  $I_{OL}$  vs.  $V_{OL}$

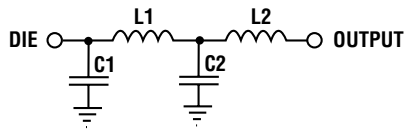
$V_{OL}$	$I_{OL} \text{ min (mA)}$	$I_{OL} \text{ max (mA)}$
-2.5	-145	-435
-2.0	-135	-410
-1.5	-115	-350
-1.0	-90	-265
-0.5	-40	-120
0.0	0	0
0.5	37	97
1.0	49	140
1.5	53	155
2.0	54	157
2.5	54	159
3.0	54	160
3.5	54	160
4.0	54	160
4.5	54	160
5.0	54	160
10.0	54	160



**Table 6. Above- $V_{DD}$  and Below-Ground Characteristics**

Diode to GND V	I (mA)	Diode Stack to VDD V	I (mA)
0.0	0	5.0	0
-0.4	0	5.4	0
-0.5	0	5.5	0
-0.6	-5	5.6	5
-0.7	-15	5.7	15
-0.8	-35	5.8	35
-0.9	-55	5.9	55
-1.0	-75	6.0	75
-2.0	-300	7.0	300
-2.5	-350	7.5	350
-3.0	-360	8.0	360

Note: TriQuint does not guarantee diode operation for purposes other than ESD protection.

**Figure 11. Output Model****Table 7. Device and Bond-Wire Characteristics (Estimated)**

L1	C1
2 nH	10 pF

**Table 8. 28-Pin MQuad Package Characteristics**

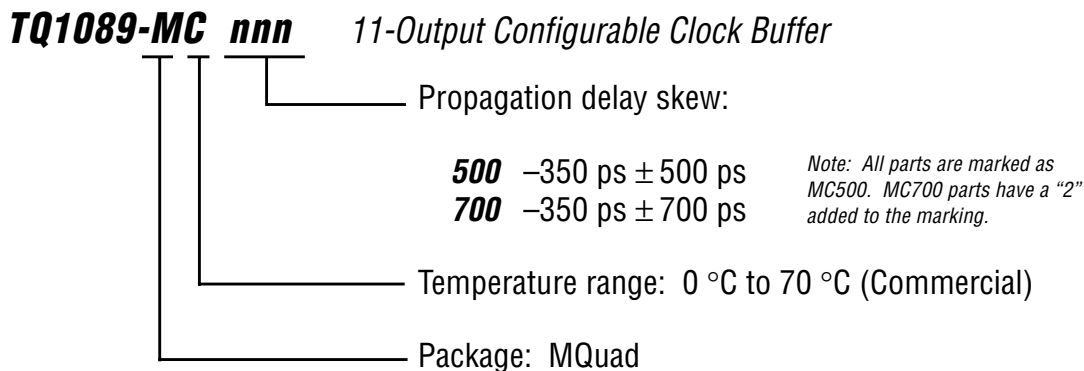
L2	C2
1.85 nH	0.40 pF

**Table 9. Rise and Fall Times (Into 0 pF, 50 Ohms to 1.5 V)**

Time (ns)	$T_R$ min (V)	$T_R$ max (V)	$T_F$ min (V)	$T_F$ max (V)
0.0	0.15	0.32	3.20	3.04
0.1	0.15	0.32	3.20	3.04
0.2	0.16	0.32	3.06	2.95
0.3	0.18	0.32	2.86	2.90
0.4	0.23	0.32	2.62	2.68
0.5	0.26	0.32	2.38	2.50
0.6	0.34	0.32	2.17	2.36
0.7	0.46	0.34	2.00	2.22
0.8	0.67	0.39	1.85	2.09
0.9	0.89	0.49	1.69	1.95
1.0	1.12	0.63	1.52	1.86
1.1	1.32	0.86	1.38	1.68
1.2	1.50	1.09	1.26	1.59
1.3	1.73	1.27	1.12	1.49
1.4	1.93	1.45	0.96	1.36
1.5	2.15	1.64	0.83	1.23
1.6	2.75	2.23	0.52	0.95
1.7	2.58	2.00	0.61	1.00
1.8	2.75	2.23	0.52	0.95
1.9	2.90	2.41	0.45	0.91
2.0	3.02	2.50	0.39	0.86
2.1	3.12	2.64	0.33	0.77
2.2	3.17	2.77	0.29	0.73
2.3	3.19	2.86	0.24	0.68
2.4	3.20	2.95	0.21	0.64
2.5	3.20	2.99	0.19	0.59
2.6	3.20	3.02	0.17	0.55
2.7	3.20	3.02	0.16	0.53
2.8	3.20	3.04	0.16	0.50
2.9	3.20	3.04	0.15	0.45
3.0	3.20	3.04	0.15	0.41
3.1	3.20	3.04	0.15	0.40
3.2	3.20	3.04	0.15	0.37
3.3	3.20	3.04	0.15	0.36
3.4	3.20	3.04	0.15	0.32
3.5	3.20	3.04	0.15	0.32

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