

The TQ8032 is a non-blocking 32 x 32 digital crosspoint switch capable of 800 Megabits per second per port data rates. Utilizing a fully differential internal data path and ECL I/O, the TQ8032 offers a high data rate with exceptional signal fidelity. The symmetrical switching and noise rejection characteristics inherent in differential logic result in low jitter and signal skew. The TQ8032 is ideally suited for digital video, data communications and telecommunication switching applications.

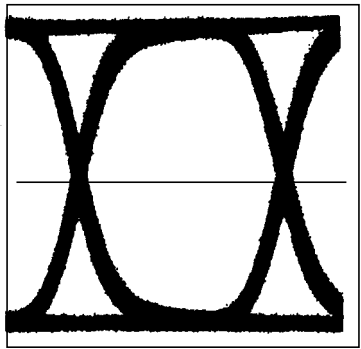
The non-blocking architecture uses 32 fully independent 32:1 multiplexers (see diagram on page 2), allowing each output port to be independently programmed to any input port. The switch is configured by sequentially loading each multiplexer's 5-bit program latch (OA0:4) with the desired input port address (IA0:4) and enabling the LOAD pin. When complete, the CONFIGURE pin is strobed and all new configurations are simultaneously transferred into the switch multiplexers. Data integrity is maintained on all unchanged data paths.

### Electrical Characteristics

	Min	Max	Units
Data Rate/Port	800		Mb/s
Jitter		150	ps pk-pk
Channel Propagation Delay		2300	ps
Ch-to-Ch Propagation Delay Skew		500	ps

## TQ8032

### 800 Megabit/sec 32x32 Digital ECL Crosspoint Switch



Typical output waveform with all channels driven

### Features

- >25 Gb/s aggregate BW
- 800 Mb/s/port NRZ data rate
- Non-blocking architecture
- 500 ps delay match
- Differential ECL-level data I/O; Selectable CMOS/TTL-level control inputs
- Low jitter and signal skew
- Fully differential data path
- Double buffered configuration latches
- 196-pin CQFP package

### Applications

- Telecom/Datacom Switching
- Hubs and Routers
- Video Switching

Figure 1. Architecture

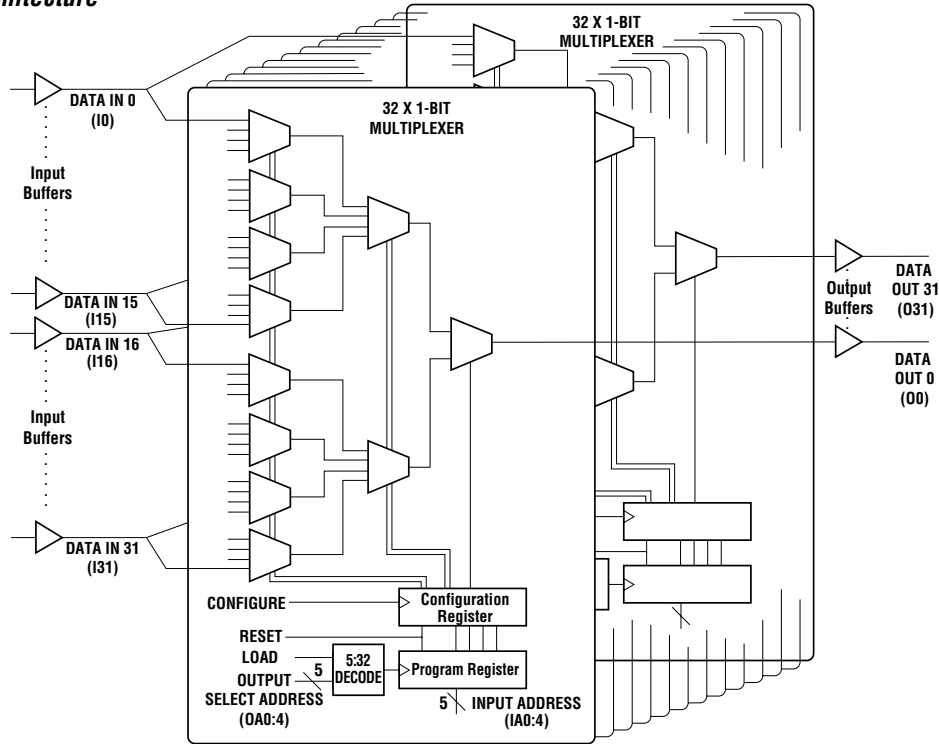


Table 2. Pin Descriptions

Signal	Name/Level	Description																																				
I0 to I31, NI0 to NI31	Data input true and complement. Differential ECL	Differential data input ports.																																				
O0 to O31, NO0 to NO31	Data output true and complement. Differential ECL	Differential data output ports.																																				
IA0:4	Input address. CMOS/TTL	Input port selection address that is written into the selected output port program latches (OA0:4).																																				
<table><tr><td>IA4</td><td>IA3</td><td>IA2</td><td>IA1</td><td>IA0</td><td>Input port</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>2</td></tr><tr><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>31</td></tr></table>			IA4	IA3	IA2	IA1	IA0	Input port	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	0	2	:	:	:	:	:	:	1	1	1	1	1	31
IA4	IA3	IA2	IA1	IA0	Input port																																	
0	0	0	0	0	0																																	
0	0	0	0	1	1																																	
0	0	0	1	0	2																																	
:	:	:	:	:	:																																	
1	1	1	1	1	31																																	
OA0:4 CMOS/TTL	Output select address.	Output port selection address. Selects the output port program latches to which the input port selection address (IA0:4) is written.																																				
<table><tr><td>OA4</td><td>OA3</td><td>OA2</td><td>OA1</td><td>OA0</td><td>Output port</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>2</td></tr><tr><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td><td>:</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>31</td></tr></table>			OA4	OA3	OA2	OA1	OA0	Output port	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	0	2	:	:	:	:	:	:	1	1	1	1	1	31
OA4	OA3	OA2	OA1	OA0	Output port																																	
0	0	0	0	0	0																																	
0	0	0	0	1	1																																	
0	0	0	1	0	2																																	
:	:	:	:	:	:																																	
1	1	1	1	1	31																																	

Figure 2. Package Pinout

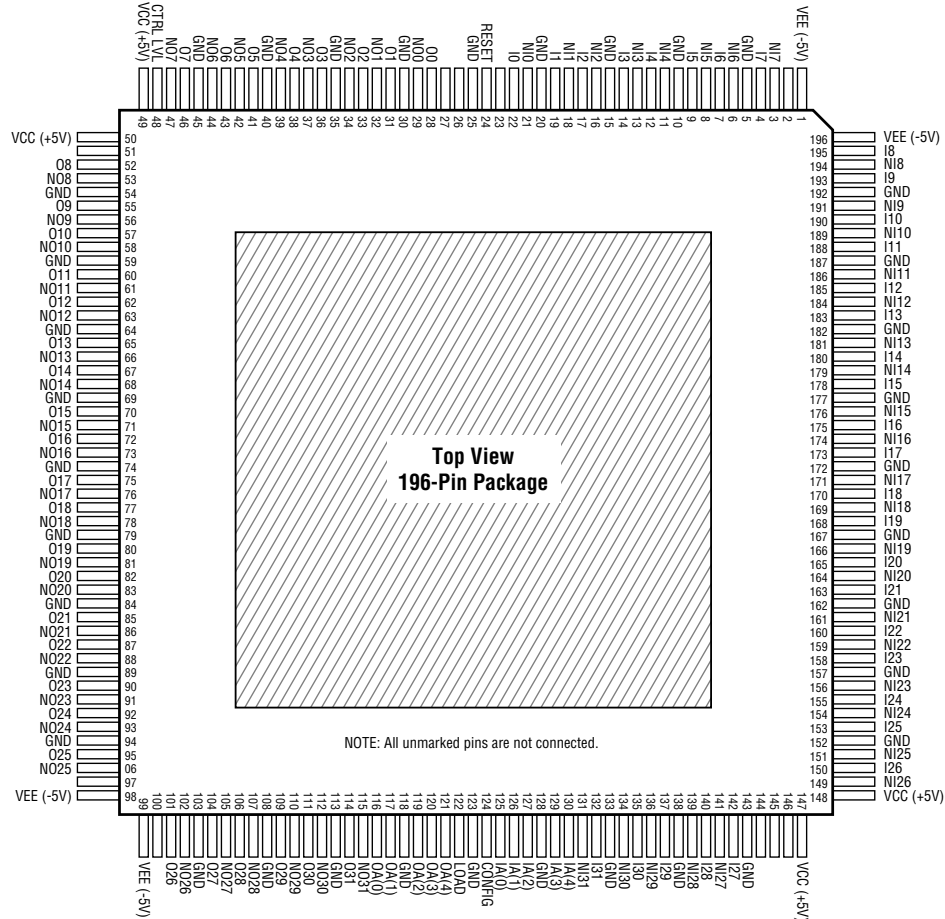


Table 2. Pin Descriptions (continued)

Signal	Name/Level	Description
LOAD	CMOS/TTL Latches the data when set to a 'low' level.	Enables the selected output port program latches while set 'high'.
CONFIGURE	CMOS/TTL	Transfers the program latches data to the configuration latches and implements the switch changes while set "high." Latches the data when set to a "low" level.
RESET	CMOS/TTL	Puts the switch into <i>Broadcast</i> or <i>Pass-Through</i> configuration, overwriting existing configurations. <b>Broadcast mode:</b> All output ports are connected to data input port 0. This mode is selected by applying a RESET "high" pulse with CONFIGURE held "low." <b>Pass-through mode:</b> IO is connected to O0, I1 to O1, etc. This mode is selected by applying a RESET "high" pulse with CONFIGURE held "high."
CNTRL LVL	Input level control. GND/Open	Selects the input levels for the input address (IA0:4), output address(OA0:4), CONFIGURE, LOAD and RESET inputs. Inputs are configured for TTL when tied to GND and CMOS when left unconnected.

**Table 3. Absolute Maximum Ratings<sup>5</sup>**

Symbol	Parameter	Absolute Max. Rating	Notes
T <sub>STOR</sub>	Storage Temperature	–65° C to +150° C	
T <sub>CH</sub>	Junction (Channel) Temperature	–65° C to +150° C	1
T <sub>C</sub>	Case Temperature Under Bias	–65° C to +125° C	2
V <sub>CC</sub>	Supply Voltage	0 V to +7 V	3
V <sub>EE</sub>	Supply Voltage	–7 V to 0 V	3
V <sub>TT</sub>	Load Termination Supply Voltage	V <sub>EE</sub> to 0 V	4
V <sub>IN</sub>	Voltage Applied to Any ECL Input; Continuous	V <sub>EE</sub> –0.5 V to +0.5 V	
I <sub>IN</sub>	Current Into Any ECL Input; Continuous	–1.0 mA to +1.0 mA	
V <sub>IN</sub>	Voltage Applied to Any TTL/CMOS Input; Continuous	–0.5 V to V <sub>CC</sub> +0.5 V	
I <sub>IN</sub>	Current Into Any TTL/CMOS Input; Continuous	–1.0 mA to +1.0 mA	
V <sub>OUT</sub>	Voltage Applied to Any ECL Output	V <sub>EE</sub> –0.5 V to +0.5 V	4
I <sub>OUT</sub>	Current From Any ECL Output; Continuous	–40 mA	
P <sub>D</sub>	Power Dissipation per Output P <sub>OUT</sub> = (GND – V <sub>OUT</sub> ) x I <sub>OUT</sub>	50 mW	

Notes: 1. For die applications.

2. T<sub>C</sub> is measured at case top.

3. All voltages specified with respect to GND, defined as 0V.

4. Subject to I<sub>OUT</sub> and power dissipation limitations.

5. Absolute maximum ratings, as detailed in this table, are the ratings beyond which the device's performance may be impaired and/or permanent damage to the device may occur.

**Table 4. Recommended Operating Conditions<sup>4</sup>**

Symbol	Parameter	Min	Typ	Max	Units	Notes
T <sub>C</sub>	Case Operating Temperature	0		85	°C	1,3
V <sub>CC</sub>	Supply Voltage	4.5		5.5	V	
V <sub>EE</sub>	Supply Voltage	–5.5		–4.5	V	
V <sub>TT</sub>	Load Termination Supply Voltage		–2.0		V	2
R <sub>LOAD</sub>	Output Termination Load Resistance		50		Ω	2
Θ <sub>JC</sub>	Thermal Resistance Junction to Case			2	°C/W	

Notes: 1. T<sub>C</sub> measured at case top. Use of adequate heatsink is required.

2. The V<sub>TT</sub> and R<sub>LOAD</sub> combination is subject to maximum output current and power restrictions.

3. Contact the Factory for extended temperature range applications.

4. Functionality and/or adherence to electrical specifications is not implied when the device is subjected to conditions that exceed, singularly or in combination, the operating range specified.

**Table 5. DC Characteristics<sup>1,2</sup>** – Within recommended operating conditions, unless otherwise indicated.

Symbol	Parameter	Min	Max	Units	Test Cond.	Notes
V <sub>IH</sub>	ECL Input Voltage High	–1100	–500	mV		
V <sub>IL</sub>	ECL Input Voltage Low	V <sub>TT</sub>	–1500	mV		
I <sub>IH</sub>	ECL Input Current High		+30	μA	V <sub>IH</sub> = –0.7 V	
I <sub>IL</sub>	ECL Input Current Low		–30	μA	V <sub>IL</sub> = –2.0 V	
V <sub>ICM</sub>	ECL Input Common Mode Voltage	–1500	–1100	mV		
V <sub>IDIF</sub>	ECL Input Differential Voltage (pk-pk)	400	1200	mV		
V <sub>IH</sub>	CMOS/TTL Input Voltage High	3.5/2.0	V <sub>CC</sub> /V <sub>CC</sub>	V		2
V <sub>IL</sub>	CMOS/TTL Input Voltage Low	0/0	1.5/0.8	V		2
I <sub>IH</sub>	CMOS/TTL Input Current High		+100	μA	V <sub>IH</sub> = V <sub>CC</sub>	2
I <sub>IL</sub>	CMOS/TTL Input Current Low		–100	μA	V <sub>IL</sub> = 0 V	2
V <sub>OCM</sub>	ECL Output Common Mode	–1500	–1100	mV		
V <sub>ODIF</sub>	ECL Output Differential Voltage	600		mV		
V <sub>OH</sub>	ECL Output Voltage High	–1000	–600	mV		
V <sub>OL</sub>	ECL Output Voltage Low	V <sub>TT</sub>	–1600	mV		
I <sub>OH</sub>	ECL Output Current High	20	27	mA		
I <sub>OL</sub>	ECL Output Current Low	0	8	mA		
I <sub>CC</sub>	Power Supply Current (+)		20	mA		
I <sub>EE</sub>	Power Supply Current (–)		–1950	mA		

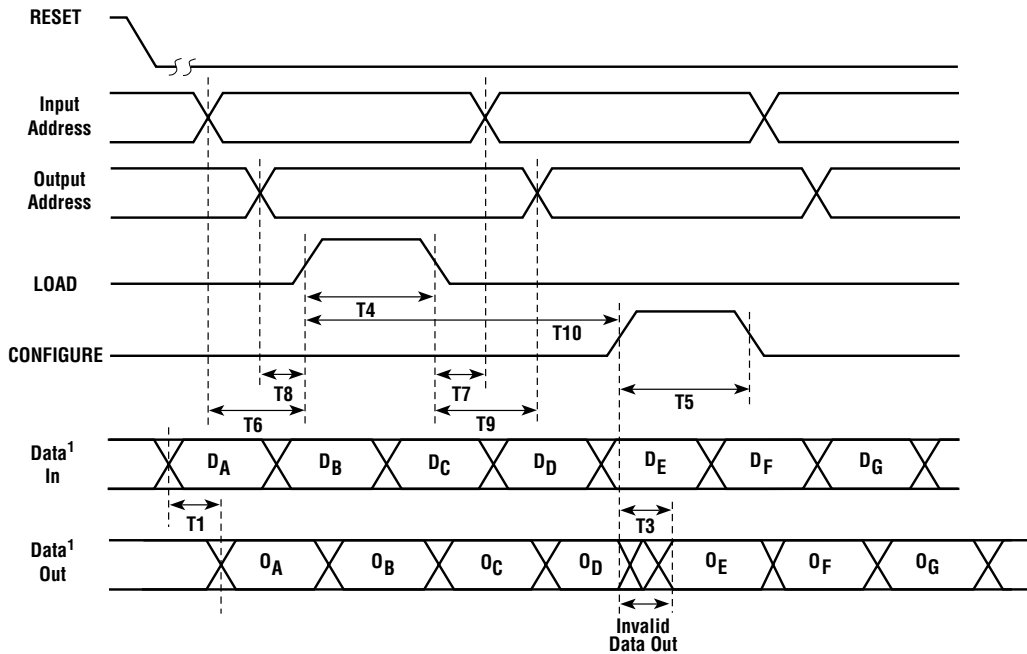
Notes: 1. Test conditions unless otherwise indicated: V<sub>TT</sub> = –2.0 V, R<sub>LOAD</sub> = 50 Ω to V<sub>TT</sub>.  
 2. Input level is selected by the CNTRL\_LVL input. Tying CNTRL\_LVL to GND selects TTL levels, leaving CNTRL\_LVL OPEN selects CMOS levels.

**Table 6. AC Characteristics<sup>1</sup>** – Within recommended operating conditions, unless otherwise indicated.

Symbol	Parameter	Min	Typ	Max	Units	Notes
	Maximum Data Rate/Port			800	Mb/s	1,2
	Jitter			150	ps pk-pk	1
T <sub>1</sub>	Channel Propagation Delay			2300	ps	
T <sub>2</sub>	Channel-to-Channel Delay Skew			500	ps	
T <sub>3</sub>	CONFIG to Data Out (Oi) Delay			5	ns	
T <sub>4</sub>	LOAD Pulse Width	7			ns	
T <sub>5</sub>	CONFIG Pulse Width	7			ns	
T <sub>6</sub>	IAi to LOAD High Setup Time	0			ns	
T <sub>7</sub>	LOAD to IAi Low Hold Time	3			ns	
T <sub>8</sub>	OAi to LOAD High Setup Time	0			ns	
T <sub>9</sub>	LOAD to OAi Low Hold Time	3			ns	
T <sub>10</sub>	Load ↑ to CONFIG ↑	0			ns	
T <sub>11</sub>	RESET Pulse Width	10			ns	
T <sub>R,F</sub>	Output Rise or Fall Time		300	400	ps	3

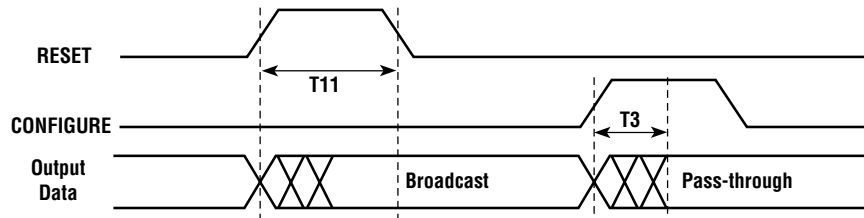
Notes: 1. Test conditions: V<sub>TT</sub> = –2.0 V, R<sub>LOAD</sub> = 50 Ω to V<sub>TT</sub>; ECL inputs: V<sub>IH</sub> = –1.1 V; V<sub>IL</sub> = –1.5 V; CMOS inputs: V<sub>IH</sub> = 3.5 V, V<sub>IL</sub> = 1.5 V; ECL outputs: V<sub>OH</sub> ≥ –1.0 V, V<sub>OL</sub> ≤ –1.6 V; ECL inputs rise and fall times ≤ 1 ns; CMOS inputs rise and fall times ≤ 20 ns. A bit error rate of 1E – 13 BER or better for 2<sup>23</sup> – 1 PRBS pattern, jitter and rise/fall times are guaranteed through characterization.  
 2. 800 Mb/s Non-Return-Zero (NRZ) data equivalent to 400 MHz clock signal.  
 3. Rise and fall times are measured at the 20% and 80% points of the transition from V<sub>OL</sub> max to V<sub>OL</sub> min.

Figure 3. Timing Diagram – Switch Configuration



Notes: 1. No data loss on unchanged paths.

Figure 4. Timing Diagram – Reset



Notes: 1. LOAD input must remain LOW to insure correct programming of the switch.  
2. "Broadcast" is defined as data input 0 to all data outputs (0..31).  
3. "Pass-through" is defined as data input 0 to data output 0, data input 1 to data output 1, etc.

## Typical Performance Data

Figure 5. Jitter – Single Channel

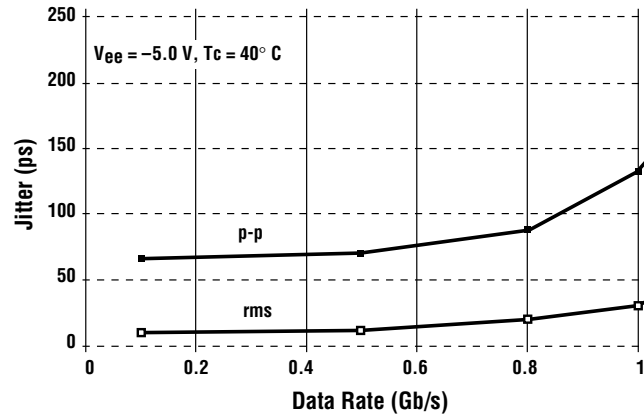
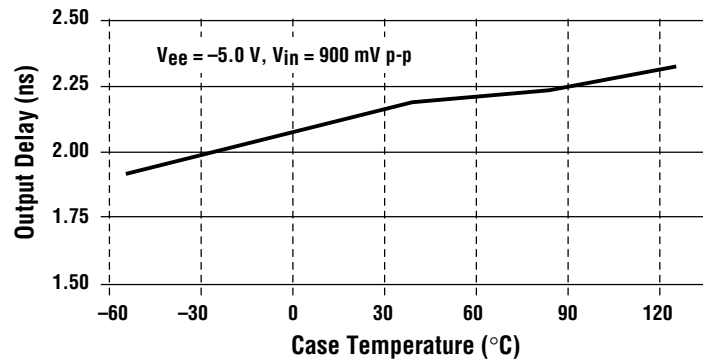


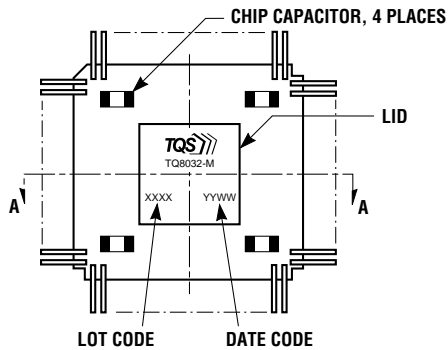
Figure 6. Output Delay



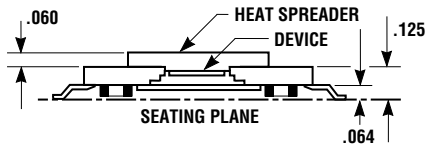
## TQ8032

**Figure 7. Mechanical Dimensions**

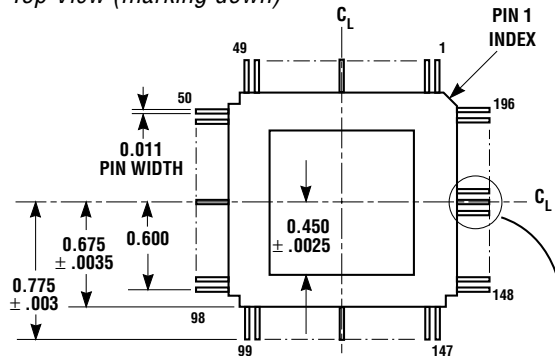
*Bottom View (marking up)*



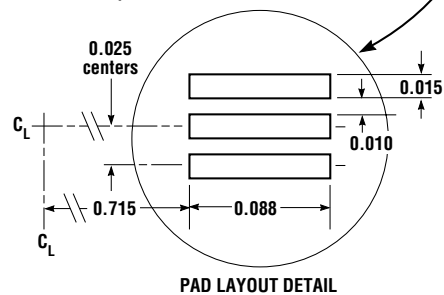
*Section A-A*



*Top View (marking down)*



1. Part is symmetrical about the center axes.
2. Centerline bisects center pin in both directions.
3. See pad detail below.



## Ordering Information

**TQ8032-M**

*800 Mb/s 32x32 ECL Crosspoint Switch*

## Additional Information

For latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

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