

The TQ8105/TQ8106 are SONET/SDH transceivers that integrate multiplexing, demultiplexing, SONET/SDH framing, clock-synthesis PLL, and enhanced line and clock diagnostic functions into a single monolithic device. The TQ8106 is a pin-compatible upgrade of the TQ8105 that includes a Clock and Data Recovery (CDR) function. The TQ8105 and TQ8106 allow maximum flexibility in the selection of internal/external Clock and Data Recovery, Opto-Electronic (O/E) Module, and Reference Clock Sources.

On-chip PLLs use external RC-based loop filters to allow custom tailoring of loop response and support the wide range of reference clock frequencies found in SONET/SDH/ATM systems. For transmit clock synthesis or for CDR, the PLLs exceed ANSI, Bellcore, and ITU jitter specifications for systems when combined with industry-typical O/E devices such as Sumitomo, AT&T, HP, and AMP. The TQ8105/TQ8106 PLLs provide byte clocks and constant-rate 38.88 MHz and 51.84 MHz, synthesized clock outputs, providing clocking for UTOPIA and other system busses. Transmit data may also be clocked into the devices with respect to the reference clock.

Operating from a single +5V supply, the TQ8105/TQ8106 provides fully compliant functionality and performance, utilizing direct-connected PECL levels (differential or single-ended) for high-speed I/O. As compared to AC-coupled schemes, the direct-coupled connections reduce jitter and switching-level offsets due to data patterns. The TQ8105/TQ8106 can also provide direct connection to high-speed I/O utilizing ECL levels with a -5V supply. Low-speed bus, control, and clock I/O utilize TTL levels. (An ECL/PECL reference clock input is also provided; at 155.52 MHz the input should be only PECL/ECL.) Output TTL pins can be tristated and may also be configured for V_{OH} with a 3.3V supply connection.

TQ8105/8106

PRELIMINARY DATA SHEET

SONET/SDH Transceivers

Features

- Single-chip, byte-wide Mux, Demux, Framer, and Tx clock-synthesis PLL with enhanced diagnostics
- TQ8106 includes monolithic Clock and Data Recovery
- SONET/SDH/ATM compliant for STS-12/STM-4 (622 Mb/s) or STS-3/STM-1 (155 Mb/s) rates
- 155.52, 77.76, 51.84, 38.88, or 19.44 MHz reference clock inputs with TTL, PECL, or ECL level
- 38.88 MHz and 51.84 MHz clock outputs for UTOPIA as well as byte clock rate (77.76 or 19.44 MHz)
- External RC-based loop filters
- Integrated loopbacks with enhanced line and reference clock diagnostics
- Direct-coupled standard, PECL, high-speed I/O with ECL option
- Clean TTL interface to PMC-Sierra devices
- 100-pin 14x14 mm JEDEC plastic package
- +5V-only supply for PECL I/O (-5.2V required for ECL I/O option)
- -40 to +125°C case operating temperature

PRELIMINARY DATA SHEET

The TQ8105/TQ8106 provides comprehensive, integrated, loopback functionality and enhanced line and reference clock diagnostics required of SONET/SDH systems, minimizing additional external circuitry.

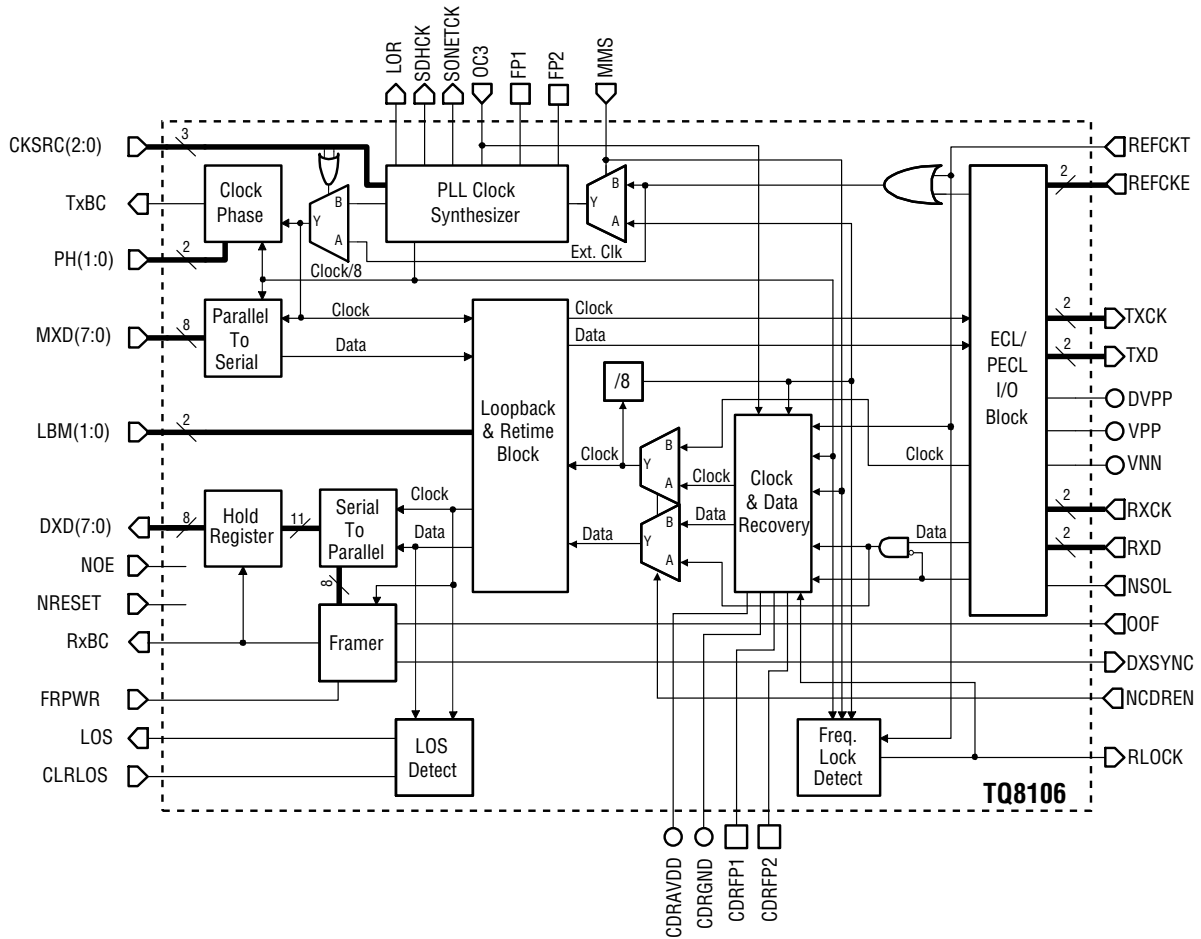
- Loss of Reference clock detector (LOR) output to indicate that the PLL Reference Clock is not toggling
- Lock Indicator (RLOCK), which permits monitoring of the receiver clock frequency, flagging when the frequency drifts beyond approximately 500 ppm
- Loss of Signal (LOS) detector output to indicate that the incoming data stream has no data transitions in 128-bit periods
- ECL/PECL input (NSOL) to allow LOS from an O/E module to force the data stream to all zeroes, eliminating the need for external glue logic.

The block diagram illustrates the internal architecture of the TQ8105 SoC. Key components include:

- PLL Clock Synthesizer:** Receives external clock inputs (LOR, SDHCK, SONET/CK, OC3, FP1, FP2, MMS) and generates internal clock signals (Clock, Clock/8, Ext. Clk).
- Loop Back & Retime Block:** Manages clock distribution and data flow between the PLL and other blocks.
- Serial to Parallel / Parallel to Serial:** Interfaces for data conversion.
- Hold Register:** Buffers data from the Serial to Parallel block.
- Framer:** Manages data framing and clock signals.
- LOS Detect:** Line of Signal detection.
- Freq. Lock Detect:** Frequency lock detection.
- ECL/PECL I/O Block:** Manages high-speed I/O signals.

Pin connections are shown on the left and right sides of the diagram, with signal names and bit widths (e.g., CKSRC(2:0), TxB, PH(1:0), MXD(7:0), LBM(1:0), DXD(7:0), NOE, NRESET, RxB, FRPWR, LOS, CLRLOS, REFCKT, REFCKE, TXCK, TXD, DVPP, VPP, VNN, RXCK, RXD, NSOL, OOF, DXSYNC, RLOCK).

Figure 2. TQ8106 Block Diagram



TQ8105/TQ8106

PRELIMINARY DATA SHEET

Figure 3. 100-Pin Enhanced Plastic 14x14 mm Package Pinout

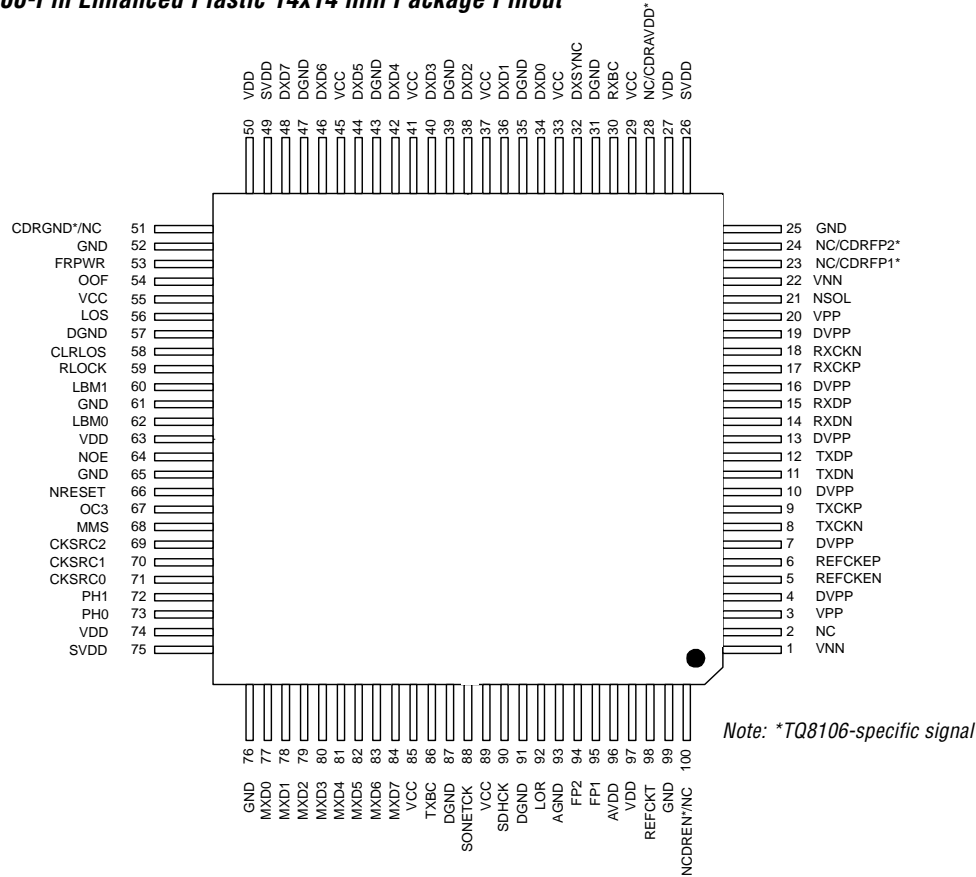


Table 1. Signal Descriptions (continues on next page)

Pin	Signal	Function	Description
1	VNN	-5.2V/Ground	ECL/PECL section power
2	NC	No Connect	Do not connect
3	VPP	Ground/+5V	ECL/PECL Positive Supply (see Table 6B)
4	DVPP	Ground/+5V	ECL/PECL Driver Return (see Table 6B)
5	REFCKEN	ECL/PECL Input	Tx Ref. Clock or Bypass Clock, Complement
6	REFCKEP	ECL/PECL Input	Tx Ref. Clock or Bypass Clock, True
7	DVPP	Ground/+5V	ECL/PECL Driver Return (see Table 6B)
8	TXCKN	ECL/PECL Out	Transmit Clock, Complement
9	TXCKP	ECL/PECL Out	Transmit Clock, True
10	DVPP	Ground/+5V	ECL/PECL Driver Return (see Table 6B)
11	TXDN	ECL/PECL Out	Transmit Data, Complement
12	TXDP	ECL/PECL Out	Transmit Data, True
13	DVPP	Ground/+5V	ECL/PECL Driver Return (see Table 6B)
14	RXDN	ECL/PECL Input	Receive Data, Complement
15	RXDP	ECL/PECL Input	Receive Data, True

Note: *TQ8106-specific signal

Table 1. Signal Descriptions (continued)

Pin	Signal	Function	Description
16	DVPP	Ground/+5V	ECL/PECL Driver Return (see Table 6B)
17	RXCKP	ECL/PECL Input	Receive Clock, True (Ignored when CDR used)
18	RXCKN	ECL/PECL Input	Receive Clock, Complement (Ignored when CDR used)
19	DVPP	Ground/+5V	ECL/PECL Driver Return (see Table 6B)
20	VPP	Ground/+5V	ECL/PECL Positive Supply (see Table 6B)
21	NSOL	ECL/PECL Input	Loss of Signal — zeroes serial data in when low; RXBC=TXCK/8
22	VNN	–5.2V/Ground	ECL/PECL section power (see Table 6B)
23	NC/CDRFP1*	Analog Output	CDR Loop Filter Pin 1 — Charge Pump Out (ignored by TQ8105)
24	NC/CDRFP2*	Analog Input	CDR Loop Filter Pin 2 — VCO Tune (ignored by TQ8105)
25	GND	GND	Core Ground
26	SVDD	+5V	Output Driver Internal Positive Supply
27	VDD	+5V	Core Positive Supply
28	CDRAVDD*	Analog +5V	TQ8106 CDR Analog +5V Supply (not connected if CDR not used; ignored by TQ8105)
29	VCC	+5V/+3.3V	TTL Driver Positive Supply
30	RxBC	Tristate TTL Out	Demultiplexer Byte Clock
31	DGND	GND	TTL Driver Ground
32	DXSYNC	Tristate TTL Out	Frame Synchronization Signal
33	VCC	+5V/+3.3V	TTL Driver Positive Supply
34	DXD0	Tristate TTL Out	Demultiplexer Data Bit 0 (LSB)
35	DGND	GND	TTL Driver Ground
36	DXD1	Tristate TTL Out	Demultiplexer Data Bit 1
37	VCC	+5V/+3.3V	TTL Driver Positive Supply
38	DXD2	Tristate TTL Out	Demultiplexer Data Bit 2
39	DGND	GND	TTL Driver Ground
40	DXD3	Tristate TTL Out	Demultiplexer Data Bit 3
41	VCC	+5V/+3.3V	TTL Driver Positive Supply
42	DXD4	Tristate TTL Out	Demultiplexer Data Bit 4
43	DGND	GND	TTL Driver Ground
44	DXD5	Tristate TTL Out	Demultiplexer Data Bit 5
45	VCC	+5V/+3.3V	TTL Driver Positive Supply
46	DXD6	Tristate TTL Out	Demultiplexer Data Bit 6
47	DGND	GND	TTL Driver Ground
48	DXD7	Tristate TTL Out	Demultiplexer Data Bit 7 (MSB)
49	SVDD	+5V	Output Driver Internal Positive Supply
50	VDD	+5V	Core Positive Supply
51	NC/CDRGND*	GND	GND for TQ8106 to powerup CDR (ignored by TQ8105)
52	GND	GND	Core Ground
53	FRPWR	TTL Input	Framer Power Control (power on when high)
54	OOF	TTL Input	Out-of-Frame: Initiates Frame Search/Bit Alignment
55	VCC	+5V/+3.3V	TTL Driver Positive Supply
56	LOS	Tristate TTL Output	Loss of Signal (high when > 128 bit periods without transitions)
57	DGND	GND	TTL Driver Ground

Note: *TQ8106-specific signal

TQ8105/TQ8106**PRELIMINARY DATA SHEET****Table 1. Signal Descriptions** (continued)

Pin	Signal	Function	Description
58	CLRLOS	TTL Input	Active-high Clear LOS output
59	RLOCK	Tristate TTL Output	Receive Clock meets lock criteria when high
60	LBM1	TTL Input	Loopback Mode Control (see Table 3)
61	GND	GND	Core Ground
62	LBM0	TTL Input	Loopback Mode Control (see Table 3)
63	VDD	+5V	Core Positive Supply
64	NOE	TTL Input	TTL tristate control (active low to enable)
65	GND	GND	Core Ground
66	NRESET	TTL Input	Global Reset (active low)
67	OC3	TTL Input	OC3/OC12 Mode Select
68	MMS	TTL Input	Master/Slave Mode Control
69	CKSRC2	TTL Input	Clock Source Select (see Table 3)
70	CKSRC1	TTL Input	Clock Source Select (see Table 3)
71	CKSRC0	TTL Input	Clock Source Select (see Table 3)
72	PH1	TTL Input	TxBC Phase Select (see Table 3)
73	PH0	TTL Input	TxBC Phase Select (see Table 3)
74	VDD	+5V	Core Positive Supply
75	SVDD	+5V	Output Driver Internal Positive Supply
76	GND	GND	Core Ground
77	MXD0	TTL Input	Multiplexer Data Bit 0 (LSB)
78	MXD1	TTL Input	Multiplexer Data Bit 1
79	MXD2	TTL Input	Multiplexer Data Bit 2
80	MXD3	TTL Input	Multiplexer Data Bit 3
81	MXD4	TTL Input	Multiplexer Data Bit 4
82	MXD5	TTL Input	Multiplexer Data Bit 5
83	MXD6	TTL Input	Multiplexer Data Bit 6
84	MXD7	TTL Input	Multiplexer Data Bit 7 (MSB)
85	VCC	+5V/+3.3V	TTL Driver Positive Supply
86	TxBC	Tristate TTL Out	Transmit Byte Clock
87	DGND	GND	TTL Driver Ground
88	SONETCK	Tristate TTL Out	51.84 MHz Clock Output
89	VCC	+5V/+3.3V	TTL Driver Positive Supply
90	SDHCK	Tristate TTL Out	38.88 MHz Clock Output
91	DGND	GND	TTL Driver Ground
92	LOR	Tristate TTL Out	Indicates Reference Clock is Absent
93	AGND	Analog Ground	VCO Analog Ground
94	FP2	Analog Output	Transmit PLL Loop Filter, Charge Pump Out
95	FP1	Analog Input	Transmit PLL Loop Filter, VCO Tune
96	AVDD	Analog +5V	VCO & Filter Analog VDD Supply
97	VDD	+5V	Core Positive Supply
98	REFCKT	TTL Input	Tx Reference Clock or Bypass Clock
99	GND	GND	Core Ground
100	NC/NCDREN*	TTL Input	Internal Pull-up, Low = CDR receiver clock; Float = Pin 17/18 Rx Clk (ignored by TQ8105)

Note: *TQ8106-specific signal

Function Description

PLL

The TQ8105 & TQ8106 incorporate high-stability, low-jitter Phase Locked Loops (PLLs) running at 2488.32 MHz. The PLLs use external surface mounted loop filters consisting of an RC network as shown in the diagrams that accompany the values shown in Table 2. Analog design principles should be applied to the loop filter portions of the circuit to ensure optimal jitter generation performance. To reduce cross-coupling of clocks, both CDR clocks and analog pins should be isolated from the transmit PLL clock and analog pins. An analog ground plane under the two capacitors and the resistor, along with guards around the filter pins is excellent practice, as is a well-filtered analog supply (AVDD) and a clean analog ground (AGND). The loop filter values specified in this preliminary data sheet may change.

Reference clock sourcing can be through a variety of mechanisms. As shown in Table 3, the MMS pin determines whether the device operates in Master mode (where the PLL reference comes in on either a TTL or PECL/ECL pin), or a Slave mode (where the PLL reference is derived from the DEMUX high-speed line clock input). If the external reference clock pins are used, note that they are logical ORs and that the unused pin should be tied to (a) GND for unused REFCKT, or (b) REFCKEN should be tied to VPP for TTL reference operation. The reference clock frequency can be selected from any number of values, as indicated in Table 3. Note that the PLL may be bypassed, allowing use of an external clock reference.

Internal dividers determine the operating line rate, as shown in Table 3. The device is capable of operating at STM1/STS-3 or STM4/STS-12 rates. The transmit PLL provides high performance and compliance with ITU/Bellcore requirements found in the first-generation TQ8101. The TQ8106 receiver's CDR can be disabled for backwards pin-compatibility with the TQ8105. For circuits not requiring the TQ8106's CDR, the CDR is disabled by floating NCDREN (pin 100). Further, the CDR

section of the TQ8106 can be powered down by disconnecting the CDRGND and CDRAVDD pins, thereby reducing power consumption. If the TQ8106 CDR is not used, the CDR filter pins may be left unconnected.

The transmit PLL also provides constant-rate 38.88 MHz and 51.84 MHz TTL outputs which may be tristated. The 38.88 MHz & 51.84 MHz output may also be achieved by using high-speed receiver timing in Clock Source Mode 011 (see Table 3).

Framer

The TQ8105 and TQ8106 provide a clean interface to devices from PMC-Sierra and others. The Out-of-Frame (OOF) input is a state (level)-initiated event, rather than the edge-triggered event found on TriQuint's first-generation TQ8101 transceiver. When OOF is high, the TQ8105/TQ8106 initiates a frame search for a serial bit pattern of twelve A1s (three A1s in OC3 mode) followed by three A2s. If a match occurs, the device realigns byte boundaries and issues a logic high on the DXSYNC pin during the third A2. In the absence of OOF, the device will not realign byte boundaries, but will report any bit-level matching of twelve A1s (three A1s in OC3 mode) followed by three A2s as a DXSYNC pulse.

Framer circuit power may be switched off by a TTL low on the FRPWR pin, saving approximately 0.25W. No further DXSYNC pulses will be issued, though bit alignment is preserved in the demux. Note that the OOF and FRPWR pins may be tied together, powering the framer only when bit realignment is required (this is not recommended practice, however, due to the inrush currents that may result).

Loopbacks

As part of the TQ8105 and TQ8106 on-chip diagnostics, four loopback modes are supported. These are selected by the dedicated pins LBM0 and LBM1, as shown in Table 3. The loopback modes are shown in Figure 5.

Functional Description (continued)**Enhanced Diagnostics**

The TQ8105 and TQ8106 incorporate on-chip clock diagnostics, allowing fast, efficient fault detection and isolation at the systems level.

The LOR (Loss Of Reference) output goes high when the reference clock is absent. Note that this signal is not latched and is only high when the reference clock is missing. A reference clock is required for the TQ8106 CDR to function correctly.

The NSOL (Loss-of-signal input, active low, PECL/ECL level) input allows the receiver to force zeroes onto the demux outputs. A TTL-level signal may also be used for NSOL if the resistor network, shown in the applications section of this data sheet, is used. NSOL is useful when a Loss Of Signal occurs on the receive optics, and a quieting of invalid data is desired. The receiver is clocked from the transmit clock when NSOL is active, and the output RXBC clock is obtained from the transmit portion of the TQ8105/TQ8106. This ensures compatibility with devices, such as the PMC-Sierra S/UNI-622 and STTX components, which may contain dynamic registers that lose contents if clocks are removed. NSOL forces the CDR to lock on REFCLK, except when in slave mode.

The LOS (Loss Of Signal) output goes high whenever 128-bit periods occur without transitions on the data input to the demux. CLRLOS forces LOS low.

The RLOCK (Receiver LOCK) output goes low whenever the signal on RXCK or the recovered clock drifts more than 500 ppm from the reference frequency. This output returns high whenever the frequency accuracy is within 100 ppm.

Demux

The TQ8105/TQ8106 demultiplexer converts an NRZ PECL/ECL data input, at either 155 Mb/s or 622 Mb/s, and its corresponding PECL/ECL clock into a byte-parallel

78 MHz or 19 MHz tristatable TTL data bus. The timing is shown in Figures 6 through 8. See the previous “Framer” description for bit alignment details. The TQ8106 can recover both clock and data from a NRZ data stream, whereas the TQ8105 requires NRZ data and a recovered clock.

Mux

The TQ8105/TQ8106 multiplexer converts a 78 MHz or 19 MHz byte-wide bus to a serial NRZ PECL/ECL data stream. The bytes are clocked into the device with the TXBC byte clock output. The timing is shown in Figures 6 through 8. Note that the TXBC output can be adjusted in 90-degree phase increments to accommodate variations in interface requirements. See Table 3 for settings on the PH0 and PH1 pins controlling this function. Data may also be clocked into the TQ8105/TQ8106 by a 77 MHz reference, oscillator-clock source, provided the data is within the timing limits shown in the timing diagram labelled “Reference Clock Based Transmit Timing.” The TQ8105 and TQ8106 do not require the transmit latch found on earlier TQ8101 reference designs and are backwards compatible with designs that have the latch incorporated.

High-Speed I/O and TTL Interfaces

The TQ8105/06P will operate with either PECL or ECL operation on the high-speed I/O. With a single +5V supply, the part interfaces directly with TTL and PECL (Positive Emitter Coupled Logic). By providing an additional -5.2V supply, the device's high-speed I/O becomes ECL, instead of PECL. The TQ8105/06S is designed only for PECL high-speed I/O operation with a single +5V supply. The power supply connections for PECL and ECL are shown in Table 6B.

The TTL outputs (Vcc) may be connected to either +5V or +3.3V supplies. True TTL may be obtained with the +5V connection; clamped operation, when connected to +3.3V, ensures that maximum Voh levels do not exceed +3.3V.

TQ8105/TQ8106 Design Notes

These design notes are provided to assist the circuit designer in achieving the highest possible performance while reducing design time. Unless noted otherwise, references to the TQ8105 apply equally to the TQ8106.

Interfacing to PMC-Sierra Devices

The transmit timing of the TQ8105 is such that the PMC-Sierra byte outputs (POUT(0:7)) may be directly connected to the TQ8105 mux inputs (MXD(0:7)). The TQ8105 uses an Out-Of-Frame (OOF) input as a signal to reframe while high, allowing direct connection of the PM5355's OOF output to the TQ8105 OOF input. The following summarizes connectivity between the devices.

PM5355	TQ8105/TQ8106
POUT(0:7)	MXD(0:7)
PIN(0:7)	DXD(0:7)
OOF	OOF
PICLK	RXBC
FPIN	DXSYNC
TCLK	TXBC
POP(0:5)	Any TQ8105 modes to be programmable
PIP(0:3)	Any TQ8105 diag outputs to be readable

Reference Design

A reference design (see Figure 4) and evaluation board are available from TriQuint. They incorporate a 1x9 or 2x9 fiber optic transceiver (with the option of clock recovery), the PM5355 PMC Sierra framer device, and a TQ8105 or TQ8106.

Thermal Considerations

Figure 9 shows the region where the use of a heatsink is not required. For example, the TQ8105 does not require a heatsink for ambient temperatures up to 55°C in still air. An airflow of 100 LFPM raised this temperature to approximately 75°C, eliminating heatsink requirements.

In applications requiring a heatsink, a standard pin-fin heat-sink is appropriate. To attach the sink, use spring

clips soldered to the board to cross and hold the heatsink. The clip holes in the board are at the corners of a 1.275" x 1.5" rectangle. Another alternative is the circular heatsink, #2288B from Thermalloy attached with their Thermattach #19686-3.

Power Supplies

Good decoupling practices should be observed, with a 0.1 uF decoupling capacitor at each supply pin, ideally on the component side of the board. Keep the analog supplies (Vdd and AVdd) pristine. Proper design will isolate the supply groups using point grounding to tie supplies together (*all* grounds at a single point having multiple vias).

For the analog supply, flood copper under the loop filter on the component side of the board, tying the flood to the analog ground pin, with the point ground away from the filter and analog pin, so that any switching currents are kept away from these areas. If any switching, power-supply frequencies below 500 kHz are used in the system, use a supply filter on the analog supply pin. These practices help minimize the generation of jitter.

High-Speed Connections

Connections to E/O modules (and clock reference, if used) are direct-coupled PECL and need to be terminated with decoupled 50 ohms to 3V at the receiving end of the 50 ohm transmission line. Ensure that each 50 ohm resistor (or Thevenin equivalent) has its own decoupling capacitor. Place the resistor at the end of a 50 ohm transmission line (use a controlled impedance layer), ideally with a minimal-length stub attached to either the resistor or the receiving device.

If there is no room for the resistor, use a minimal-length stub to drop the signal at the receiving device pins, continue the 50 ohm transmission line to an area where the termination resistors can be placed, and terminate at the endpoint of that line. If in doubt, contact factory applications for assistance.

PRELIMINARY DATA SHEET

Figure 4. Reference Design Schematic

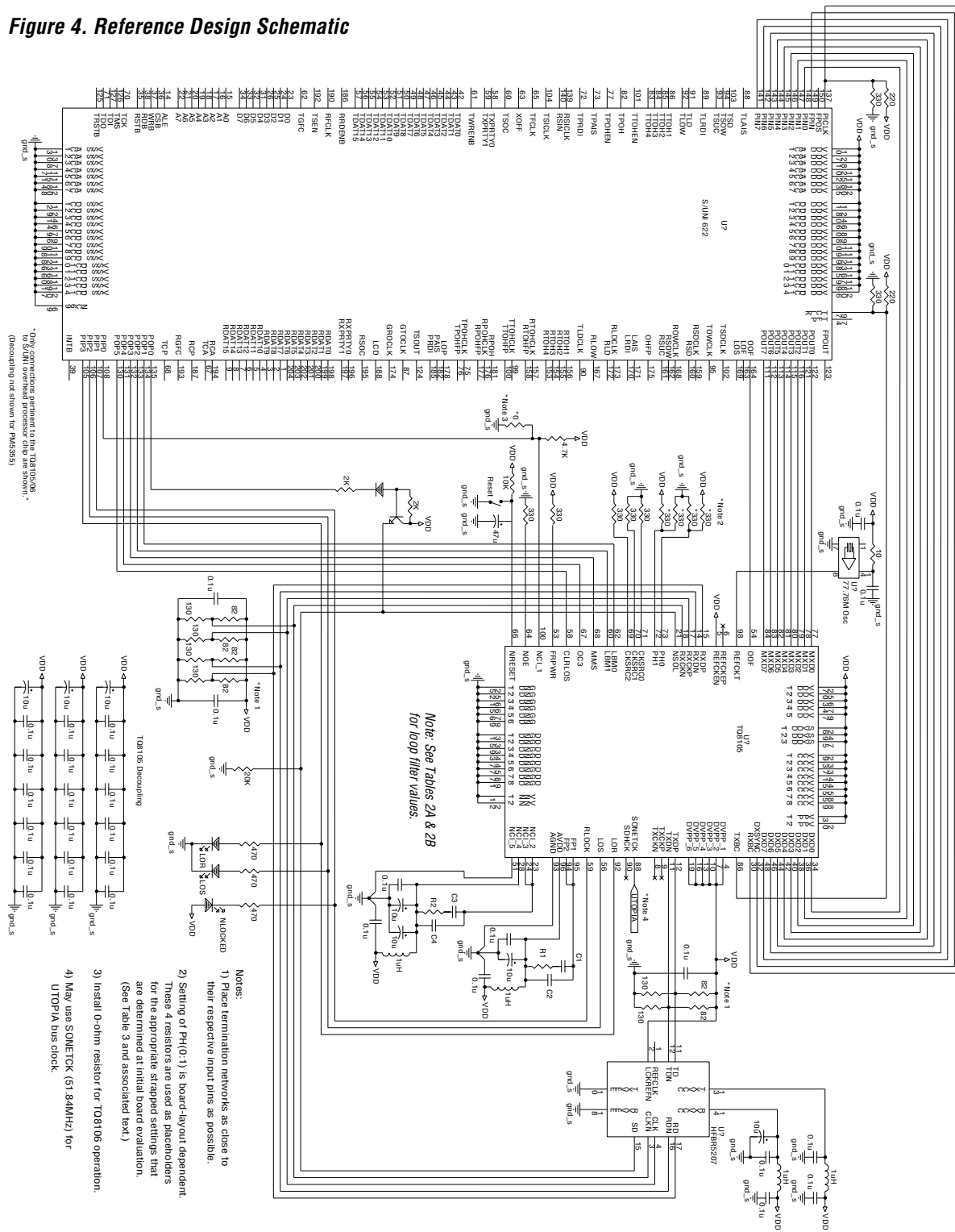


Table 2A. TQ8105/TQ8106 Recommended Transmit Loop Filter Values (Preliminary)

Reference Frequency (MHz)	Divide Ratio	Resistor Value R1 (ohms)	Capacitor Value C1 (μ F)	Capacitor Value C2 (pF)
19.44	32	1200	0.082	82
38.88	16	620	0.15	150
51.84	12	470	0.22	220
77.76	8	300	0.33	330
155.52*	4	300	0.33	330

Note: *Internal divide by two on Reference

Table 2B. TQ8106 Recommended CDR Loop Filter Values (Preliminary)

Incoming NRZ Data Rate (Mbs)	Resistor Value R2 (ohms)	Capacitor Value C3 (μ F)	Capacitor Value C4 (pF)
155.52	470	1.0	39
622.08	680	4.7	39

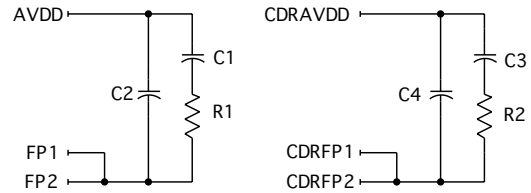
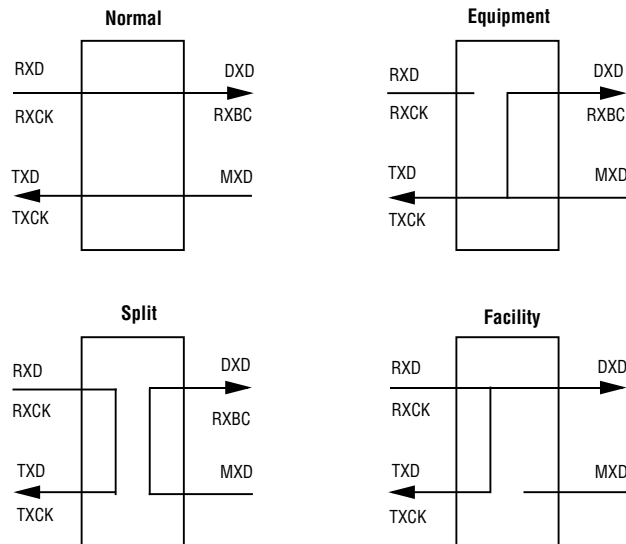


Figure 5. Loopback Modes



TQ8105/TQ8106

PRELIMINARY DATA SHEET

Table 3. Mode Selection

Signals	Mode
LBM(1:0)	Loopback: 00 = Normal, 01 = Equipment, 10 = Facility, 11 = Split
PH(1:0)	00 = 0 degrees delay, 01 = 90 degrees delay, 10 = 180 degrees delay, 11 = 270 degrees delay
MMS	1 = Master (use REFCKT/E as reference), 0 = Slave (use receive clock as reference)
CKSRC(2:0)	Clock Source: 000 = PLL bypass 001 = 51.84 MHz PLL reference, SONETCK & SDHCK tristate 010 = 155.52 MHz PLL reference 011 = 51.84 MHz PLL reference, SONETCK=8, SDHCK derived from receiver timing 100 = 77.76 MHz PLL reference 101 = 51.84 MHz PLL reference 110 = 38.88 MHz PLL reference 111 = 19.44 MHz PLL reference
OOF	1 = Initiate frame search, 0 = Do not permit reframing (see FRPWR pin in Table 1)
NSOL	1 = Pass receive data, 0 = Force receive data to 0
OC3	1 = Operate at STM1/STS-3 (or PLL bypass divided by 4), 0 = Operate at STM4/STS-12/PLL bypass
NRESET	1 = Normal operation, 0 = Reset internal counters
NCDREN	1 = TQ8105/CDR Off mode, 0 = Enable CDR (TQ8106 only)

Table 4. Absolute Maximum Ratings

Parameter	Symbol	Level	Minimum	Maximum	Unit
Positive supply	$V_{CC}, V_{PP}, V_{DD}, AV_{DD}$	GND	7	V	
Negative supply ($V_{PP} = 0$ V)	V_{NN}		-7	GND	V
Output voltage	V_O	ECL/PECL	$V_{NN}-0.5$	$V_{PP}+0.5$	V
Output current	I_O	ECL/PECL	—	40	mA
Input voltage	V_I	ECL/PECL	$V_{NN}-0.5$	$V_{PP}+0.5$	V
Input current	I_I	ECL/PECL	-1	1	mA
Output voltage	V_O	TTL	-0.5	$V_{CC}+0.5$	V
Output current	I_O	TTL	—	100	mA
Input voltage	V_I	TTL	-0.5	$V_{CC}+0.5$	V
Input current	I_I	TTL	-1	1	mA
Biased junction temperature	T_J	—	-55	+150	° C
Storage temperature	T_S	—	-65	+150	° C

Table 5. Power Consumption

Symbol	Function	Minimum	Typical	Maximum	Unit
I _{DD}	+5V supply	—	0.323	TBD	I
I _{CC}	+5V / +3V supply	—	0.016	TBD	I
I _{PP}	+5V / 0V supply	—	0.055	TBD	I
I _{ADD}	+5V supply	—	0.018	TBD	I
P _{DF}	Power dissipation, Framer on, TQ8106 CDR off	—	1.9	2.3	W
P _D	Power dissipation, Framer off, TQ8106 CDR off	—	1.7	2.1	W
P	Power dissipation, Framer on, TQ8106 CDR on			2.75	W

Table 6A. Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Positive supply	V _{PP}	4.75	5.0	5.25	V
Output driver positive supply	V _{CC}	3.0		5.25	V
Negative supply (ECL mode only)	V _{NN}	–5.5	–5.2	–4.75	V
Operating case temperature (see Figure 9)		–40		125	°C

Table 6B. Power Supply Connections

Pin	+5V TTL/PECL I/O	+3.3V TTL/PECL I/O	+5V TTL/ECL I/O	+3.3V TTL/ECL I/O
VDD	+5V	+5V	+5V	+5V
SVDD	+5V	+5V	+5V	+5V
VCC	+5V	+3.3V	+5V	+3.3V
AVDD	Filtered +5V	Filtered +5V	Filtered +5V	Filtered +5V
CDRAVDD	Filtered +5V	Filtered +5V	Filtered +5V	Filtered +5V
GND	0V (ground)	0V (ground)	0V (ground)	0V (ground)
AGND	0V (ground)	0V (ground)	0V (ground)	0V (ground)
CDRGND	0V (ground)	0V (ground)	0V (ground)	0V (ground)
VPP/DVPP	+5V	+5V	0V (ground)	0V (ground)
VNN	0V (ground)	0V (ground)	–5.2V	–5.2V

TQ8105/TQ8106

PRELIMINARY DATA SHEET

Table 7. DC Characteristics—ECL/PECL I/O

(Specifications apply over recommended operating ranges).

Parameter	Condition	Symbol	Minimum	Nominal	Maximum	Unit
Internal ECL reference	Single-ended inputs	V_{REF}	—	$0.26 V_{NN} + 0.74 V_{PP}$		mV
Common mode voltage	Differential inputs	V_{COM}	$V_{PP} - 1500$	—	$V_{PP} - 1100$	mV
Differential voltage	Differential inputs	V_{DIFF}	200	—	1200	mV
Input HIGH voltage	$V_{REF} = 1300$ mV	V_{IH}	$V_{PP} - 1050$	—	$V_{PP} - 400$	mV
Input LOW voltage		V_{IL}	V_{TT}	—	$V_{PP} - 1550$	mV
Output HIGH voltage	$R_{LOAD} = 50$ ohms to $V_{TT} = V_{PP} - 2.0V$	V_{OH}	$V_{PP} - 1000$		$V_{PP} - 600$	mV
Output LOW voltage	$R_{LOAD} = 50$ ohms to $V_{TT} = V_{PP} - 2.0V$	V_{OL}	V_{TT}	—	$V_{PP} - 1600$	mV
Input HIGH current	$V_{IH(MAX)}$	I_{IH}	—	+130	335	uA
Input LOW current	$V_{IL(MIN)}$	I_{IL}	-265	-130	—	uA
Output HIGH current	(Not tested; consistent with V_{OH} and V_{OL} tests)	I_{OH}	20	23	30	mA
Output LOW current	(Not tested; consistent with V_{OH} and V_{OL} tests)	I_{OL}	0	5	8	mA
Input capacitance		C_{IN}	—	—	TBD	pF
Output capacitance		C_{OUT}	—	—	TBD	pF
ESD breakdown rating	(Design objective)	V_{ESD}	Class I	—	—	

Note: $V_{TT} = V_{PP} - 2.0V$

Table 8. DC Characteristics—TTL I/O

(Specifications apply over recommended operating ranges)

Parameter	Condition	Symbol	Minimum	Nominal	Maximum	Unit
Input HIGH voltage		V_{IH}	2.0	—	V_{CC}	V
Input LOW voltage		V_{IL}	0	—	0.8	V
Input HIGH current	$V_{IH(MAX)}$	I_{IH}	—	—	200	uA
Input LOW current	$V_{IL(MIN)}$	I_{IL}	-400	-200	—	uA
Output HIGH voltage	$I_{OH} = 50$ mA	V_{OH}	2.4	—	V_{CC}	V
Output LOW voltage	$I_{OL} = -20$ mA	V_{OL}	0	—	0.4	V
Tristate current		I_{OZ}	-100	—	100	uA
Input capacitance		C_{IN}	—	—	TBD	pF
Output capacitance		C_{OUT}	—	—	TBD	pF
ESD breakdown rating	(Design objective)	V_{ESD}	Class I	—	—	

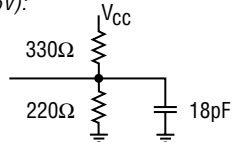
Table 9. AC Characteristics

(Specifications apply over recommended operating ranges)

Parameter	Symbol	Minimum	Nominal	Maximum	Unit
RXCK clock period	$T_{C(RXCK)}$	1.6	—	—	ns
REFCKE clock period	$T_{C(REFCKE)}$	1.6	—	—	ns
TXCK clock period	$T_{C(TXCK)}$	1.6	—	—	ns
REFCKT clock period	$T_{C(REFCKT)}$	12.8	—	—	ns
TXBC clock period	$T_{C(TXBC)}$	12.8	—	—	ns
RXBC clock period	$T_{C(RXBC)}$	12.8	—	—	ns
REFCKT/REFCKE clock duty cycle	$T_{C(REF)}$	40	—	60	%
REFCKT to TXBC skew ^{2,3,5}	$T_{SK(TXBC)}$	TBD		TBD	
SONETCK clock period	$T_{C(SONETCK)}$	—	19.29	—	ns
RXBC clock duty cycle ^{3,5}	$T_{DC(RXBC)}$	40	50	60	%
TXBC clock duty cycle ^{3,5}	$T_{DC(TXBC)}$	40	50	60	%
TXCK clock duty cycle ⁶	$T_{DC(TXCK)}$	40	50	60	%
SONETCK clock duty cycle ^{3,5}	$T_{DC(SONETCK)}$	40	50	60	%
SDHCK clock duty cycle ^{3,5}	$T_{DC(SDHCK)}$	40	50	60	%
RXCK clock duty cycle ⁶	$T_{DC(RXCK)}$	40	50	60	
High-speed rise/fall time ⁴ (> 79 MHz), Data	$T_{H(R/F)}$	—	—	500	ps
High-speed rise/fall time ⁴ (> 79 MHz), Clock	$T_{H(R/F)}$	—	—	320	ps
Low-speed rise/fall time ^{1,3,5} (< 79 MHz)	$T_{L(R/F)}$	—	—	3	ns
RXD setup time to RXCK ⁶ (see Figure 6)	$T_{S(RXD)}$	240	—	—	ps
RXD hold time to RXCK ⁶ (see Figure 6)	$T_{H(RXD)}$	20	—	—	ps
OOF rising edge before A1 changes to A2 ⁷ (see Figure 8)	$T_{(OOFH)}$	51.44	—	—	ns
DXSYNC rising edge from parallel data output change from A1 to A2 ⁷	$T_{(DSYNC)}$	—	25.72	—	ns
DXSYNC pulse width ^{3,5,7} (see Figure 8)	$T_{(DXSYNCPW)}$	11.0	—	—	ns
RXBC falling edge to valid parallel data output ³ (see Figure 7)	$T_{P(DXD)}$	0.5		1.0	ns
MXD(0:7) setup time to TXBC ^{2,3,5} (see Figure 6)	$T_{S(MXD)}$	600	—	—	ps
MXD(0:7) hold time to TXBC ^{2,3,5} (see Figure 6)	$T_{H(MXD)}$	600	—	—	ps
TXCK falling edge to TXD ⁶ (see Figure 7)	$T_{P(TXD)}$	200	—	400	ps

Notes: 1. At 0.8V/2.0V levels

2. With PH(1:0) set to 00, 18pF total loading

3. TTL outputs test load ($V_{CC} = +5V$):

4. 20%/80% levels

5. At 1.4V logic threshold level

6. Differential measurement

7. OC12 mode

Figure 6. Input Timing

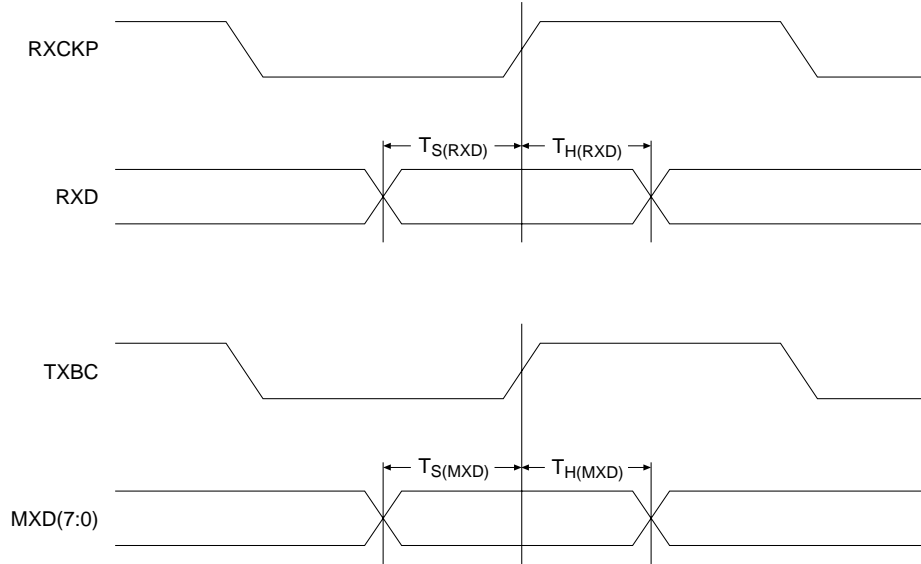


Figure 7. Output Timing

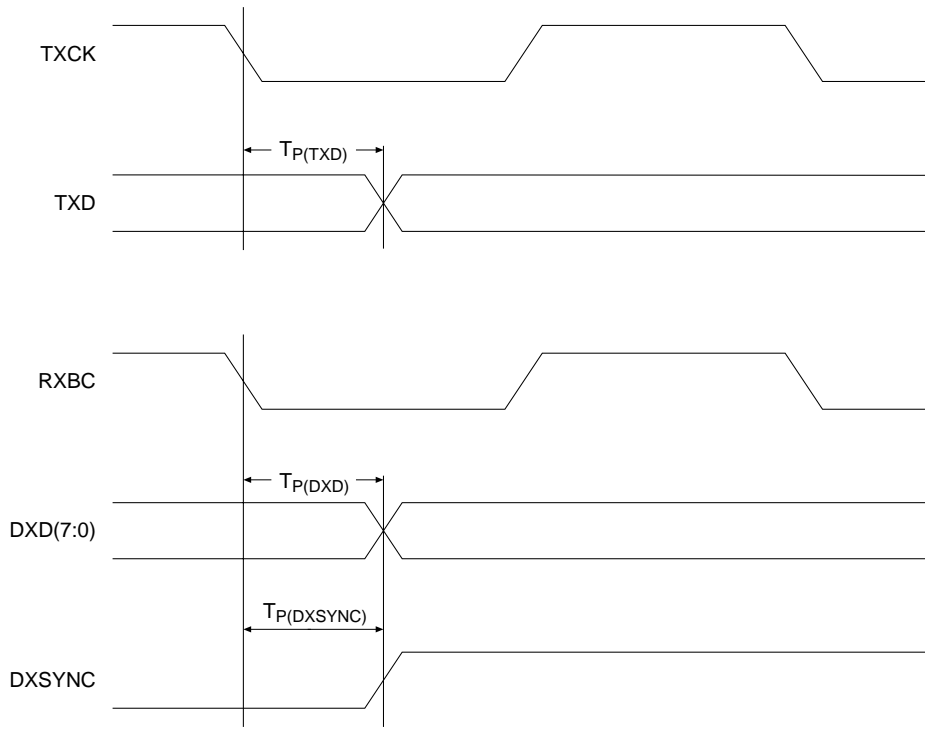


Figure 8. Demultiplexer Timing

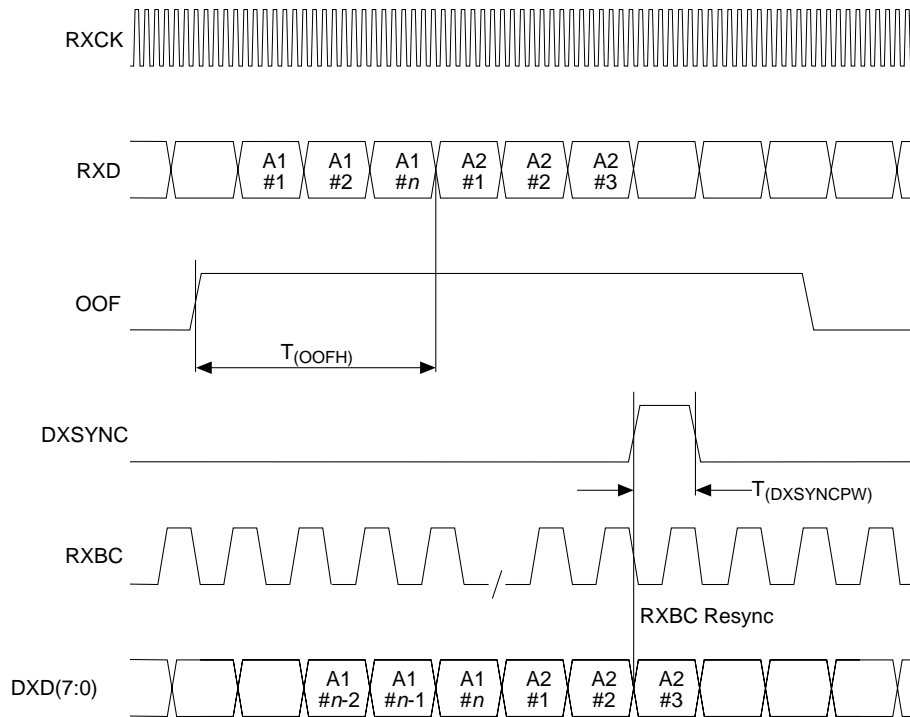
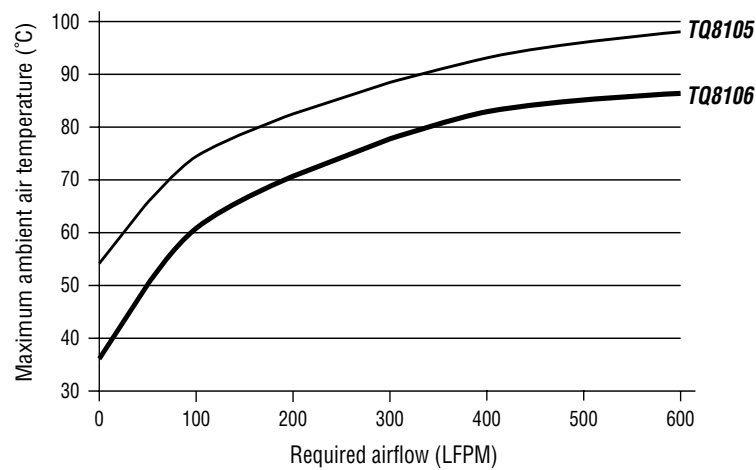


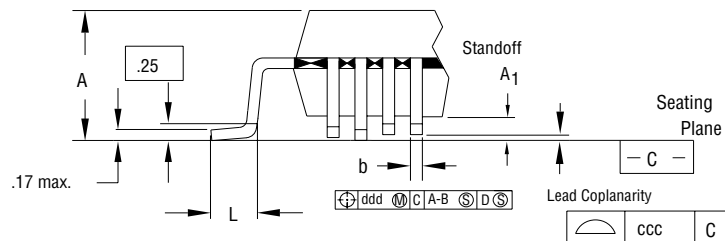
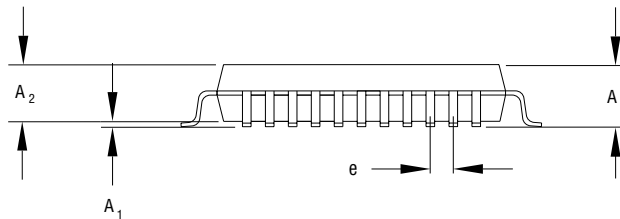
Figure 9. Required Airflow for Operation without Heatsink



PRELIMINARY DATA SHEET

<i>Package Dimension</i>	<i>Package “P”¹ Value²</i>	<i>Package “S” Value²</i>
A	2.35	1.7 max
A ₁	0.25 max	0.10
A ₂	2.00	1.40
D	17.20 ±0.25	16.00 ±0.4
D ₁	14.00	14.00
E	17.20 ±0.25	16.00 ±0.4
E ₁	14.00	14.00
L	0.88 +0.15/−0.10	0.50 ±0.20
b	0.22	0.18
e	0.50	0.50
N	100 pins	100 pins

Top view of a square microchip. The overall width is labeled D and the overall height is labeled E . The width of the central square area is labeled D_1 and the height of this central area is labeled E_1 . The chip has pins on all four sides. A circular feature is centered on the chip. Callouts include: "Exposed Heatsink $6.86 \pm .50$ dia." pointing to the circular feature, "Heatsink Intrusion .0127 max." pointing to the gap between the chip and the heatsink, and "N" pointing to the top edge of the chip. Section lines A-A, B-B, and D-D are indicated.



Ordering Information

TQ8105P	<i>SONET/SDH Transceiver, PECL/ECL I/O</i>
TQ8106P	<i>SONET/SDH Transceiver w/CDR, PECL/ECL I/O</i>
TQ8105S	<i>SONET/SDH Transceiver, PECL I/O</i>
TQ8106S	<i>SONET/SDH Transceiver w/CDR, PECL I/O</i>

Reference Designs

The following products are available for 14-day loan to qualified customers:

ATM SONET/SDH Line Interface Module (SLIM)

Supports OC12c/STM-4 (622.08 Mbps) and OC-3c/STM-1 (155.52 Mbps)

SLIM Documentation Package

- Functional Partition Drawing Set, including block, state machine, and timing diagrams
- User's Manual / Product Specification
- Schematics
- PCB Artwork (all layers)
- Programmable Logic Listings
- Component Placement Drawing

Additional Information

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