



HIGH SPEED CMOS 2 Megabit PROGRAMMABLE and ERASABLE ROM 256K X 8 BIT FLASH PEROM

FEATURES:

- 150 ns Access Time
- 5 Volt Only Reprogramming
- Sector Program Operation
 - Single Cycle Reprogram (Erase & Program)
 - 2048 Sectors (128 bytes/sector)
 - Internal Address and Data Latches for 128 Bytes
- Automatic Sector Programming Operation
 - Internal Control Timer
- Fast Program Times
 - Page Program Cycles: 10 ms Typical
 - Time to Rewrite Complete Memory: 21 s
 - Typical Byte Program Cycle Time: 80 μ s
- Software Data Protection
- Low Power Dissipation
 - 60 mA Active Current
 - 100 μ A CMOS Standby Current
- Direct Microprocessor End of Program Detection
 - Data Polling
- High Reliability CMOS Technology
 - Endurance: 10,000 Cycles
 - Data Retention: 10 years
- CMOS and TTL Compatible Inputs and Outputs
- Single 5V \pm 10% Power Supply for Read and Programming Operations
- JEDEC Approved Byte Pinout

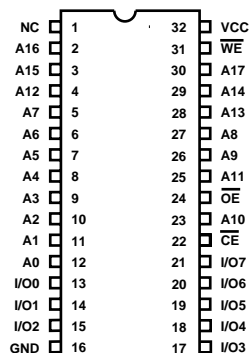
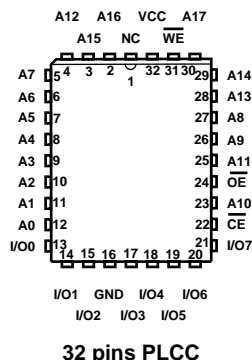
DESCRIPTION:

The Turbo IC 29C021 is a 256K x 8 Flash programmable and erasable read only memory (PEROM) fabricated with Turbo IC's proprietary, high reliability, high performance CMOS technology. Its 2048K bits of memory are organized as 256K by 8 bits. The device offers access time of 150 ns with power dissipation below 330 mW.

The 29C021 has a 128 bytes sector program operation enabling the entire memory to be programmed typically in less than 21 seconds. During a program operation, the address and a complete sector (128 bytes) of data are internally latched, freeing the address and data bus for other microprocessor operations. The programming process is automatically controlled by the device using an internal control timer. Data polling on I/O7 or a Toggle bit can be used to detect the end of a programming cycle. In addition, the 29C021 includes an user-optional software data write mode offering additional protection against unwanted (false) write.

The 29C021 does not require a separate high voltage to program the device. 5 volts is all that is required.

PIN CONFIGURATIONS:





PIN DESCRIPTION

ADDRESSES (A0 - A17)

The Addresses are used to select an 8 bits memory location during a program or read operation.

CHIP ENABLE (\overline{CE})

The Chip Enable input must be low to enable all read/program operations on the device. By setting \overline{CE} high, the device is disabled and the power consumption is extremely low with the standby current below 100 μ A.

DEVICE OPERATION

READ

The 29C021 is accessed like a static RAM. Read operations are initiated by both \overline{CE} and \overline{OE} on low and terminated by either \overline{CE} or \overline{OE} returning high. The outputs are at the high impedance state whenever \overline{CE} or \overline{OE} returns high. The two line control architecture gives designers flexibility in preventing bus contention.

PROGRAM

A program cycle is initiated when \overline{CE} and \overline{WE} are low and \overline{OE} is high. The address is latched internally on the falling edge of the \overline{CE} or \overline{WE} , whichever occurs last. The data is latched by the rising edge of \overline{CE} or \overline{WE} , whichever occurs first. Once a programming cycle has been started, the internal timer automatically generates the program sequence to the completion of the program operation.

SECTOR PROGRAM OPERATION

The device is reprogrammed on a sector basis. When a byte of data within a sector is to be changed, data for the entire sector must be loaded into the device. Any byte that is not loaded during the programming of its sector will be erased to read FFh. The programming operation of the 29C021 allows 128 bytes of data to be serially loaded into the device and then simultaneously written into memory during the internally generated program cycle. After the first byte has been loaded, successive bytes of data must be loaded until the full sector of 128 bytes is loaded. Each new byte to be written must be loaded within 300 μ s of the previously loaded byte. The sector address defined by the addresses A7 - A17 is latched by the first \overline{CE} or \overline{WE} falling edge which initiates a program cycle and they stay latched until the completion of the program cycle. Any changes in the sector addresses during the load-program cycle will not affect the initially latched sector address. Addresses A0 - A6 are used to define which bytes will be loaded within the 128 bytes sector. The bytes may be loaded in any order that is convenient to the user. The content of a loaded byte may be altered at any time during the loading cycle if the maximum allowed byte-load time (300 μ s) is not exceeded. All the 128 bytes of the page are serially loaded and are programmed in a single 10 ms program cycle.

DATA POLLING

The 29C021 features \overline{DATA} Polling to indicate the completion of a program cycle to the host system. During a program cycle, an attempted read of the last byte loaded into the page will result in the complement of the loaded byte on I/O7, i.e., loaded 0 would be read 1. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may be started. \overline{DATA} Polling may begin at any time during the programming cycle.

OUTPUT ENABLE (\overline{OE})

The Output Enable input activates the output buffers during the read operations.

WRITE ENABLE (\overline{WE})

The Write Enable input initiates the programming of data into the memory.

DATA INPUT/OUTPUT (I/O0-I/O7)

Data Input/Output pins are used to read data out of the memory or to program Data into the memory.

TOGGLE BIT

In addition to \overline{DATA} Polling the 29C021 provides another method for determining the end of a programming or erase cycle. During a program or erase operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle.

CHIP CLEAR

The content of the entire memory array of the 29C021 may be altered to HIGH by the use of the CHIP CLEAR operation. By setting \overline{CE} to low, \overline{OE} to 12 Volts, and \overline{WE} to low, the entire memory array can be cleared (written HIGH) within 20 ms. The CHIP CLEAR operation is a latch operation mode. After \overline{CE} , \overline{WE} , and \overline{OE} get the CHIP CLEAR process started, the internal chip timer takes over the CHIP CLEAR operation and \overline{CE} , \overline{OE} , or \overline{WE} becomes free to be used by the system for other purposes.

HARDWARE DATA PROTECTION

The 29C021 has three hardware features to protect the written content of the memory against inadvertent programming:

- Vcc threshold detector - If Vcc is below 3 V the program capabilities of the chip is inhibited for whatever input conditions.
- Noise protection - A \overline{WE} , \overline{OE} , or CE pulse of less than 10 ns in width is not able to initiate a program cycle.
- Write inhibit - Holding \overline{OE} at low, or \overline{CE} at high, or \overline{WE} at high inhibits the program cycle.

SOFTWARE DATA PROTECTION

The 29C021 offers a software controlled data program protection feature. The device is delivered to the user with the software data protection DISABLED, i.e., the device will go to the program operation as long as Vcc exceeds 3 V and \overline{CE} , \overline{WE} , and \overline{OE} inputs are set at program mode levels. The 29C021 can be automatically protected against an accidental write operation during power-up or power-down without any external circuitry by enabling the software data protection feature. This feature is enable after the first program cycle which includes the software algorithm. After this operation is done the program function of the device may be performed only if every program cycle is preceded by the software algorithm. The device will maintain its software protect feature for the rest of its life, unless the software algorithm for disabling the protection is implemented.



SOFTWARE ALGORITHM

The 29C021 has an internal register for the software algorithm which enables the memory to provide the user with additional features:

a) Software Data Protect Enable

A sequence of the three dummy data writes to the memory will activate internal EEPROM fuses during the first page write cycle. These EEPROM fuses will reject any write attempts of new pages of data, unless the three dummy data writes are repeated at the beginning of any page writes.

The timing for the dummy data and addresses must be the same as for a normal program operation. A violation of the three steps program protect sequence in data or address timing and content will abort the procedure and reset the device to the starting point condition.

Note: Software data protect enable procedure must be performed as part of a standard program cycle. If no additional page data is added to the three dummy data writes, the software data protect enable procedure will be aborted. The data protect state will be activated at the end of the program cycle. 128 bytes of data must be loaded during a Software Data Protection Enable cycle.

Table 1 shows the required procedure for enabling the software data protect:

TABLE 1

STEP	MODE	ADD.A14-A0	DATA I/O 7-0
1	Page Write	5555 Hex	AA Hex
2	Page Write	2AAA Hex	55 Hex
3	Page Write	5555 Hex	A0 Hex
4-131	Page Write	Address	Sector Data (128 Bytes)

b) Software Data Protect Disable

The software algorithm of 29C021 includes a six step sequence dummy data programming sequence to disable the software data protect feature described in a). The six step sequence shown in Table 2 must be performed at the beginning of a program cycle. A violation of the six step program sequence in data or address timing and content will abort the procedure and reset the chip to the starting point condition. After a software data protect disable cycle including the six step sequence has been performed, the 29C021 does not require the use of three dummy loads described in a) for the following program cycle. The device is at the software data protect disabled state.

Note: When six step sequence of software data protect disable procedure is performed, if no additional bytes of data is added after the six-step write sequence, the software data protect disable procedure will be aborted. The data protect state will be deactivated at the end of the program period. 128 bytes of data must be loaded during a Software Data Protection disable cycle.

Table 2 shows the required procedure for disabling the software data protect:

TABLE 2

STEP	MODE	ADD.A14-A0	DATA I/O 7-0
1	Page Write	5555 Hex	AA Hex
2	Page Write	2AAA Hex	55 Hex
3	Page Write	5555 Hex	80 Hex
4	Page Write	5555 Hex	AA Hex
5	Page Write	2AAA Hex	55 Hex
6	Page Write	5555 Hex	20 Hex
7-134	Page Write	Address	Sector Data (128 Bytes)

C) Software Chip Clear

The software algorithm of 29C021 includes a sequence of six step dummy data writing to perform a chip clear operation. Table 3 shows the six step write sequence to perform the software chip clear operation:

TABLE 3

STEP	MODE	ADD.A14-A0	DATA I/O 7-0
1	Page Write	5555 Hex	AA Hex
2	Page Write	2AAA Hex	55 Hex
3	Page Write	5555 Hex	80 Hex
4	Page Write	5555 Hex	AA Hex
5	Page Write	2AAA Hex	55 Hex
6	Page Write	5555 Hex	10 Hex

At the end of the six step program sequence shown in Table 3, the device automatically activates its internal timer to control the chip erase cycle; typically takes 20 msec. After a software chip clear operation has been completed, all 2048K bit locations of memory show high level at read operation mode.

d) Software Autoclear Disable Mode

This software algorithm disables the internal automatic clear before a program cycle. Table 4 shows the six steps needed to perform the autoclear disable mode.

TABLE 4

STEP	MODE	ADD.A14-A0	DATA I/O 7-0
1	Page Write	5555 Hex	AA Hex
2	Page Write	2AAA Hex	55 Hex
3	Page Write	5555 Hex	80 Hex
4	Page Write	5555 Hex	AA Hex
5	Page Write	2AAA Hex	55 Hex
6	Page Write	5555 Hex	40 Hex
7-134	Page Write	Address	Sector Data (128 Bytes)

Program operation using the software autoclear disable mode will reduce programming time to typically 40 μ s per byte. The program cycle using software autoclear disable mode is usually used after a chip clear or a software chip clear operation. At the end of the six step sequence, the autoclear before program is disabled and will stay that way unless a power-down occurs or the software autoclear enable procedure is initiated.

e) Software Autoclear Enable Mode

Automatic page clear before page program can be restored to 29C021 either by Vcc power-down or by software autoclear enable mode. Table 5 shows the six step page procedure needed to enable software autoclear mode:

TABLE 5

STEP	MODE	ADD.A14-A0	DATA I/O 7-0
1	Page Write	5555 Hex	AA Hex
2	Page Write	2AAA Hex	55 Hex
3	Page Write	5555 Hex	80 Hex
4	Page Write	5555 Hex	AA Hex
5	Page Write	2AAA Hex	55 Hex
6	Page Write	5555 Hex	50 Hex
7-134	Page Write	Address	Sector Data (128 Bytes)



ABSOLUTE MAXIMUM STRESS RANGES *

TEMPERATURE

Storage: -65° C to 150° C
Under Bias: -55° C to 125° C

ALL INPUT OR OUTPUT VOLTAGES

with respect to Vss +6 V to -0.3 V

* "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature Range: Commercial: 0° C to 70° C
Industrial: -40° C to 85° C
Military: -55° C to 125° C

Vcc Supply Voltage: 5 V ± 10%

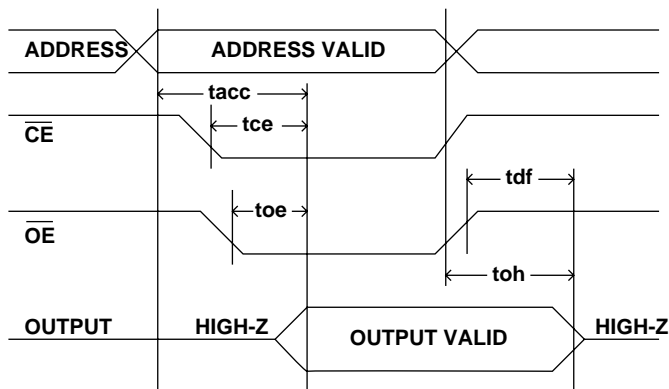
Endurance: 10,000 Cycles/Byte (Typical)

Data Retention: 10 Years

A.C. CHARACTERISTICS - READ OPERATION

Symbol	Parameters	29C021-1		29C021-2		29C021-3		Unit
		Min	Max	Min	Max	Min	Max	
tacc	Address to Output Delay		150		200		250	ns
tce	\overline{CE} to Output Delay		150		200		250	ns
toe	\overline{OE} to Output		80		90		100	ns
tdf	\overline{OE} to Output In High Z	0	50	0	60	0	70	ns
toh	Output Hold from Address Changes, Chip Enable or Output Enable Whichever Occurs First	0		0		0		ns

A.C. Read Wave Forms



D.C. CHARACTERISTICS

(C) = COMMERCIAL
(I) = INDUSTRIAL
(M) = MILITARY

Symbol	Parameter	Condition	Min	Max	Units
Icc	Active Vcc Current	$\overline{CE}=\overline{OE}=V_{il}$; All I/O Open, Min Read or Write Cycle Time		60 (C) 70 (I) 90 (M)	mA
I _{sb1}	CMOS Standby Current	$\overline{CE}=V_{cc}-0.3$ V to $V_{cc}+1$ V		100 (C) 200 (I&M)	μ A
I _{sb2}	TTL Standby Current	$\overline{CE}=V_{ih}$, $\overline{OE}=V_{il}$, All I/O Open, Other Inputs= V_{cc} Max		3	mA
I _{il}	Input Leakage Current	$V_{in}=V_{cc}$ Max		1	μ A
I _{ol}	Output Leakage Current			10	μ A
V _{il}	Input Low Voltage		-0.1	-0.8	V
V _{ih}	Input High Voltage		2	$V_{cc}+0.3$	V
V _{ol}	Output Low Voltage	I _{ol} =2.1 mA		0.45	V
V _{oh}	Output High Voltage	I _{oh} =-0.45 mA	2.4		V

A.C. TEST CONDITIONS

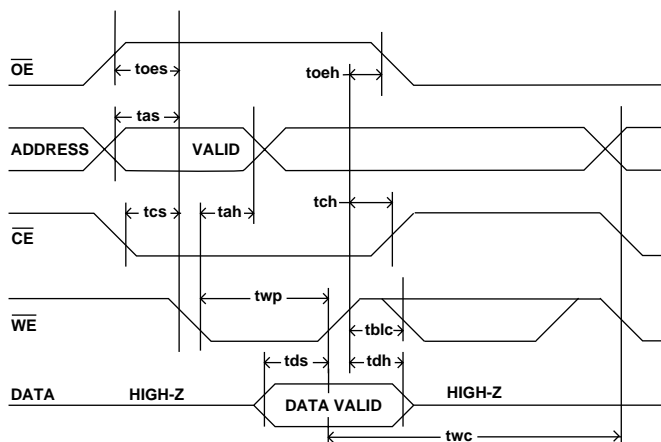
Output Load : 1 TTL Load and C_I=100 pF
Input Rise and Fall Times : < 10 ns
Input Pulse Level : 0.45 V to 2.4V



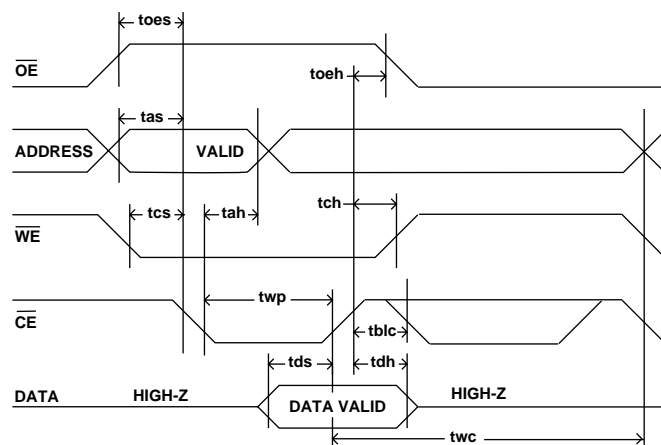
A.C. WRITE CHARACTERISTICS

Symbol	Parameter	Min	Max	Units
tas	Address Set-up Time	20		ns
tah	Address Hold Time	100		ns
tcs	Write Set-up Time	0		ns
tch	Write Hold Time	0		ns
tcw	\overline{CE} Pulse Width	100		ns
twp	\overline{WE} Pulse Width	100		ns
toes	\overline{OE} Set-up Time	10		ns
toeh	\overline{OE} Hold Time	10		ns
tds	Data Set-up Time	50		ns
tdh	Data Hold Time	0		ns
tbic	Byte Load Cycle	0.2	300	μ s
tlp	Last Byte Loaded to Data			
	Polling Output		500	μ s
twc	Write Cycle Time		10	ms

A.C. Write Wave Forms \overline{WE} -Controlled



A.C. Write Wave Forms \overline{CE} -Controlled

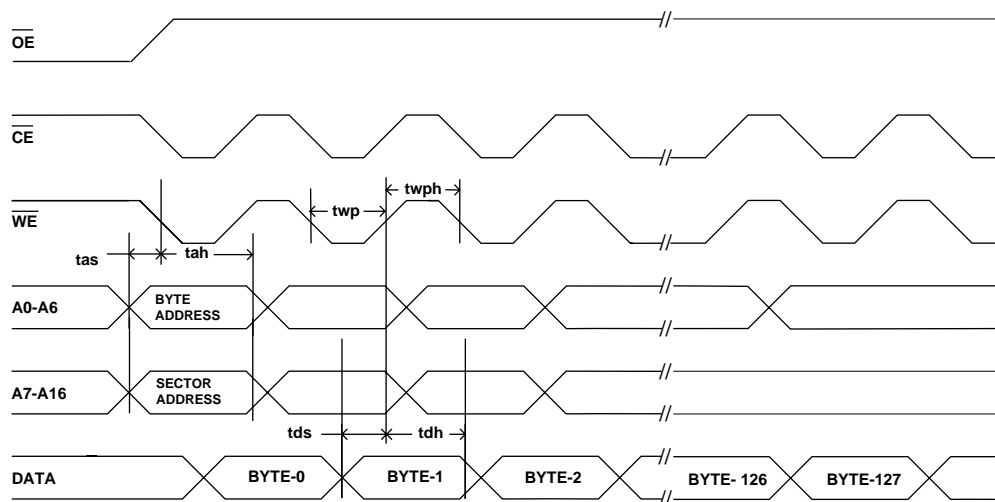




PAGE MODE WRITE CHARACTERISTICS

Symbol	Parameter	Min	Max	Unit
twc	Write Cycle Time		10	ms
tas	Address Set-up Time	20		ns
tah	Address Hold Time	100		ns
tds	Data Set-up Time	50		ns
tdh	Data Hold Time	0		ns
twp	Write Pulse Width	100		ns
tbtc	Byte Load Cycle Time	0.2	300	µs
twph	Write Pulse Width High	100		ns

Page Mode Write Wave Forms (1,2,3)



- Note:
1. A7 through A16 must be specify the sector address during each high to low transition of \overline{WE} or \overline{CE} .
 2. \overline{OE} must be high when \overline{WE} and \overline{CE} are both low.
 3. All bytes that are not loaded within the sector being programmed will be erased to FF.

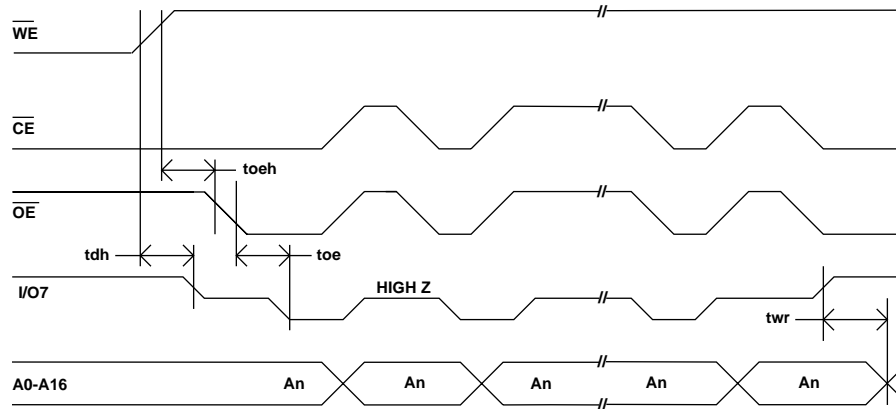


DATA Polling Characteristics

Symbol	Parameter	Min	Max	Unit
tdh	Data Hold Time	10		ns
toeh	\overline{OE} Hold Time	10		ns
toe	\overline{OE} to Output Delay (1)			ns
twr	Write Recovery Time	0		ns

Note: 1. See toe Specification in AC Characteristics - Read Operation

DATA Polling Wave Forms

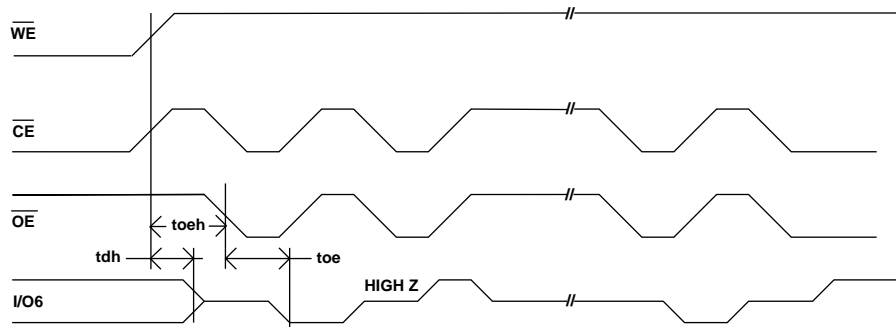


Toggle Bit Characteristics

Symbol	Parameter	Min	Max	Unit
tdh	Data Hold Time	10		ns
toeh	\overline{OE} Hold Time	10		ns
toe	\overline{OE} to Output Delay (1)			ns
toeh	\overline{OE} High Pulse	150		ns

Note: 1. See toe Specification in AC Characteristics - Read Operation

Toggle Bit Wave Forms (1,2,3)



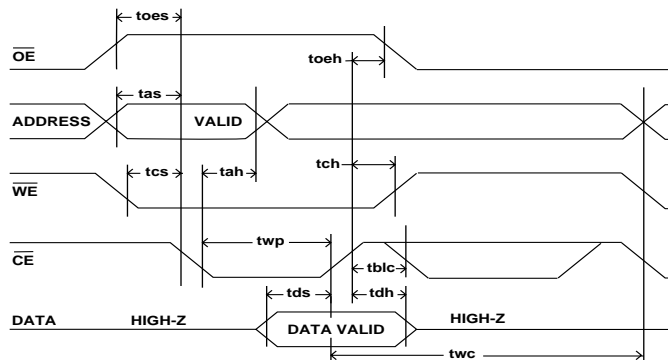
Note:

1. Toggling either \overline{OE} or \overline{CE} or both will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.



Chip Clear Wave Form

The content of the 29C021 may be altered to HIGH by the use of the Chip Clear operation. By setting \overline{CE} to low, \overline{OE} to 12 volts, and \overline{WE} to low, the entire memory can be cleared (written HIGH) within 20 ms. The Chip Clear operation is a latch operation mode. After the Chip Clear starts, the internal chip timer takes over and completes the clear without \overline{CE} , \overline{OE} and \overline{WE} being held active.



TURBO IC PRODUCTS AND DOCUMENTS

1. All documents are subject to change without notice. Please contact Turbo IC for the latest revision of documents.
2. Turbo IC does not assume any responsibility for any damage to the user that may result from accidents or operation under abnormal conditions.
3. Turbo IC does not assume any responsibility for the use of any circuitry other than what embodied in a Turbo IC product. No other circuits, patents, licenses are implied.
4. Turbo IC products are not authorized for use in life support systems or other critical systems where component failure may endanger life. System designers should design with error detection and correction, redundancy and back-up features.

Part Numbers & Order Information

29C021PC-2

256K x 8
PEROM

Package
J -PLCC
P -PDIP
T -TSOP

Temperature
C -Commercial
I -Industrial
M -Military

Speed
-1 150 ns
-2 200 ns
-3 250 ns