

NEW

24-31 GHz Power Amplifier

GaAs Monolithic Microwave IC

Preliminary

Description

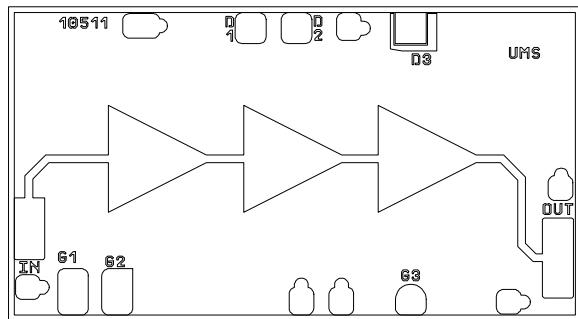
The CHA4042 is a compact three-stage PHEMT HPA MMIC designed for point-to-point multi-point radio, and other Ka-band applications. It provides 25 dBm nominal output power at 1dB gain compression over the 24-31 GHz frequency range, and 15dB small signal gain.

The circuit is manufactured with a $0.25\mu\text{m}$ gate length power PHEMT process on $70\text{-}\mu\text{m}$ substrate, via holes through the substrate, air bridges and electron beam gate lithography.

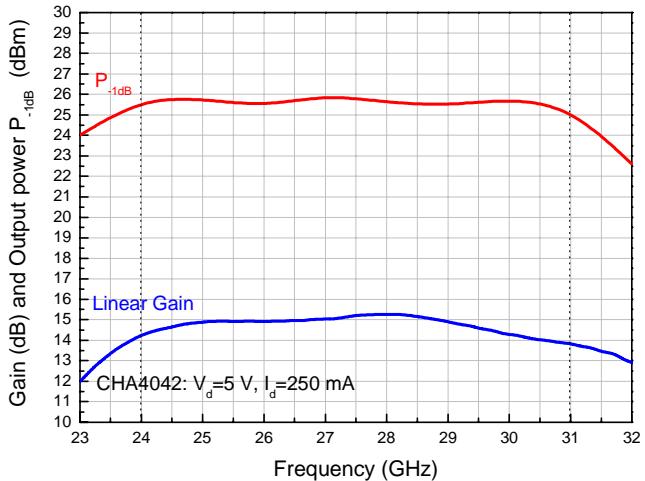
It is available in chip form. The backside of the chip is both RF and DC grounds. This helps to simplify the assembly process.

Main Features

- Broadband performances : 24-31GHz
- $15\text{dB} \pm 1\text{dB}$ linear gain
- 25.5dBm output power at 1-dB comp.
- Chip size : $1.93 \times 1.09 \times 0.07\text{mm}^3$



Chip size 2.1mm^2



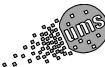
Typical MMIC characteristic

Main Characteristics

Tamb = +25°C, Vd = 5V

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	24		31	GHz
G	Small signal gain	14	15		dB
P1dB	CW output power at 1dB gain compression	25	25.5		dBm
Vd	Drain bias voltage		5		V
Id	Bias current		250	500	mA

ESD Protection : Electrostatic discharge sensitive device. Observe handling precautions !



Electrical characteristics in JIG test fixture

Tamb = +25°C, Vd = 5V, Id=250mA (typically Vg=-0.4V)

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	24		31	GHz
G	Small signal gain (1)	14	15		dB
ΔG	Small signal gain flatness		± 1		dB
P1dB	CW output power at 1dB gain compression (2)	25	25.5		dBm
Psat	Saturated output power (1)	26	27		dBm
IP3	3 rd order intercept point (1)		-		dBm
RLin	Input return loss (1)		-10	-9	dB
RLout	Output return loss (1)		-7	-5	dB
Is	Reverse Isolation (2)		40		dB
Vd	Drain bias voltage		5		V
Id	Bias current		250		mA
Vg	Gate bias voltage		-0.4		V

(1) These values are representative for CW JIG test fixture measurements, that are made with bond wires at RF ports.

(2) CW on-wafer measurements.

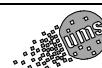
Absolute Maximum Ratings (2)

Tamb = +25°C

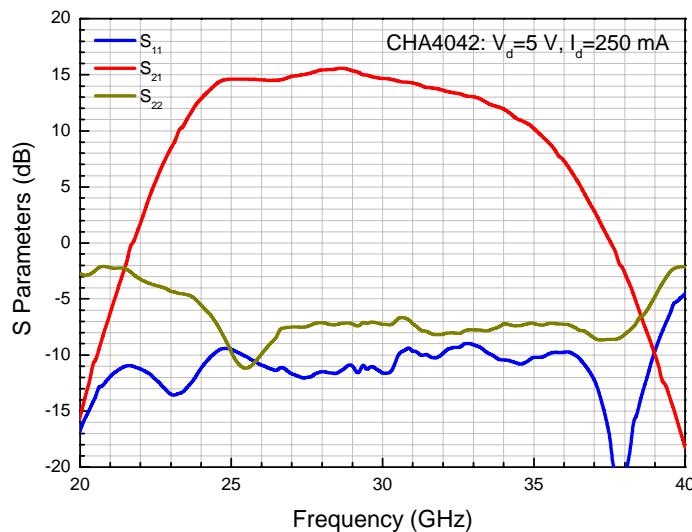
Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	6.5	V
Id	Maximum drain current	500	mA
Vg	Min. and max. gate bias voltage	-2.5 ~ 0	V
Pin	Maximum peak input power overdrive (3)	+15	dBm
Top	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +125	°C

(2) Operation of this device above anyone of these parameters may cause permanent damage.

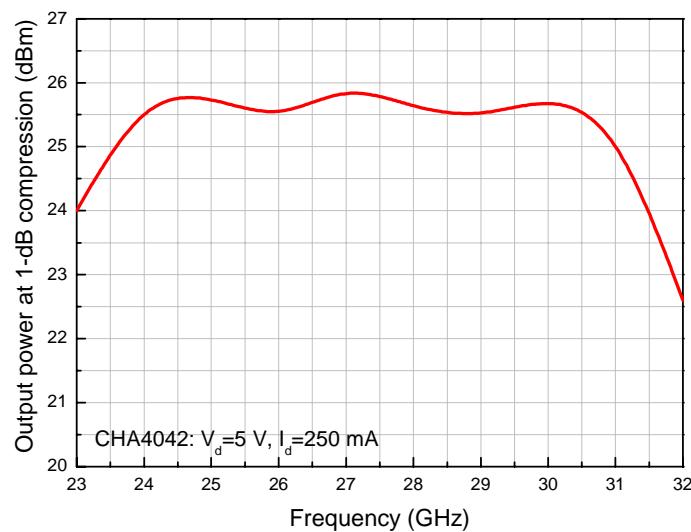
(3) Duration < 1s.



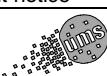
Typical CW performance @ Tamb=25°C



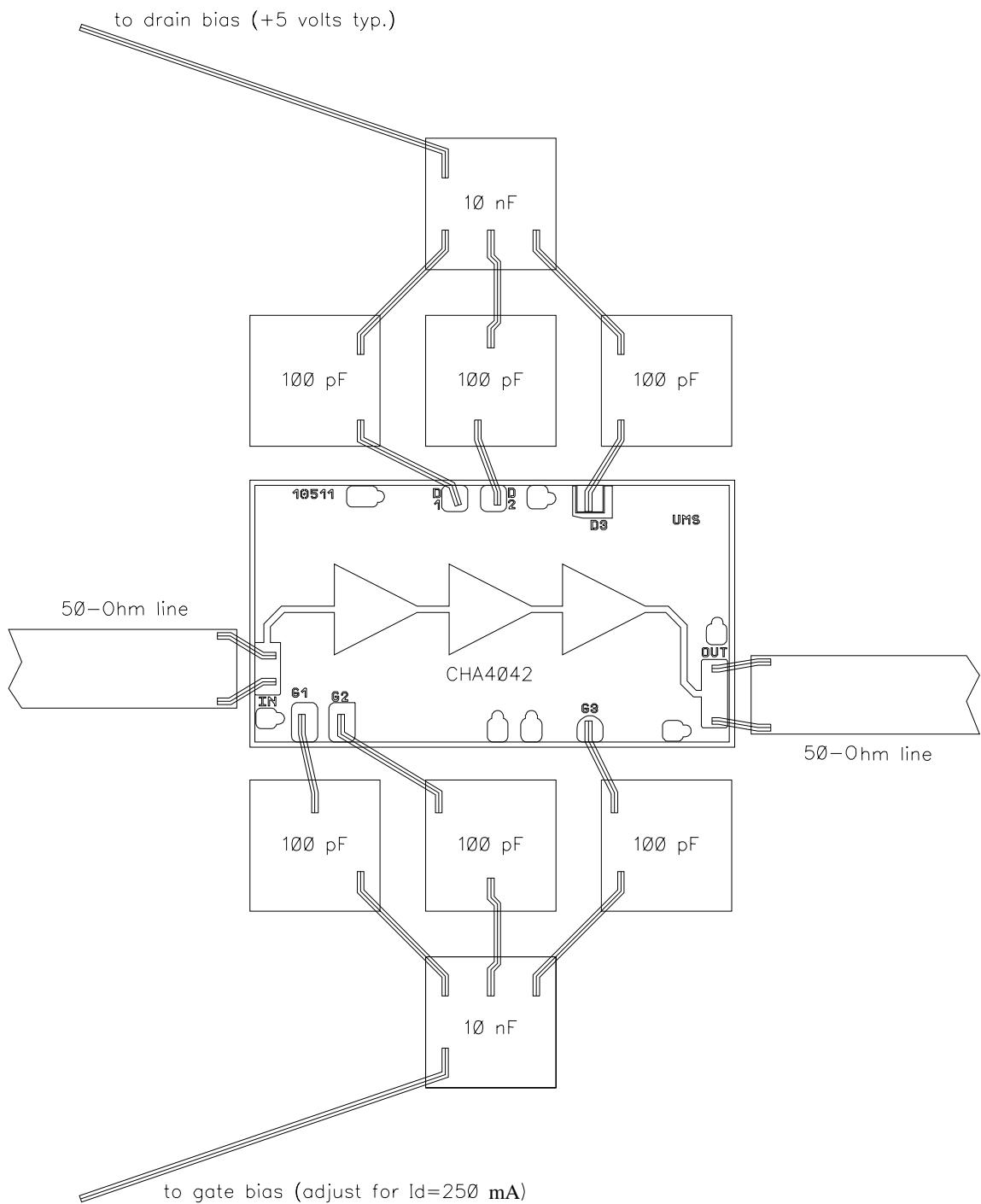
Typical JIG test fixture S-parameter measurements (test fixture losses uncorrected)



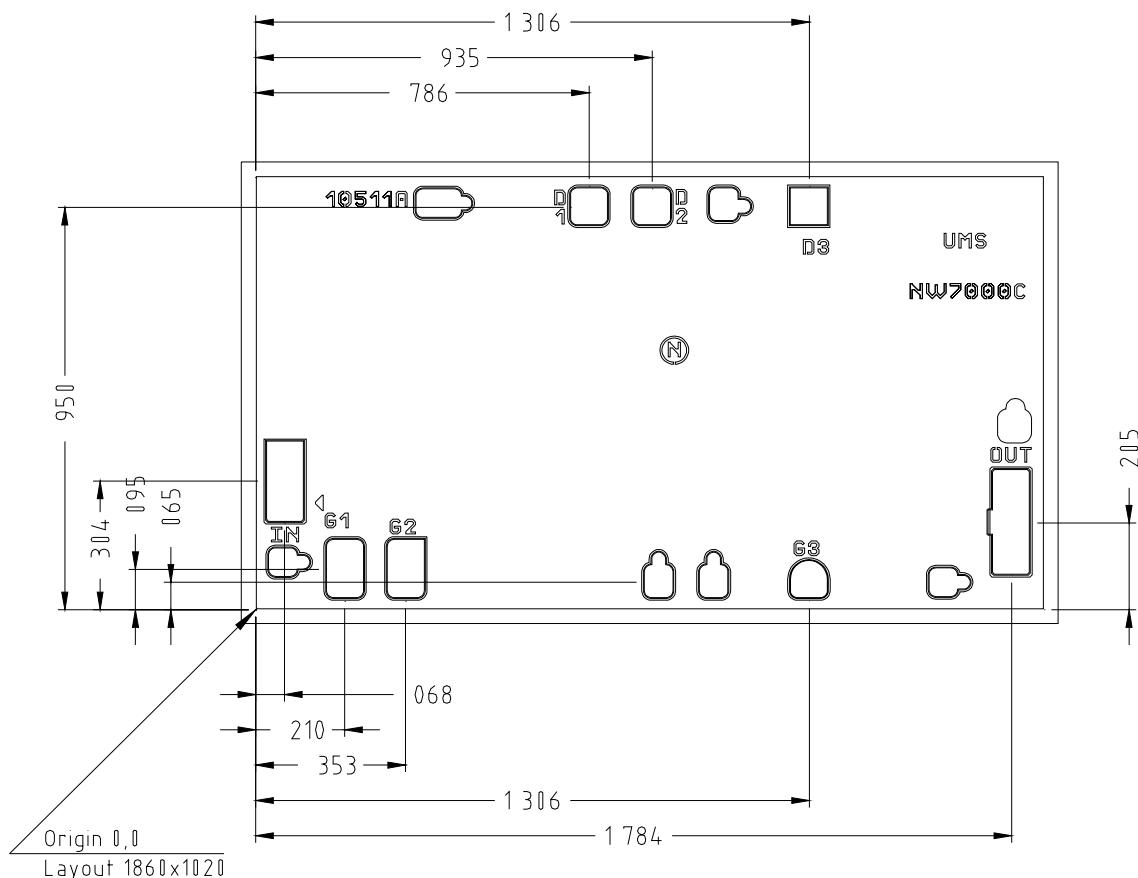
Typical CW output power at 1-dB gain compression (on-wafer measurements)



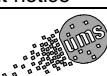
Chip Assembly and Mechanical Data

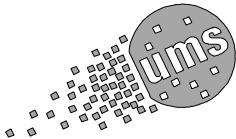


Bonding pad positions



DIMENSIONS : /units μm /
 $1930 \pm 35 \times 1090 \pm 35$
Thickness : 70





Ordering Information

Chip form : CHA4042-99F/00

Information furnished is believed to be accurate and reliable. However **United Monolithic Semiconductors S.A.S.** assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of **United Monolithic Semiconductors S.A.S.**. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. **United Monolithic Semiconductors S.A.S.** products are not authorised for use as critical components in life support devices or systems without express written approval from **United Monolithic Semiconductors S.A.S.**

