

5.8GHz I/Q Mixer

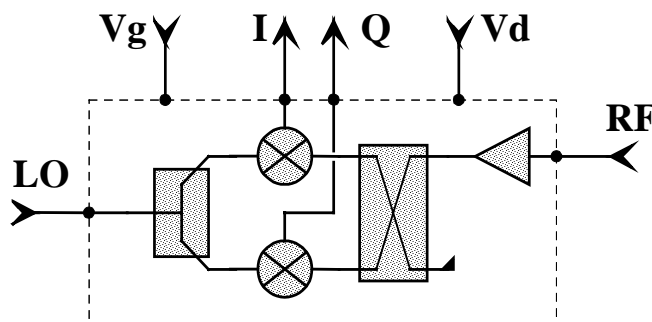
GaAs Monolithic Microwave IC

Description

The CHR0100a is a single chip MMIC including an I/Q mixer and a RF gain block that minimises the overall conversion loss of the receiver and provides the RF signal to the mixer through a power divider.

The circuit is manufactured with the P-HEMT process : 0.25 μ m gate length, via holes through the substrate, air bridges and electron beam gate lithography.

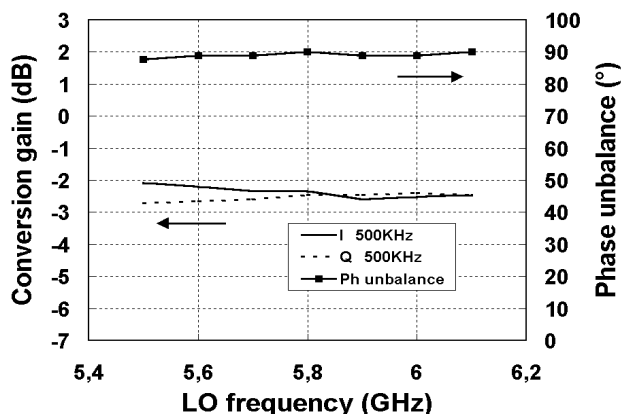
It is supplied in chip form or in ceramic leadless chip carrier.



Block diagram

Main Features

- 5.8GHz centre frequency
- DC-50MHz IF bandwidth
- Low noise figure
- Low I/Q phase & amplitude unbalance
- Chip size : 1.77 x 1.37 x 0.10 mm



*Conversion gain (RF to I; RF to Q)
and phase unbalance*

Main Characteristics

Tamb = +25°C

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fop	Operating frequency range	5.725	5.8	5.875	GHz
Cg	Conversion gain (RF to I; RF to Q)	-4	-2.5		dB
Plo	LO input power		6		dBm

ESD Protections : Electrostatic discharge sensitive device observe handling precaution !

Electrical Characteristics

Tamb = +25°C

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Fop	Operating frequency range		5.725	5.8	5.875	GHz
BWif	IF frequency band		DC		50	MHz
Cg	Conversion gain, RF to I or RF to Q	(1)	-4	-2.5		dB
NF	Noise figure (DSB), RF to I or RF to Q IF=10MHz			5		dB
Pif_1dB	I or Q IF output power at 1dB compression gain			-5		dBm
Plo	LO input power		5	8		dBm
$\Delta\phi$	I/Q phase unbalance			10	15	°
ΔCg	I/Q amplitude unbalance			0.5	1.0	dB
Vd	Positive bias voltage			4		V
Id	Bias current			15	25	mA

(1) Conversion gain will be 3dB higher after I/Q combination.

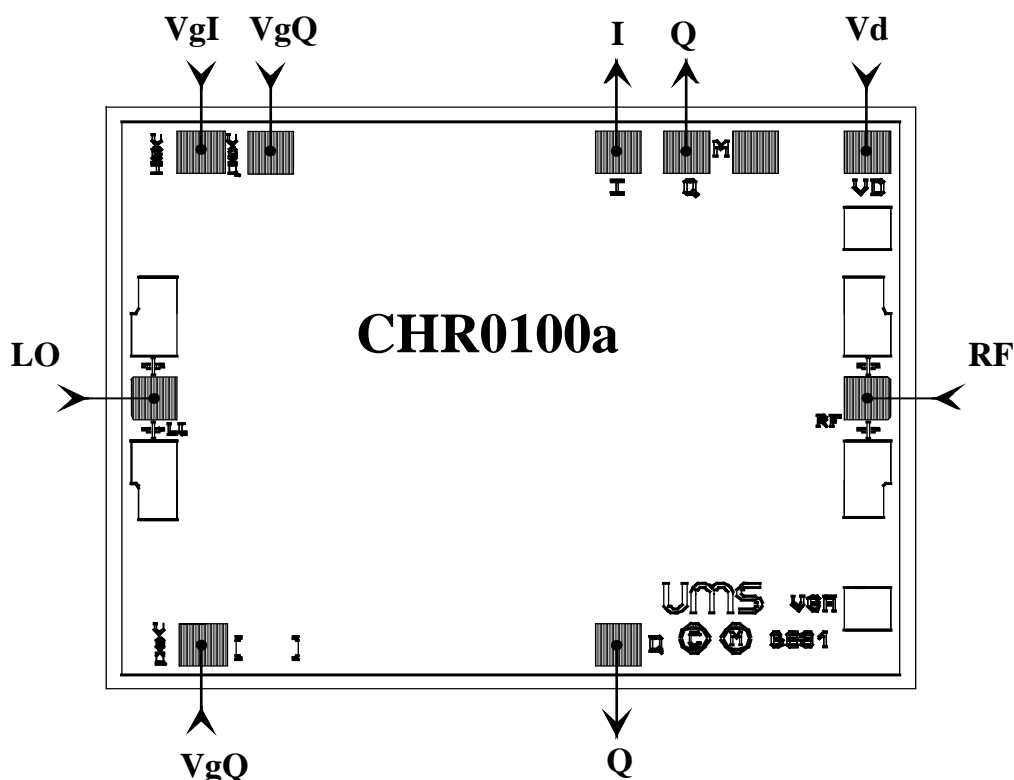
Absolute Maximum Ratings (1)

Tamb = +25°C

Symbol	Parameter	Values	Unit
Vd	Positive supply voltage	6	V
Vg	Negative supply voltage	-2 to 0	V
Pin	Maximum peak input power overdrive (2)	10	dBm
Top	Operating temperature range	-50 to 70	°C
Tstg	Storage temperature range	-55 to 155	°C

(1) Operation of this device above any one of these parameters may cause permanent damage

(2) Duration < 1s.

Chip Pad Allocation**Input And Output Pin References**

Pin	Description
RF	RF signal input
LO	LO signal input
VgI	I mixer negative supply voltage
VgQ	Q mixer negative supply voltage
Vd	Positive supply voltage
I	First IF output
Q	Second IF output (in quadrature)

Connection of only one of the two VgQ and Q pads is necessary
 VgI, VgQ only necessary for low LO power

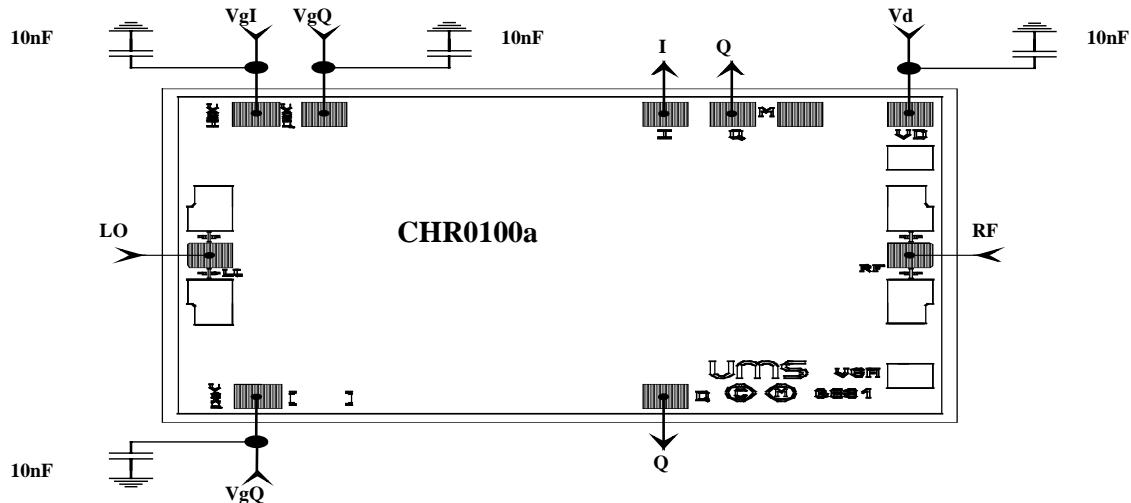
Typical Bias Configuration

The typical bias voltage applied to the chip is $V_d = 4V$.

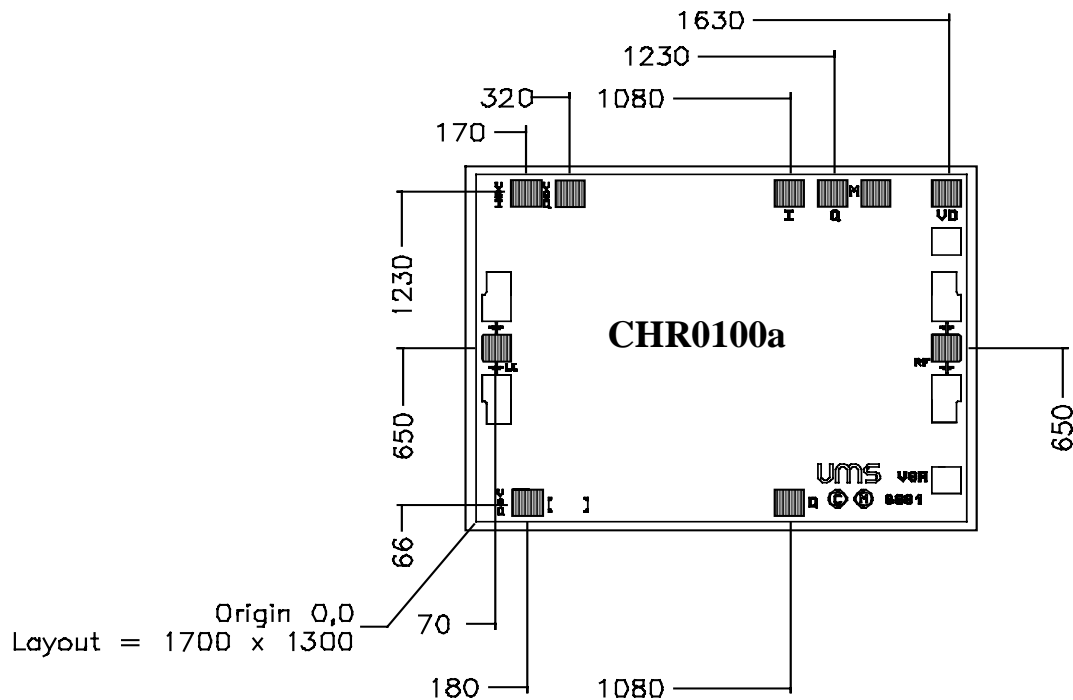
If the LO power is low (ex: $< 5\text{dBm}$) one can apply a negative voltage ($-0.3V$) on V_g to improve and secure the conversion characteristic.

Each V_g and V_d port should have a 10nF decoupling capacitor to the ground.

Connection of only one of the two V_{gQ} and Q pads is necessary

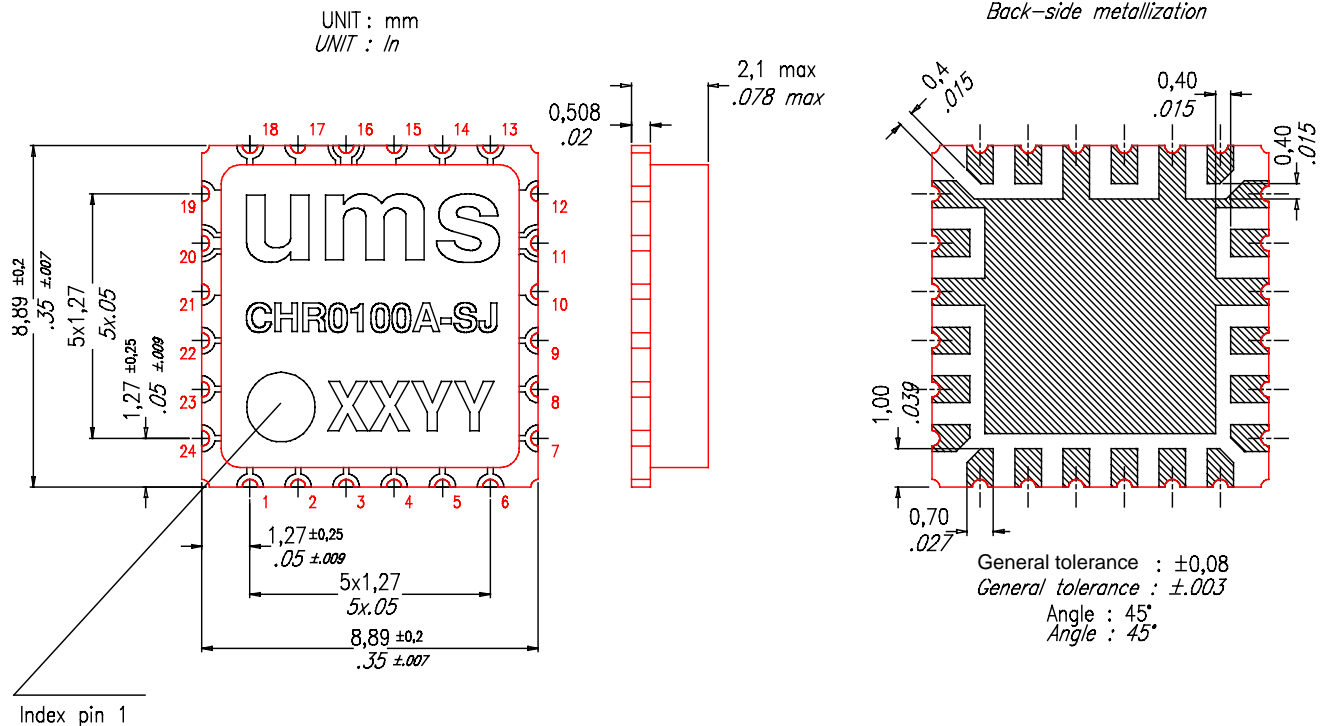


Chip Mechanical Data



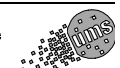
Chip size $1770 \pm 20 \mu\text{m} \times 1370 \pm 20 \mu\text{m}$

Chip thickness $100 \pm 10 \mu\text{m}$



Package Pin Allocation (SJ)

Pin	Number	Description
RF	20	RF signal input
LO	11	LO signal input
Vgl	7	I mixer negative supply voltage
VgQ	6	Q mixer negative supply voltage
Vd	1	Positive supply voltage
I	4	First IF output
Q	3	Second IF output (in quadrature)
	10,12,15,17, 19,21	GROUND
	2,5,8,9,13,14, 16,18,22,23,24	Not connected



Ordering Information

Chip form : CHR0100a99F/00

Package : CHR0100aSJF/24

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