

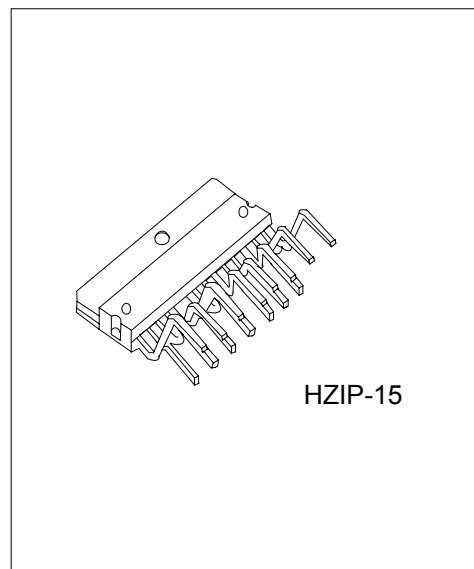
5W+5W AMPLIFIER WITH DC VOLUME CONTROL

DESCRIPTION

The UTC **TDA8496** is a stereo 5+5W class AB power amplifier with mute and dc volume control, assembled in the HZIP-15 package. It is designed for high quality sound, LCD TV or LCD Monitor applications.

FEATURES

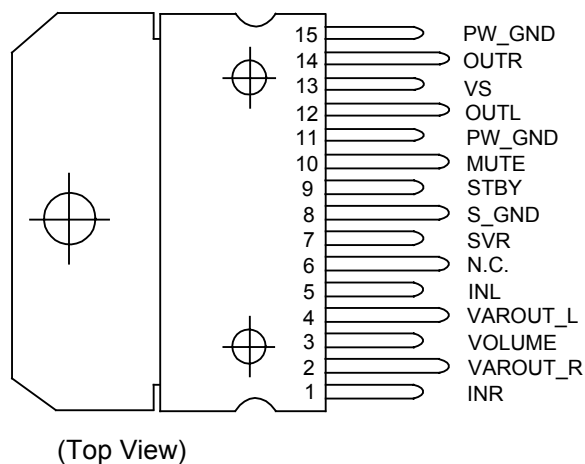
- * 5+5W OUTPUT POWER @ $V_{CC} = 22V$; $R_L = 8\Omega$
- * LOW TURN-ON TURN-OFF POP NOISE
- * LOW EXTERNAL COMPONENTS
- * SHORT CIRCUIT & THERMAL OVERLOAD PROTECTION
- * LINEAR VOLUME CONTROL BY DC VOLTAGE
- * SOFT CLIPPING
- * INTERNALLY FIXED GAIN
- * ST-BY AND MUTE FUNCTIONS



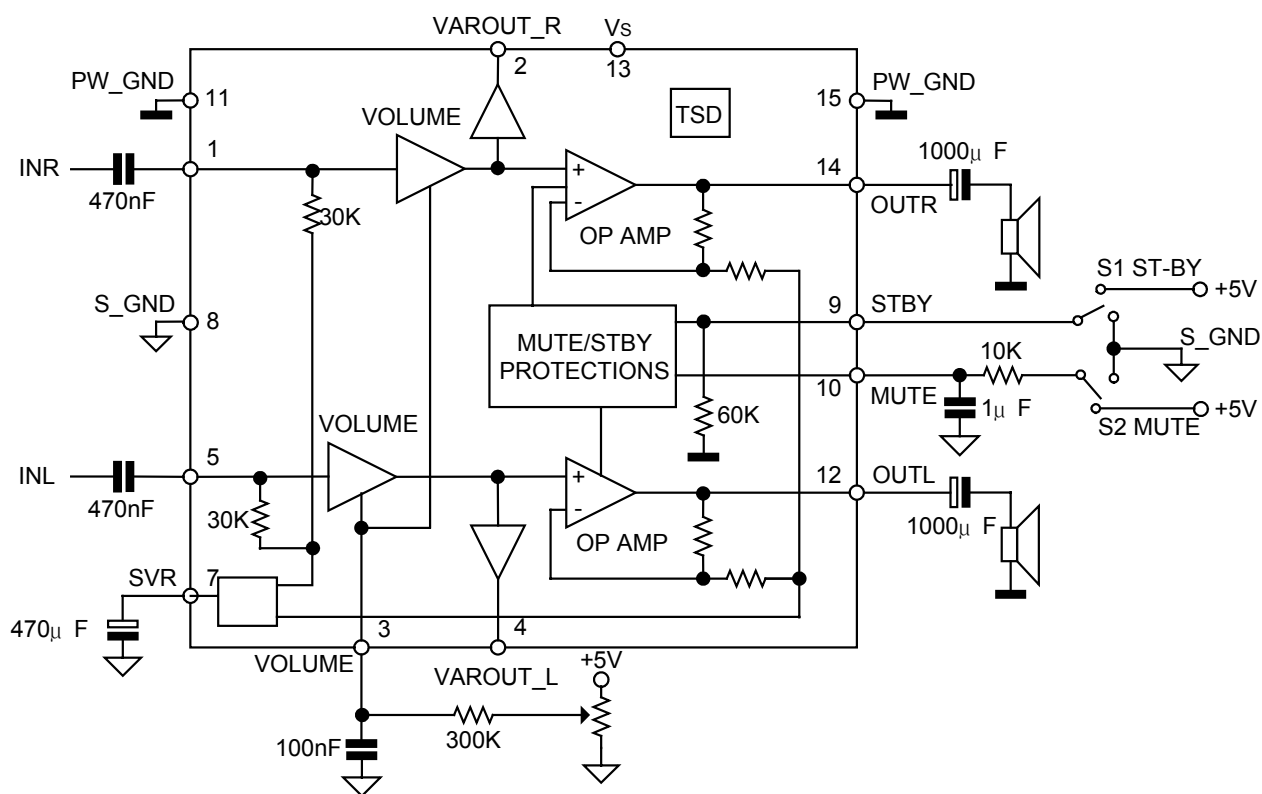
HZIP-15

*Pb-free plating product number: TDA8496L

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT
DC Supply voltage	V_S	35	V
Maximum Input Voltage	V_{IN}	8	V_{PP}
Volume Control DC Voltage	V_3	7	V
Total Power Dissipation ($T_a = 80^\circ\text{C}$)	P_{tot}	15	W
Ambient Operating Temperature	T_{amb}	0 ~ 70	$^\circ\text{C}$
Junction Temperature	T_j	-40 ~ 150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-40 ~ 150	$^\circ\text{C}$

THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Thermal Resistance junction-case	Θ_{JC}	Typ. = 4, Max. = 4.6	$^\circ\text{C}/\text{W}$
Thermal Resistance junction-ambient Max.	Θ_{JA}	35	$^\circ\text{C}/\text{W}$

ELECTRICAL CHARACTERISTICS(Refer to the test circuit $V_S = 22V$, $R_L = 8\Omega$, $R_g = 50\Omega$, $T_a = 25^\circ C$)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage Range	V_S		10		32	V
Total Quiescent Current	I_q			25	50	mA
Output DC Offset Referred to SVR Potential	DCV_{OS}	No Input Signal		200		mV
Quiescent Output Voltage	V_O			11		V
Output Power	P_O	THD = 10%, $R_L = 8\Omega$	5	5.5		W
		THD = 1%, $R_L = 8\Omega$		4		
		THD = 10%, $R_L = 4\Omega$, $V_S = 12V$ THD = 1%, $R_L = 4\Omega$, $V_S = 12V$		2.1 1.0		W
Total Harmonic Distortion	THD	$G_V = 30dB$, $P_O = 1W$, $f = 1KHz$			0.4	%
Output Peak Current	I_{peak}	(internally limited)	1.0	1.3		A
Input Signal	V_{IN}				2.8	Vrms
Closed Loop Gain	G_V	$V_{OI\ Ctrl} > 4.5V$	28.5	30	31.5	dB
Monitor Out Gain	G_{VLine}	$V_{OI\ Ctrl} > 4.5V$, $Z_{load} > 30K\Omega$	-1.5	0	1.5	dB
Attenuation at Minimum Volume	$A_{Min} V_{OL}$	$V_{OI\ Ctrl} < 0.5V$	80			dB
	BW			0.6		MHz
Total Output Noise	eN	$f = 20Hz \sim 22KHz$ (PLAY, max volume)		500	800	μV
		$f = 20Hz \sim 22KHz$ PLAY, max attenuation		100	250	μV
		$f = 20Hz \sim 22KHz$ MUTE		60	150	μV
Slew Rate	SR		5	8		V/ μs
Input Resistance	R_i		22.5	30		K Ω
Variable Output Resistance	$R_{Var\ Out}$			30	100	Ω
Variable Output Load	$R_{L\ Var\ Out}$		2			K Ω
Supply Voltage Rejection	SVR	$f = 1KHz$, max volume $C_{SVR} = 470mF$, $V_{RIP} = 1Vrms$	35	39		dB
		$f = 1KHz$, max attenuation $C_{SVR} = 470mF$, $V_{RIP} = 1Vrms$	55	65		dB
Thermal Muting	T_M			150		$^\circ C$
Thermal Shut-down	T_S			160		$^\circ C$
MUTE STAND-BY & INPUT SELECTION FUNCTIONS						
Stand-by ON Threshold	V_{ST-ON}		3.5			V
Stand-by OFF Threshold	V_{ST-OFF}				1.5	V
Mute ON threshold	V_{MUTEON}		3.5			V
Mute OFF threshold	$V_{MUTEOFF}$				1.5	V
Mute Attenuation	A_{MUTE}		50	65		dB
Quiescent Current @ Stand-by	I_{qST-BY}			0.6	1	mA
Stand-by bias current	$I_{stbyBIAS}$	Stand by ON: $V_{ST-BY} = 5V$, $V_{mute} = 5V$		80		μA
		Play or Mute	-20	-5		μA
Mute Bias Current	$I_{muteBIAS}$	Mute		1	5	μA
		Play		0.2	2	μA

The schematic diagram illustrates the internal architecture of the TSD1000 audio IC, which includes two operational amplifiers (OP AMP), a TSD (Thermal Shutdown) block, and a MUTE/STBY PROTECTIONS block. The IC is configured for stereo audio processing with two channels (L and R).

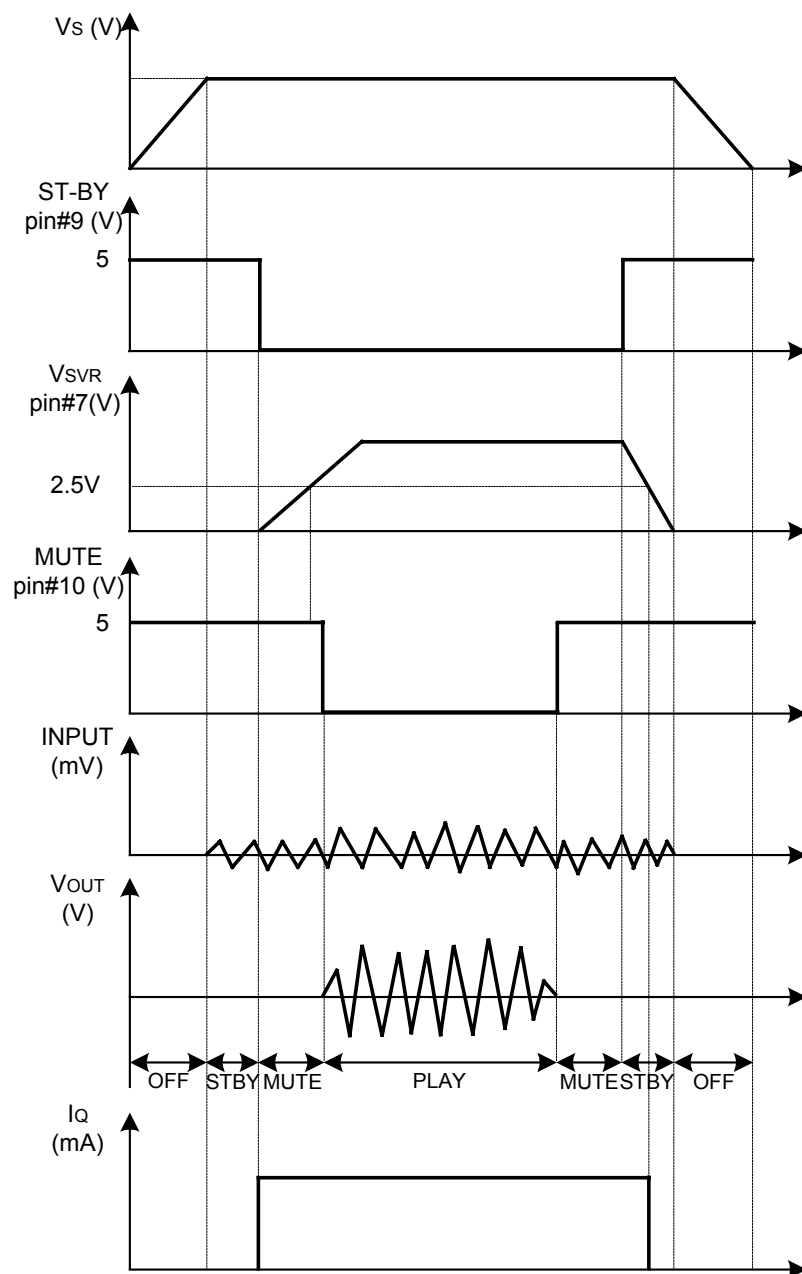
Key Components and Connections:

- Power Supply:** +Vs and -Vs are connected to the top and bottom pins (13 and 14) respectively. A 1000μF capacitor (C1) is connected to +Vs, and a 0.1μF capacitor (C9) is connected to -Vs.
- Input Stage:** The INR (Right Input) is connected to pin 1 through a 470nF capacitor (C2). The INL (Left Input) is connected to pin 5 through a 470nF capacitor (C3). A 30K resistor is connected between pins 1 and 2, and another 30K resistor is connected between pins 5 and 6.
- Volume Control:** The VOLUME control is implemented using two potentiometers (P1 and P2) connected to pins 2 and 4. The wipers of these potentiometers are connected to pins 3 and 4, respectively. A 100nF capacitor (C5) is connected to pin 3 to ground.
- Output Stage:** The OP AMPs drive the OUTL (Left Output) and OUTR (Right Output) pins. The output filters are implemented using 1000μF capacitors (C6 and C8) connected to pins 12 and 14, respectively, to ground.
- Protection and Control:** The MUTE/STBY PROTECTIONS block is connected to pins 9 and 10. It controls the output via switches S1 (ST-BY) and S2 (MUTE). A 1μF capacitor (C7) and a 10K resistor (R2) are connected to pins 9 and 10, respectively.
- Thermal Shutdown (TSD):** The TSD block is connected to pins 2 and 13, providing thermal protection for the IC.
- Other Pins:** Pin 8 is connected to S_GND. Pin 7 is connected to SVR (Speaker Volume Register) through a 470μF capacitor (C4). Pin 11 is connected to PW_GND. Pin 15 is connected to PW_GND.

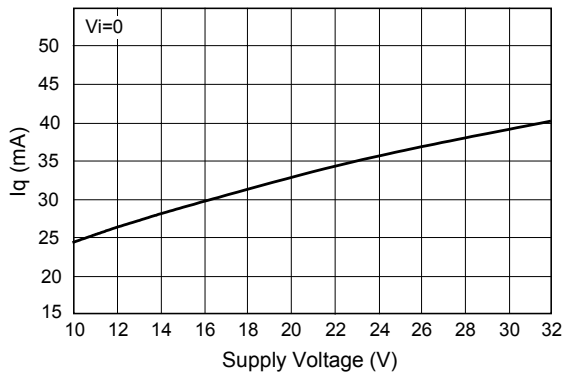
MUTE	St-BY	OPERATING CONDITION
H	H	STAND-BY
L	H	STAND-BY
H	L	MUTE
I	I	PLAY

Turn ON/OFF Sequences

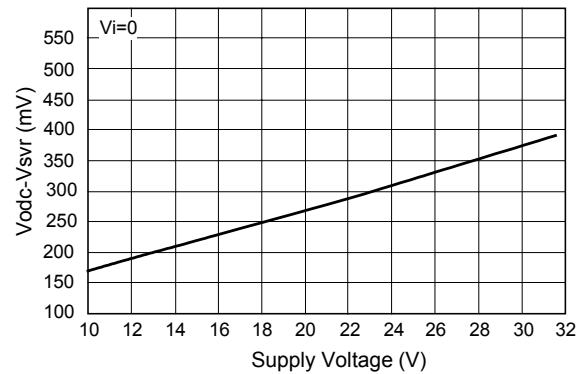
USING ONLY THE MUTE FUNCTION



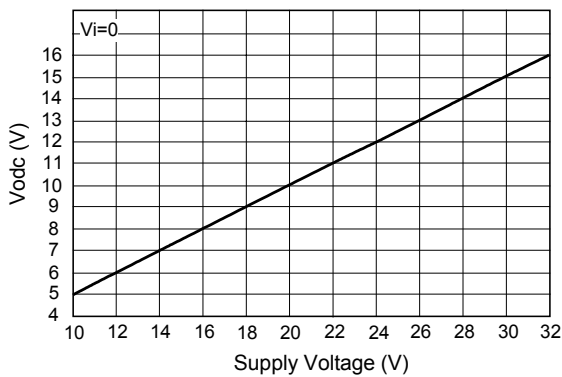
Quiescent Current vs. Supply Voltage



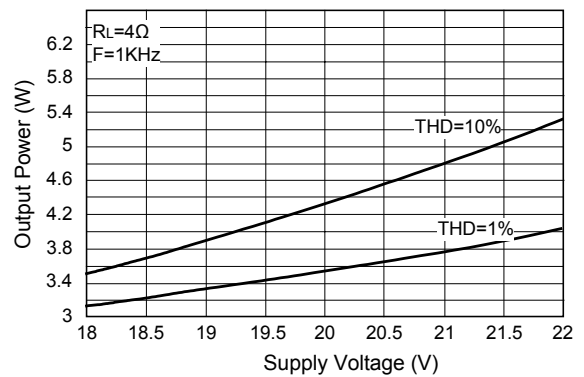
Output DC Offset vs. Supply Voltage



Output Dc Offset vs. Supply Voltage



Output Power vs Supply Voltage



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