Low-Voltage, Low r_{ON} Quad SPST Analog Switch

FEATURES

- Low Voltage Operation (1.8 V to 5.5 V)
- Low On-Resistance - $r_{DS(on)}$: 1.0 Ω
- Fast Switching - 14 ns t_{ON}
- Low Charge Injection - Q_{INJ}: 1 pC
- Low Power Consumption
- TTL/CMOS Compatible
- TSSOP-16 and QFN-16 Packages

BENEFITS

- Reduced Power Consumption
- Simple Logic Interface
- High Accuracy
- Reduce Board Space

APPLICATIONS

- Cellular Phones
- Communication Systems
- Portable Test Equipment
- Battery Operated Systems
- Sample and Hold Circuits

DESCRIPTION

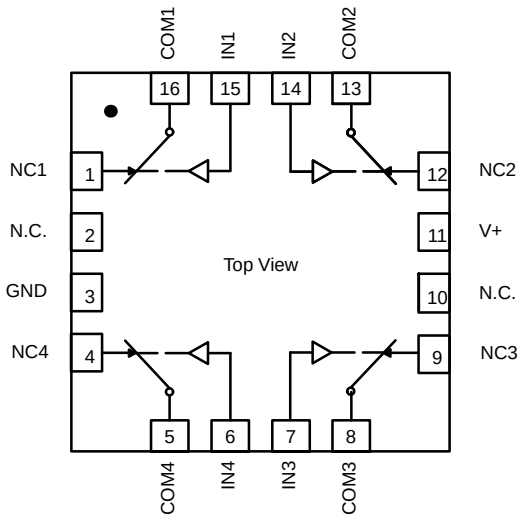
The DG2041/2042/2043 are quad single-pole/single-throw monolithic CMOS analog switch designed for high performance switching of analog signals. Combining low power, fast switching, low on-resistance ($r_{DS(on)}$: 1.0 Ω @ 2.7 V) and small physical size, the DG2041/2042/2043 are ideal for portable and battery powered applications requiring high performance and efficient use of board space.

The DG2041/2042/2043 are built on Vishay Siliconix's new high density low voltage process. An epitaxial layer prevents latchup.

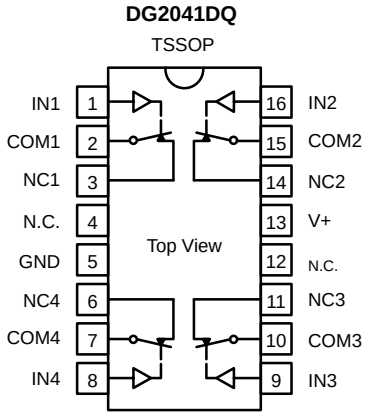
Each switch conducts equally well in both directions when on, and blocks up to the power supply level when off.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION—DG2041

DG2041DN
QFN-16 (4 X 4)



DG2041DQ
TSSOP

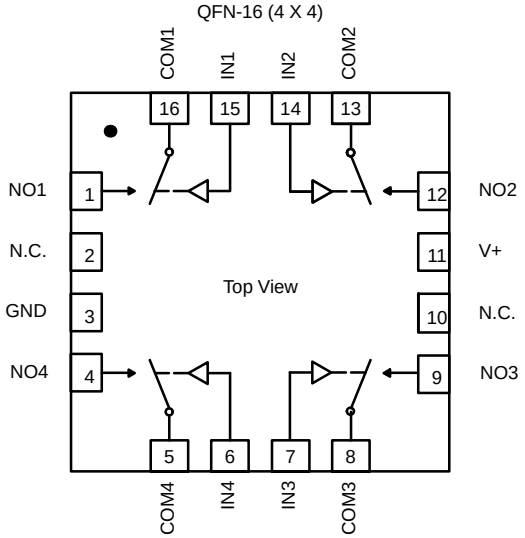


TRUTH TABLE DG2041	
Logic	**Switch**
0	On
1	Off

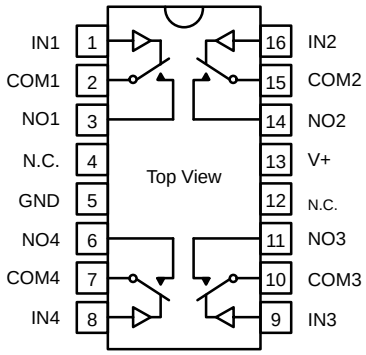
Switches Shown for Logic "0" Input

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION—DG2042

DG2042DN
QFN-16 (4 X 4)



DG2042DQ
TSSOP

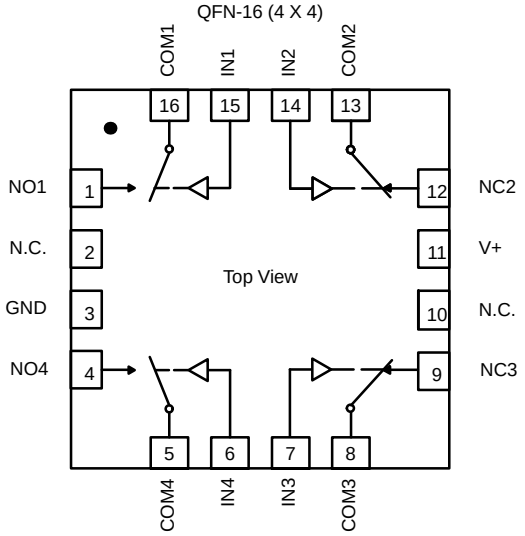


TRUTH TABLE DG2042	
Logic	**Switch**
0	Off
1	On

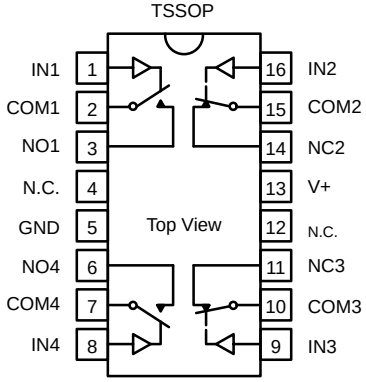
Switches Shown for Logic “0” Input

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION—DG2043

DG2043DN
QFN-16 (4 X 4)



DG2043DQ
TSSOP



TRUTH TABLE DG2043		
Logic	**Switches 1, 4**	**Switches 2, 3**
0	Off	On
1	On	Off

Switches Shown for Logic “0” Input

ORDERING INFORMATION		
Temp Range	**Package**	**Part Number**
-40 to 85°C	TSSOP-16	DG2041DQ
		DG2042DQ
		DG2043DQ
	QFN-16 (4x4 mm)	DG2041DN
		DG2042DN
		DG2043DN

ABSOLUTE MAXIMUM RATINGS

Reference to GND
V+ ..... -0.3 to +6 V
IN, COM, NC, NO[a] ..... -0.3 to (V+ + 0.3 V)
Continuous Current (Any terminal) ..... ±50 mA
Peak Current ..... ±200 mA
(Pulsed at 1 ms, 10% duty cycle)
Storage Temperature (D Suffix) ..... -65 to 150°C
Power Dissipation (Packages)[b]
TSSOP-16[c] ..... 450 mW
QFN-16 (4 x 4 mm)[d] ..... 1880 mW

Notes:
a. Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 5.6 mW/°C above 70°C
d. Derate 23.5 mW/°C above 70°C
e. Manual soldering with soldering iron is not recommended for leadless components. The QFN is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper lip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

SPECIFICATIONS (V+ = 2.0 V)

Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 2.0 V, V_{IN} = 0.4 or 1.6 V[e]	Temp[a]	Limits -40 to 85°C Min[b]	Typ[c]	Max[b]	Unit
Analog Switch							
Analog Signal Range[d]	V_{NO}, V_{NC}, V_{COM}		Full	0		V+	V
On-Resistance	r_{ON}	V+ = 2.0 V, V_{COM} = 0.2 V/1.2 V, I_{NO}, I_{NC} = 10 mA	Room Full[d]		3.0	6.3 6.3	Ω
r_{ON} Flatness[d]	r_{ON} Flatness	V+ = 2.0 V, V_{COM} = 0 to V+, I_{NO}, I_{NC} = 10 mA	Room			4.2	Ω
r_{ON} Match Between Channels	Δ r_{ON}		Room			0.4	Ω
Switch Off Leakage Current[f]	$I_{NO(off)}$, $I_{NC(off)}$	V+ = 2.2 V V_{NO}, V_{NC} = 0.2 V/2.0 V, V_{COM} = 2.0 V/0.2 V	Room Full[d]	-1 -10		1 10	nA
	$I_{COM(off)}$		Room Full[d]	-1 -10		1 10	nA
Channel-On Leakage Current[f]	$I_{COM(on)}$	V+ = 2.2 V, V_{NO}, V_{NC} = V_{COM} = 0.2 V/2.0 V	Room Full[d]	-1 -10		1 10	nA
Digital Control							
Input High Voltage	V_{INH}		Full	1.6			V
Input Low Voltage	V_{INL}		Full			0.4	V
Input Capacitance[d]	C_{in}		Full		4		pF
Input Current	I_{INL} or I_{INH}	V_{IN} = 0 or V+	Full	-1		1	µA

SPECIFICATIONS (V+ = 2.0 V)

Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 2.0 V, V_{IN} = 0.4 or 1.6 V[e]	Temp[a]	Limits -40 to 85°C Min[b]	Typ[c]	Max[b]	Unit
Dynamic Characteristics							
Turn-On Time	t_{ON}	V_{NO} or V_{NC} = 1.5 V, R_L = 300 Ω, C_L = 35 pF Figures 1 and 2	Room Full[d]		30	81 82	ns
Turn-Off Time	t_{OFF}		Room Full[d]		22	41 42	
Break-Before-Make Time Delay	t_D	V_{NO} or V_{NC} = 1.5 V, R_L - 300 Ω, C_L - 35 pF (DG2043 Only)	Room	5			
Charge Injection[d]	Q_{INJ}	C_L = 1 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω, Figure 2	Room		1		pC
Off-Isolation[d]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room		-63		dB
Crosstalk[d]	X_{TALK}		Room		-95		
NO, NC Off Capacitance[d]	$C_{NO(off)}$, $C_{NC(off)}$	V_{IN} = 0 or V+, f = 1 MHz	Room		24		pF
Channel-On Capacitance[d]	C_{ON}		Room		48		
Power Supply							
Power Supply Current[d]	I+	V_{IN} = 0 or V+			0.001	1.0	μA

SPECIFICATIONS (V+ = 3.0 V)

Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 3 V, ±10%, V_{IN} = 0.4 or 2.0 V[e]	Temp[a]	Limits -40 to 85°C Min[b]	Typ[c]	Max[b]	Unit
Analog Switch							
Analog Signal Range[d]	V_{NO}, V_{NC}, V_{COM}		Full	0		V+	V
On-Resistance	r_{ON}	V+ = 2.7 V, V_{COM} = 0.7 V/1.5 V, I_{NO}, I_{NC} = 10 mA	Room Full		1.6	2.1 2.2	Ω
r_{ON} Flatness[d]	r_{ON} Flatness	V+ = 2.7 V, V_{COM} = 0 to V+, I_{NO}, I_{NC} = 10 mA	Room			0.7	
r_{ON} Match Between Channels	Δ r_{ON}		Room			0.3	
Switch Off Leakage Current[f]	$I_{NO(off)}$, $I_{NC(off)}$	V+ = 3.3 V V_{NO}, V_{NC} = 0.3 V/3.0 V, V_{COM} = 3.0 V/0.3 V	Room Full	-1 -10		1 10	nA
	$I_{COM(off)}$		Room Full	-1 -10		1 10	
Channel-On Leakage Current[f]	$I_{COM(on)}$	V+ = 3.3 V, V_{NO}, V_{NC} = V_{COM} = 0.3 V/3.0 V	Room Full	-1 -10		1 10	
Digital Control							
Input High Voltage[d]	V_{INH}		Full	1.6			V
Input Low Voltage	V_{INL}		Full			0.4	
Input Capacitance[d]	C_{in}		Full		4		pF
Input Current	I_{INL} or I_{INH}	V_{IN} = 0 or V+	Full	-1		1	μA

SPECIFICATIONS (V+ = 3.0 V)

Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 3 V, ±10%, V_{IN} = 0.4 or 2.0 V[e]	Temp[a]	Limits -40 to 85°C Min[b]	Typ[c]	Max[b]	Unit
Dynamic Characteristics							
Turn-On Time[d]	t_{ON}	V_{NO} or V_{NC} = 2.0 V, R_L = 300 Ω, C_L = 35 pF Figure 1 and 2	Room Full		19	51 52	ns
Turn-Off Time[d]	t_{OFF}		Room Full		17	36 37	
Break-Before-Make Time Delay	t_D	V_{NO} or V_{NC} = 2.0 V, R_L - 300 Ω, C_L - 35 pF (DG2043 Only)	Room	2			
Charge Injection[d]	Q_{INJ}	C_L = 1 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω, Figure 2	Room		3		pC
Off-Isolation[d]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room		-63		dB
Crosstalk[d]	X_{TALK}		Room		-94		
NO, NC Off Capacitance[d]	$C_{NO(off)}$, $C_{NC(off)}$	V_{IN} = 0 or V+, f = 1 MHz	Room		25		pF
Channel-On Capacitance[d]	C_{ON}		Room		49		
Power Supply							
Power Supply Current	I+	V_{IN} = 0 or V+			0.001	1.0	µA

SPECIFICATIONS (V+ = 5.0 V)

Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 5 V, ±10%, V_{IN} = 0.8 or 2.4 V[e]	Temp[a]	Limits -40 to 85°C Min[b]	Typ[c]	Max[b]	Unit
Analog Switch							
Analog Signal Range[d]	V_{NO}, V_{NC}, V_{COM}		Full	0		V+	V
On-Resistance	r_{ON}	V+ = 4.5 V, V_{COM} = 0.7 V/2.5 V, I_{NO}, I_{NC} = 10 mA	Room Full		1.0	1.5 1.6	Ω
r_{ON} Flatness[d]	r_{ON} Flatness	V+ = 4.5 V, V_{COM} = 0 to V+, I_{NO}, I_{NC} = 10 mA	Room			0.7	
r_{ON} Match Between Channels	Δ r_{ON}		Room			0.3	
Switch Off Leakage Current	$I_{NO(off)}$, $I_{NC(off)}$	V+ = 5.5 V V_{NO}, V_{NC} = 1 V/4.5 V, V_{COM} = 4.5 V/1 V	Room Full	-1.0 -10		1.0 10	nA
	$I_{COM(off)}$		Room Full	-1.0 -10		1.0 10	
Channel-On Leakage Current	$I_{COM(on)}$	V+ = 5.5 V, V_{NO}, V_{NC} = V_{COM} = 1 V/4.5 V	Room Full	-1.0 -10		1.0 10	
Digital Control							
Input High Voltage	V_{INH}		Full	2.4			V
Input Low Voltage	V_{INL}		Full			0.8	
Input Capacitance	C_{in}		Full		4		pF
Input Current	I_{INL} or I_{INH}	V_{IN} = 0 or V+	Full	-1		1	µA

SPECIFICATIONS (V+ = 5.0 V)

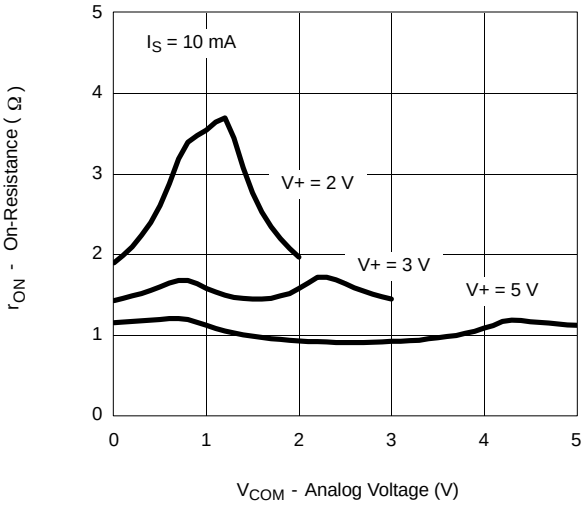
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 5 V, ±10%, V_{IN} = 0.8 or 2.4 V[e]	Temp[a]	Limits -40 to 85°C Min[b]	Typ[c]	Max[b]	Unit
Dynamic Characteristics							
Turn-On Time[d]	t_{ON}	V_{NO} or V_{NC} = 3 V, R_L = 300 Ω, C_L = 35 pF Figure 1 and 2	Room Full		13	42 43	ns
Turn-Off Time[d]	t_{OFF}		Room Full		19	32 33	
Break-Before-Make Time Delay	t_D	V_{NO} or V_{NC} = 3 V, R_L - 300 Ω, C_L - 35 pF (DG2043 Only)	Room	1			
Charge Injection[d]	Q_{INJ}	C_L = 1 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω, Figure 2	Room		3		pC
Off-Isolation[d]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room		-63		dB
Crosstalk[d]	X_{TALK}		Room		-93		
Source-Off Capacitance[d]	$C_{NO(off)}$, $C_{NC(off)}$	V_{IN} = 0 or V+, f = 1 MHz	Room		26		pF
Channel-On Capacitance[d]	C_{ON}		Room		49		
Power Supply							
Power Supply Current	I+	V_{IN} = 0 or V+			0.001	1.0	µA

Notes:

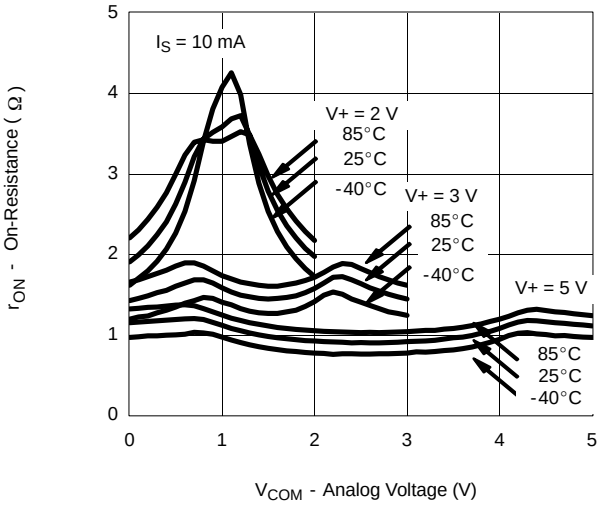
a. Room = 25°C, Full = as determined by the operating suffix.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Typical values are for design aid only, not guaranteed nor subject to production testing.
d. Guarantee by design, nor subjected to production test.
e. V_{IN} = input voltage to perform proper function.
f. Guaranteed by 5-V leakage testing, not production tested.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

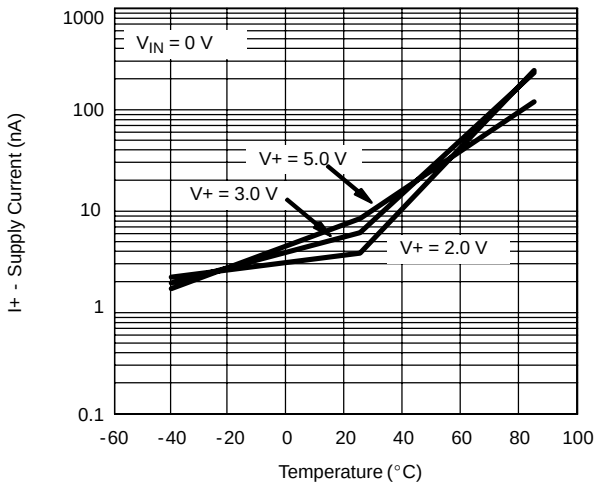
r_{ON} vs. V_{COM} Supply Voltage



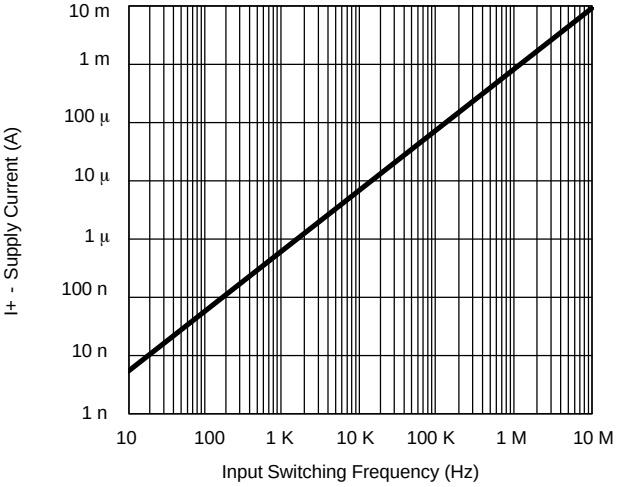
r_{ON} vs. Analog Voltage and Temperature



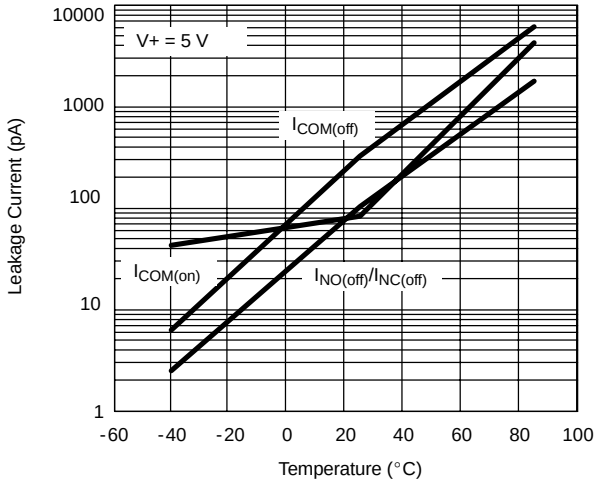
Supply Current vs. Temperature



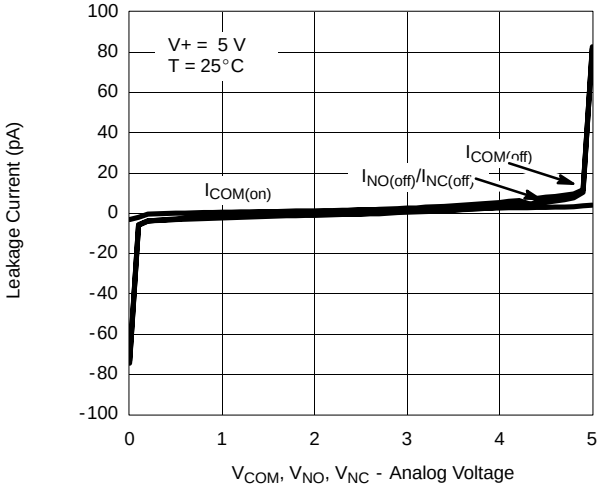
Supply Current vs. Input Switching Frequency



Leakage Current vs. Temperature

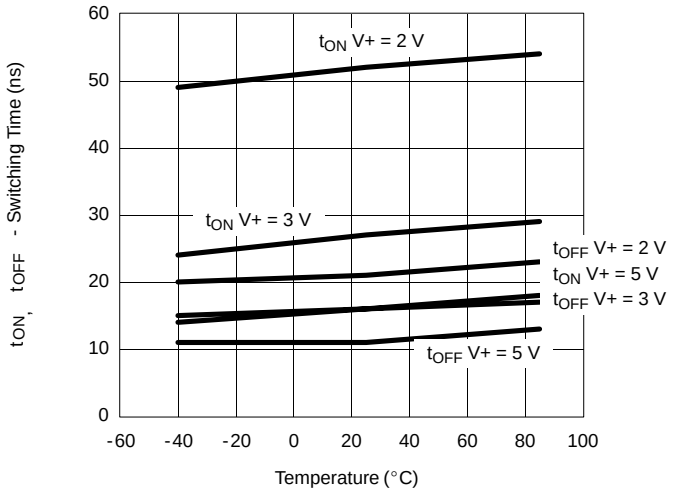


Leakage vs. Analog Voltage

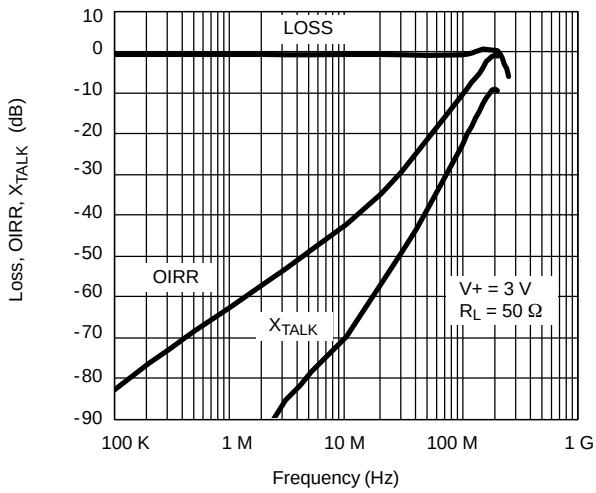


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

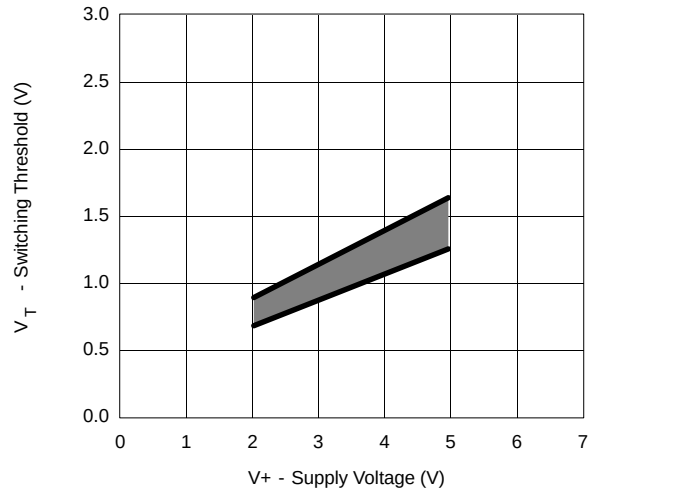
Switching Time vs. Temperature and Supply Voltage



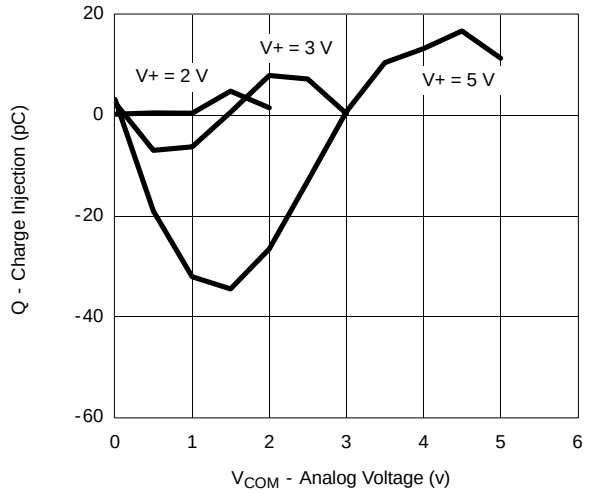
Insertion Loss, Off-Isolation, Crosstalk vs. Frequency



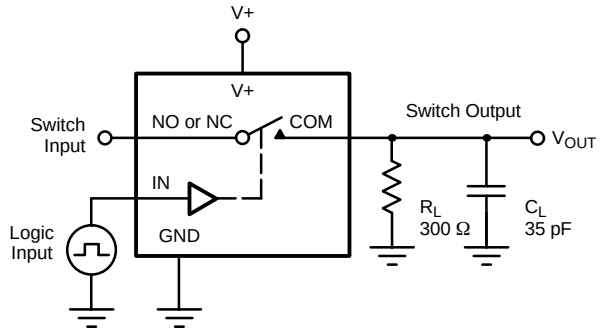
Switching Threshold vs. Supply Voltage



Charge Injection vs. Analog Voltage

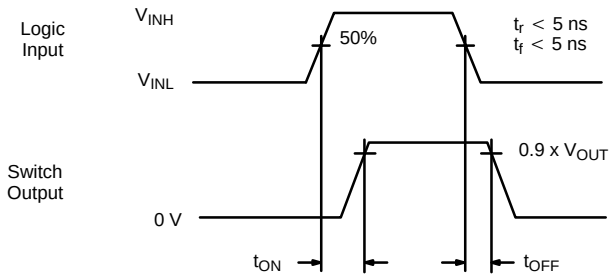


TEST CIRCUITS



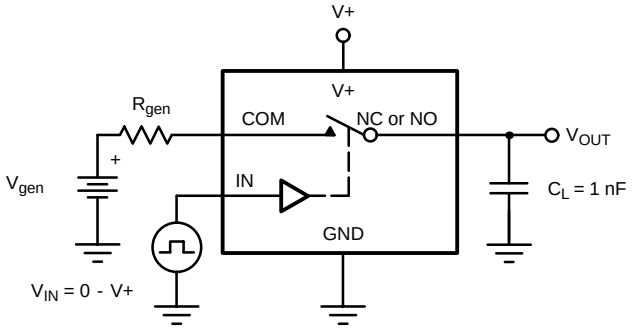
C_L (includes fixture and stray capacitance)

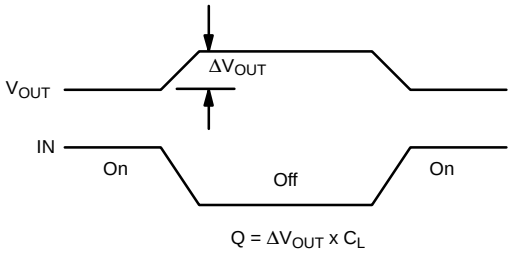
$$V_{OUT} = V_{COM}\left(\frac{R_L}{R_L + R_{ON}}\right)$$



Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

FIGURE 1. Switching Time

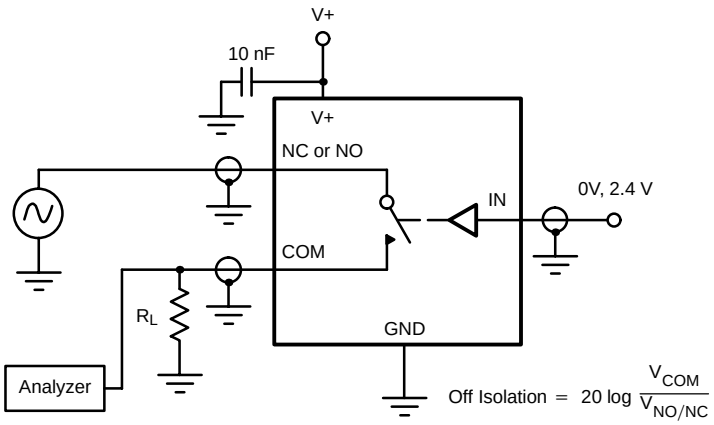




$Q = \Delta V_{OUT} \times C_L$

IN depends on switch configuration: input polarity determined by sense of switch.

FIGURE 2. Charge Injection



Off Isolation = 20 log $\frac{V_{COM}}{V_{NO/NC}}$

FIGURE 3. Off-Isolation

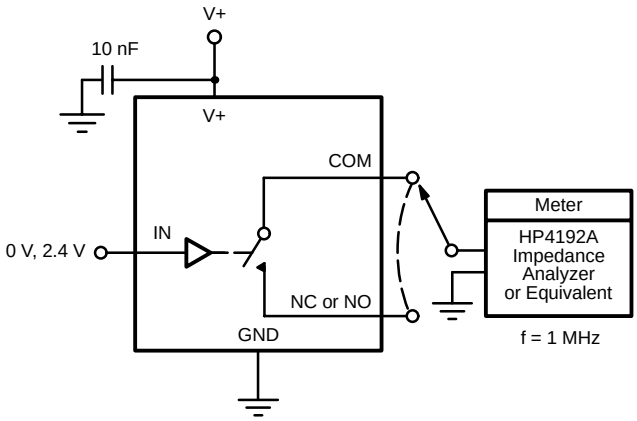


FIGURE 4. Channel Off/On Capacitance