



## 0.35- $\Omega$ Low-Voltage Dual SPDT Analog Switch

### FEATURES

- Low Voltage Operation
- Low On-Resistance -  $r_{ON}$ : 0.35  $\Omega$  @ 2.7 V
- -69 dB OIRR @ 2.7 V, 100 kHz
- MSOP-10 and DFN-10 Packages
- ESD Protection >2000 V
- Latch-Up Current >300 mA (JESD 78)

### BENEFITS

- Reduced Power Consumption
- High Accuracy
- Reduce Board Space
- 1.8-V Logic Compatible
- High Bandwidth

### APPLICATIONS

- Cellular Phones
- Speaker Headset Switching
- Audio and Video Signal Routing
- PCMCIA Cards
- Battery Operated Systems
- Relay Replacement

### DESCRIPTION

The DG2535/DG2536 is a sub 1- $\Omega$  (0.35  $\Omega$  @ 2.7 V) dual SPDT analog switches designed for low voltage applications.

The DG2535/DG2536 has on-resistance matching (less than 0.05  $\Omega$  @ 2.7 V) and flatness (less than 0.2  $\Omega$  @ 2.7 V) that are guaranteed over the entire voltage range. Additionally, low logic thresholds make the DG2535/DG2536 an ideal interface to low voltage DSP control signals.

The DG2535/DG2536 has fast switching speed with break-before-make guaranteed. In the On condition, all switching elements conduct equally in both directions. Off-isolation and crosstalk is -69 dB @ 100 kHz.

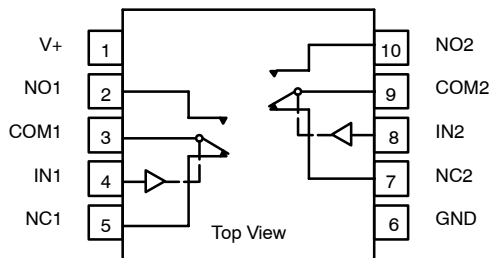
The DG2535/DG2536 is built on Vishay Siliconix's high-density low voltage CMOS process. An epitaxial layer is

built in to prevent latchup. The DG2535/DG2536 contains the additional benefit of 2,000-V ESD protection.

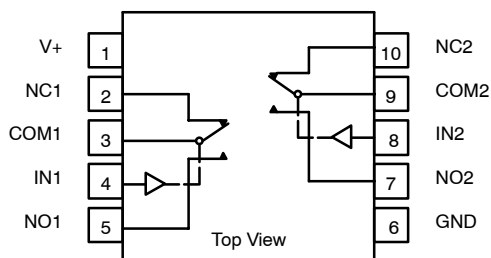
In space saving MSOP-10 and DFN-10 lead (Pb)-free packages, the DG2535/DG2536 are high performance, low  $r_{ON}$  switches for battery powered applications. No lead (Pb) is used in the manufacturing process either inside the device/package or on the external terminations. As a committed partner to the community and the environment, Vishay Siliconix manufactures this product with the lead (Pb)-free device terminations. For analog switching products manufactured in DFN packages, the lead (Pb)-free "-E3/E4" suffix is being used as a designator. Lead (Pb)-free DFN products purchased at any time will have either a nickel-palladium-gold device termination or a 100% matte tin device termination. The different lead (Pb)-free materials are interchangeable and meet all JEDEC standards for reflow and MSL rating.

### FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG2535



DG2536



TRUTH TABLE

Logic	NC1 and NC2	NO1 and NO2
0	ON	OFF
1	OFF	ON

ORDERING INFORMATION

Temp Range	Package	Part Number
-40 to 85°C	MSOP-10	DG2535DQ-T1—E3 DG2536DQ-T1—E3
	DFN-10	DG2535DN-T1—E3/E4 DG2536DN-T1—E3/E4

**ABSOLUTE MAXIMUM RATINGS**

Reference to GND

V+	.....	-0.3 to +6 V
IN, COM, NC, NO <sup>a</sup>	.....	-0.3 to (V+ + 0.3 V)
Continuous Current (NO, NC, COM)	.....	±300 mA
Peak Current	.....	±500 mA
(Pulsed at 1 ms, 10% duty cycle)		
Storage Temperature (D Suffix)	.....	-65 to 150°C
ESD per Method 3015.7	.....	>2 kV

Power Dissipation (Packages)<sup>b</sup>

MSOP-10 <sup>c</sup>	.....	320 mW
DFN-10 <sup>d</sup>	.....	1191 mW

Notes:

- Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads welded or soldered to PC Board.
- Derate 4.0 mW/°C above 70°C
- Derate 14.9 mW/°C above 70°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

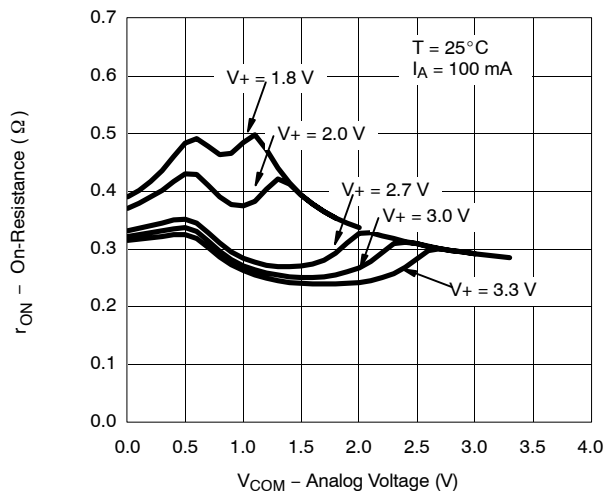
SPECIFICATIONS (V+ = 3 V)							
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 3 V, ±10%, VIN = 0.5 or 1.4 V <sup>e</sup>	Temp <sup>a</sup>	Limits −40 to 85°C			Unit
				Min <sup>b</sup>	Typ <sup>c</sup>	Max <sup>b</sup>	
Analog Switch							
Analog Signal Range <sup>d</sup>	VNO, VNC, VCOM		Full	0		V+	V
On-Resistance	rON	V+ = 2.7 V, VCOM = 0.6/1.5 V INO, INC = 100 mA	Room Full		0.35	0.5 0.6	Ω
rON Flatness <sup>d</sup>	rON Flatness		Room		0.09	0.2	
On-Resistance Match Between Channels <sup>d</sup>	ΔrDS(on)		Room			0.05	
Switch Off Leakage Current	INO(off), INC(off)	V+ = 3.3 V, VNO, VNC = 0.3 V/3 V VCOM = 3 V/0.3 V	Room Full	−1 −10		1 10	nA
	ICOM(off)		Room Full	−1 −10		1 10	
Channel-On Leakage Current	ICOM(on)	V+ = 3.3 V, VNO, VNC = VCOM = 0.3 V/3 V	Room Full	−1 −10		1 10	
Digital Control							
Input High Voltage <sup>d</sup>	VINH		Full	1.4			V
Input Low Voltage	VINL		Full			0.5	
Input Capacitance	Cin		Full		10		pF
Input Current	IINL or IINH	VIN = 0 or V+	Full	1		1	μA
Dynamic Characteristics							
Turn-On Time	tON	VNO or VNC = 2.0 V, RL = 50 Ω, CL = 35 pF	Room Full		52	82 90	ns
Turn-Off Time	tOFF		Room Full		43	73 78	
Break-Before-Make Time	td	VNO or VNC = 2.0 V, RL = 50 Ω, CL = 35 pF	Full	1	6		
Charge Injection <sup>d</sup>	QINJ	CL = 1 nF, VGEN = 1.5 V, RGEN = 0 Ω	Room		21		pC
Off-Isolation <sup>d</sup>	OIRR	RL = 50 Ω, CL = 5 pF, f = 100 KHz	Room		−69		dB
Crosstalk <sup>d</sup>	XTALK		Room		−69		
NO, NC Off Capacitance <sup>d</sup>	CNO(off)	VIN = 0 or V+, f = 1 MHz	Room		145		pF
	CNC(off)		Room		145		
Channel-On Capacitance <sup>d</sup>	CNO(on)		Room		406		
	CNC(on)		Room		406		
Power Supply							
Power Supply Current	I+	VIN = 0 or V+	Full			1.0	μA

Notes:

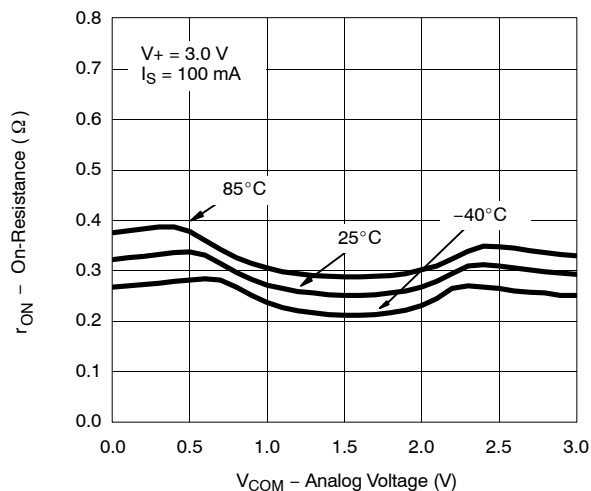
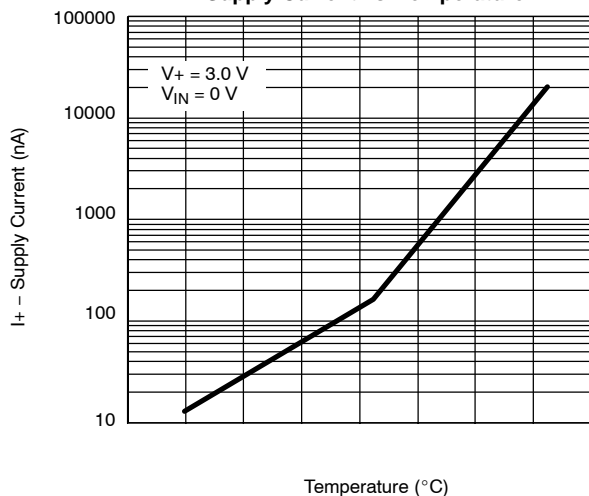
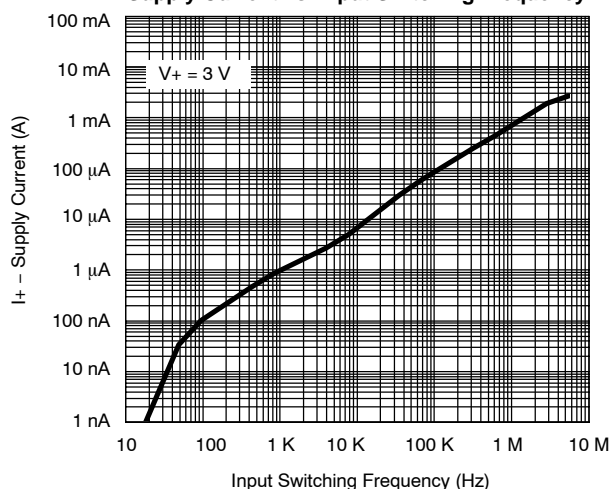
- Room = 25°C, Full = as determined by the operating suffix.
- Typical values are for design aid only, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guarantee by design, nor subjected to production test.
- V<sub>IN</sub> = input voltage to perform proper function.

### TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

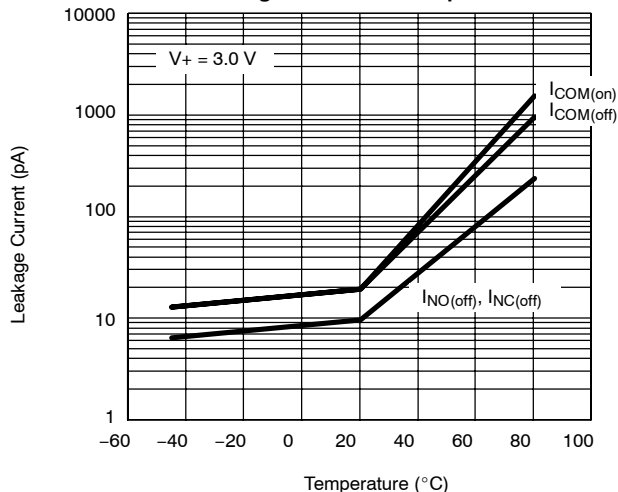
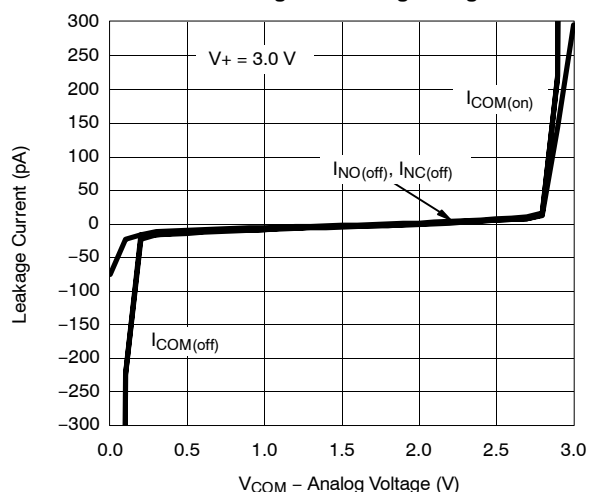
### $r_{ON}$ vs. $V_{COM}$ and Supply Voltage

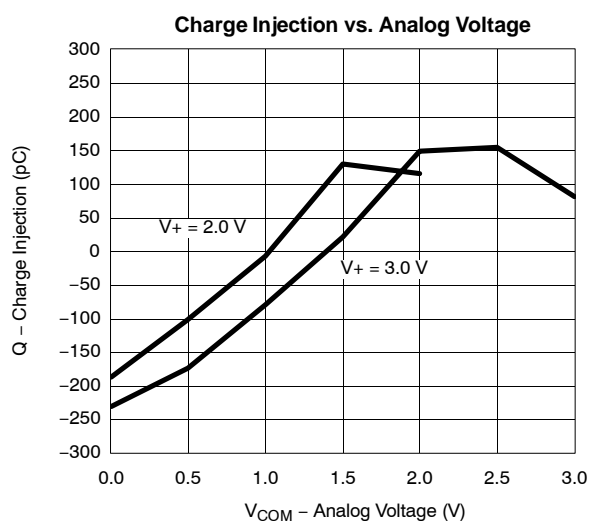
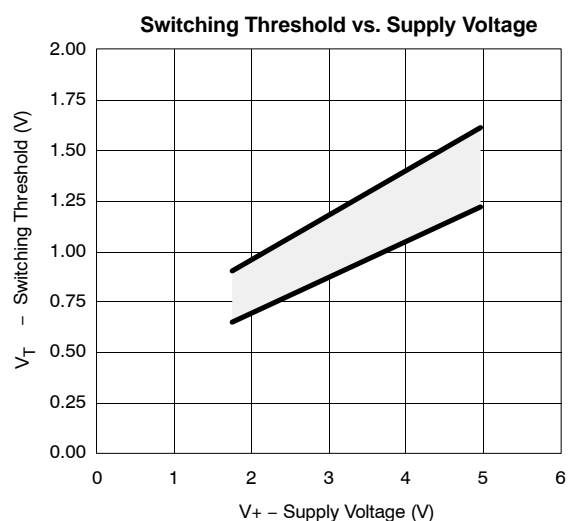
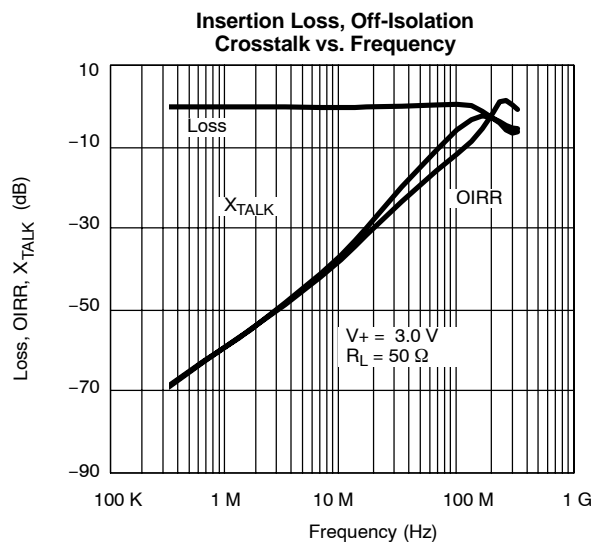
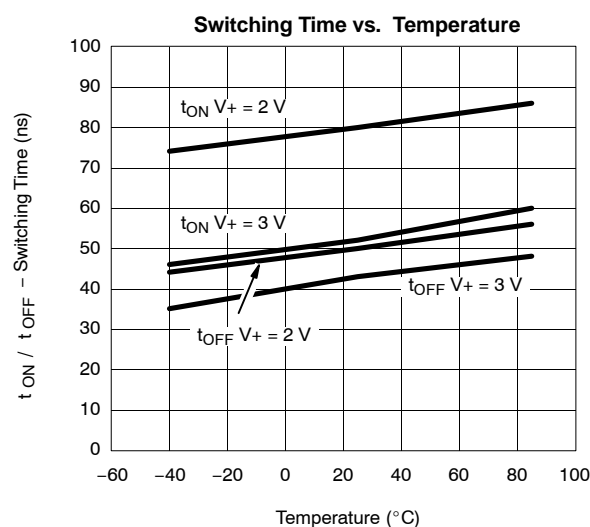


### r<sub>ON</sub> vs. Analog Voltage and Temperature (NC1)

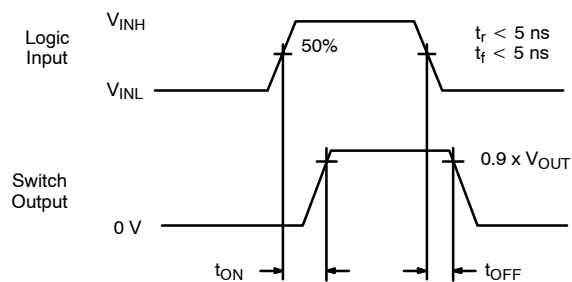
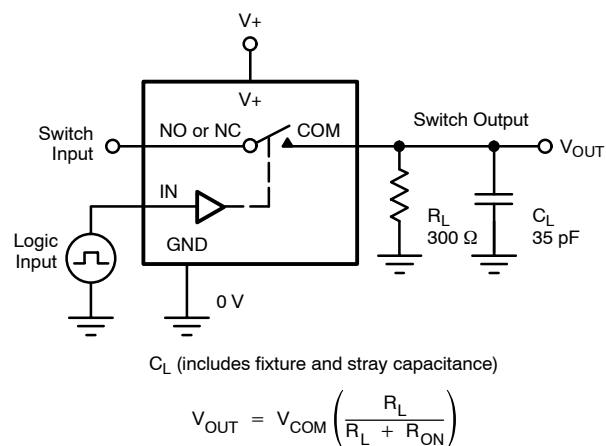
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### Leakage Current vs. Temperature

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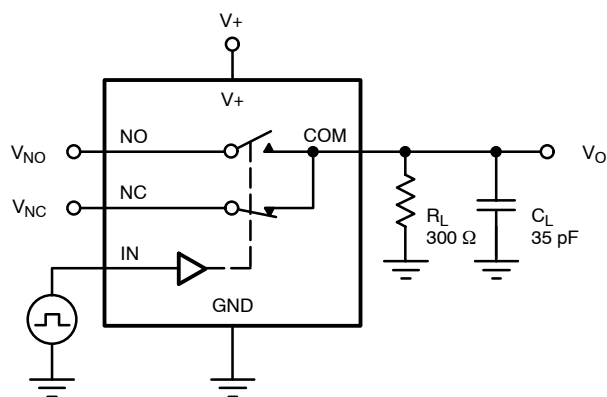
## TEST CIRCUITS



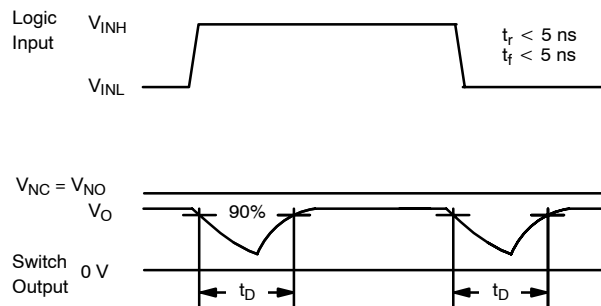
Logic "1" = Switch On  
Logic input waveforms inverted for switches that have the opposite logic sense.

**FIGURE 1. Switching Time**

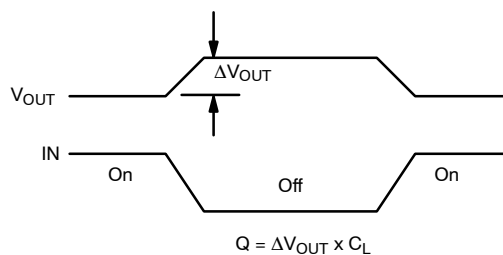
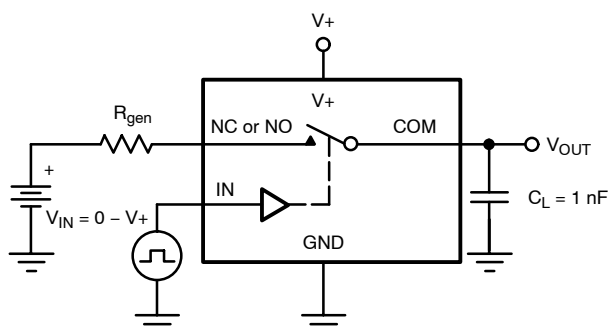
## TEST CIRCUITS



$C_l$  (includes fixture and stray capacitance)

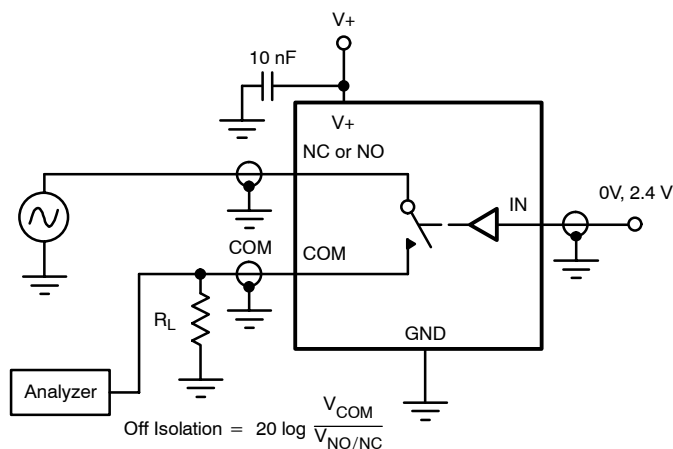


**FIGURE 2.** Break-Before-Make Interval

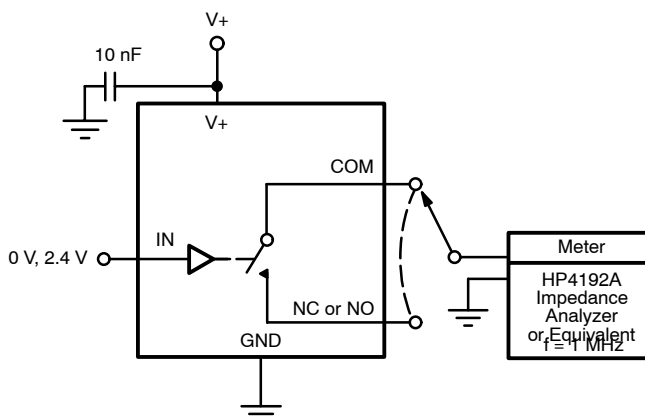


IN depends on switch configuration: input polarity determined by sense of switch.

**FIGURE 3.** Charge Injection



**FIGURE 4. Off-Isolation**



**FIGURE 5.** Channel Off/On Capacitance

*Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?72939>.*