



## High-Speed, Low $r_{ON}$ , SPDT Analog Switch (2:1 Multiplexer/Demultiplexer Bus Switch)

### FEATURES

- Direct Cross to Industry Standard *SN74LVC1G3157*, *NC7SB3157*, *NLASB3175*, *PI5A3157*, and *STG3157*
- SC-70 6-Lead Package
- 1.65-V to 5.5-V  $V_{CC}$  Operation
- 5- $\Omega$  Connection Between Ports
- Minimal Propagation Delay
- Break-Before-Make Switching
- Zero Bounce In Flow-Through Mode

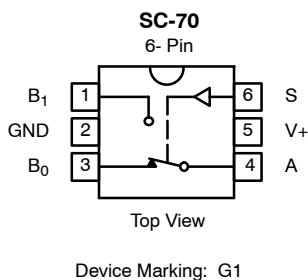
### DESCRIPTION

The DG3157 is a high-speed single-pole double-throw, low power, TTL-Compatible bus switch. Using sub-micro CMOS technology, the DG3157 achieves low on-resistance and negligible propagation delay.

The DG3157 can handle both analog and digital signals and permits signals with amplitudes of up to  $V_{CC}$  to be transmitted in either direction.

When the Select pin is low,  $B_0$  is connected to the output A pin. When the Select pin is high,  $B_1$  is connected to the output A pin. The path that is open will have a high-impedance state with respect to the output. Make-before-break is guaranteed. An epitaxial layer prevents latch-up.

### FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



#### TRUTH TABLE

Logic Input (S)	Function
0	$B_0$ Connected to A
1	$B_1$ Connected to A

#### ORDERING INFORMATION

Temp Range	Package	Part Number
-40 to 85°C	SC70-6	DG3157DL



## ABSOLUTE MAXIMUM RATINGS

Reference to GND

V+	.....	-0.3 to +6 V
S, A, B <sup>a</sup>	.....	-0.3 to (V+ + 0.3 V)
Continuous Current (Any terminal)	.....	± 50 mA
Peak Current (Pulsed at 1 ms, 10% duty cycle)	.....	± 200 mA
Storage Temperature (D Suffix)	.....	-65 to 150°C

Power Dissipation (Packages)<sup>b</sup>

6-Pin SC70 <sup>c</sup>	.....	250 mW
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Notes:

- Signals on A, or B or S exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads welded or soldered to PC Board.
- Derate 3.1 mW/°C above 70°C

SPECIFICATIONS								
Parameter	Symbol	Test Conditions Otherwise Unless Specified  V+ = 3.0 V, V <sub>S</sub> = 0.25 V to 0.7 V+ <sup>e</sup>		Temp <sup>a</sup>	Limits −40 to 85 °C			Unit
					Min <sup>b</sup>	Typ <sup>c</sup>	Max <sup>b</sup>	
DC Characteristics								
High Level Input Voltage	V <sub>SH</sub>	V+ = 1.65 to 1.95 V		Full	0.75 V+			V
		V+ = 2.3 to 5.5 V		Full	0.7 V+			
Low Level Input Voltage	V <sub>SL</sub>	V+ = 1.65 to 1.95 V		Full			0.25 V+	V
		V+ = 2.3 to 5.5 V		Full			0.3 V+	
On Resistance	R <sub>ON</sub>	V+ = 4.5 V	V <sub>BN</sub> = 0 V, I <sub>A</sub> = 30 mA	Full		6	7	Ω
			V <sub>BN</sub> = 2.3 V, I <sub>A</sub> = −30 mA	Full		6	12	
			V <sub>BN</sub> = 4.5 V, I <sub>A</sub> = −30 mA	Full		9	15	
		V+ = 3.0 V	V <sub>BN</sub> = 0 V, I <sub>A</sub> = 24 mA	Full		8	9	
			V <sub>BN</sub> = 3.0 V, I <sub>A</sub> = −24 mA	Full		12	20	
		V+ = 2.3 V	V <sub>BN</sub> = 0 V, I <sub>A</sub> = 8 mA	Full		9	12	
			V <sub>BN</sub> = 2.3 V, I <sub>A</sub> = −8 mA	Full		13	30	
		V+ = 1.65 V	V <sub>BN</sub> = 0 V, I <sub>A</sub> = 4 mA	Full		12	20	
V <sub>BN</sub> = 1.8 V, I <sub>A</sub> = −4 mA	Full			18	50			
On Resistance Ftness	R <sub>FLAT</sub>	0 < V <sub>BN</sub> < V+	V+ = 4.5 V, I <sub>A</sub> = −30 mA	Room		6		Ω
			V+ = 3.0 V, I <sub>A</sub> = −24 mA	Room		12		
			V+ = 2.3 V, I <sub>Z</sub> = −8 mA	Room		22		
			V+ = 1.65 V, I <sub>A</sub> = −4 mA	Room		90		
On Resistance Matching Between Channels	ΔR <sub>ON</sub>	V+ = 4.5 V, V <sub>BN</sub> = 3.15 V, I <sub>A</sub> = −30 mA		Room		0.32		Ω
		V+ = 3.0 V, V <sub>BN</sub> = 2.1 V, I <sub>A</sub> = −24 mA		Room		0.31		
		V+ = 2.3 V, V <sub>BN</sub> = 1.6 V, I <sub>A</sub> = −8 mA		Room		0.30		
		V+ = 1.65 V, V <sub>BN</sub> = 1.15 V, I <sub>A</sub> = −4 mA		Room		0.29		
Input Leakage Current	I <sub>S</sub>	V+ = 5.5 V, V <sub>A</sub> = 5.5 V		Room Full	−0.1 −1.0		0.1 −1.0	μA
Off Stage Switch Leakage	I <sub>BN(off)</sub>	V+ = 5.5 V, V <sub>A</sub> /V <sub>B</sub> = 0 V/5.5 V		Room Full	−0.1 −1.0		0.1 −1.0	
On State Switch Leakage	I <sub>BN(on)</sub>	V+ = 5.5 V, V <sub>A</sub> /V <sub>B</sub> = 0 V/5.5 V		Room Full	−0.1 −1.0		0.1 −1.0	
Power Supply								
Power Supply Range	V+			Full	1.8		5.5	
Quiescent Supply Current	I+	V+ = 5.5 V, V <sub>A</sub> = V <sub>B</sub> = V+ or GND		Room Full			1 10	μA



SPECIFICATIONS								
Parameter	Symbol	Test Conditions Otherwise Unless Specified  V <sub>+</sub> = 3.0 V, V <sub>S</sub> = 0.25 V to 0.7 V <sub>+</sub> <sup>e</sup>		Temp <sup>a</sup>	Limits –40 to 85°C			Unit
					Min <sup>b</sup>	Typ <sup>c</sup>	Max <sup>b</sup>	
AC Electrical Characteristice								
Prop Delay Time <sup>f</sup>	t <sub>PHL</sub> /t <sub>PLH</sub>	V <sub>A</sub> = 0 V	V <sub>+</sub> =1.65 to 1.95 V	Full				ns
			V <sub>+</sub> =2.3 to 2.7 V	Full		1.2		
			V <sub>+</sub> =3.0 to 3.6 V	Full		0.8		
			V <sub>+</sub> =4.5 to 5.5 V	Full		0.3		
Output Enable Time <sup>f</sup>	t <sub>PZL</sub> /t <sub>PZH</sub>	V <sub>LOAD</sub> = 2 x V <sub>+</sub> for t <sub>PZL</sub> V <sub>LOAD</sub> = 0 V for t <sub>PZH</sub>	V <sub>+</sub> =1.65 to 1.95 V	Room Full		10.2 10.4		
			V <sub>+</sub> =2.3 to 2.7 V	Room Full		5.9 6.2		
			V <sub>+</sub> =3.0 to 3.6 V	Room Full		4.1 4.5		
			V <sub>+</sub> =4.5 to 5.5 V	Room Full		2.6 2.9		
Output Disable Time <sup>f</sup>	t <sub>PLZ</sub> /t <sub>PHZ</sub>	V <sub>LOAD</sub> = 2 x V <sub>+</sub> for t <sub>PLZ</sub> V <sub>LOAD</sub> = 0 V for t <sub>PHZ</sub>	V <sub>+</sub> =1.65 to 1.95 V	Room Full		10.2 10.4		
			V <sub>+</sub> =2.3 to 2.7 V	Room Full		5.9 6.2		
			V <sub>+</sub> =3.0 to 3.6 V	Room Full		4.1 4.5		
			V <sub>+</sub> =4.5 to 5.5 V	Room Full		2.6 2.9		
Break-Before-Make Time <sup>d</sup>	t <sub>BBM</sub>	V <sub>+</sub> =1.65 to 1.95 V		Full	0.5			
		V <sub>+</sub> =2.3 to 2.7 V		Full	0.5			
		V <sub>+</sub> =3.0 to 3.65 V		Full	0.5			
		V <sub>+</sub> =4.5 to 5.5 V		Full	0.5			
Charge Injection <sup>d</sup>	Q	C <sub>L</sub> = 0.1 nF, V <sub>GEN</sub> = 0 V R <sub>GEN</sub> = 0 Ω	V <sub>+</sub> = 5 V	Room		7		pC
			V <sub>+</sub> = 3.3 V	Room		3		
Analog Switch Characteristics								
Off Isolation <sup>d</sup>	OIRR	R <sub>L</sub> = 50 Ω, f = 10 MHz		Room		–57.6		dB
Crosstalk <sup>d</sup>	X <sub>TALK</sub>			Room		–58.7		
–3-db Bandwidth <sup>d</sup>	BW	R <sub>L</sub> = 50 Ω		Room		> 250		MHz
Capacitance								
Control Pin Capacitance <sup>d</sup>	C <sub>IN</sub>	V <sub>+</sub> = 0 V		Room		4.9		pF
B Port Off Capacitance <sup>d</sup>	C <sub>IO-B</sub>	V <sub>+</sub> = 5 V		Room		< 6.5		
A Port Capacitance When Switch Enabled <sup>d</sup>	C <sub>IO-A(on)</sub>			Room		< 18.5		

## Notes:

- Room = 25°C, Full = as determined by the operating suffix.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Typical values are for design aid only, not guaranteed nor subject to production testing.
- Guarantee by design, nor subjected to production test.
- $V_{IN}$  = input voltage to perform proper function.
- Guaranteed by design and not production tested. The bus switch propagation delay is a function of the RC time constant contributed by the on-resistance and the specified load capacitance with an ideal voltage source (zero output impedance) driving the switch.

LOGIC DIAGRAM (POSITIVE LOGIC)

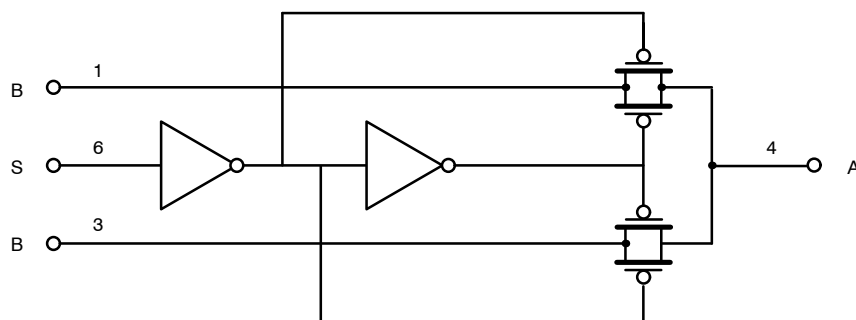
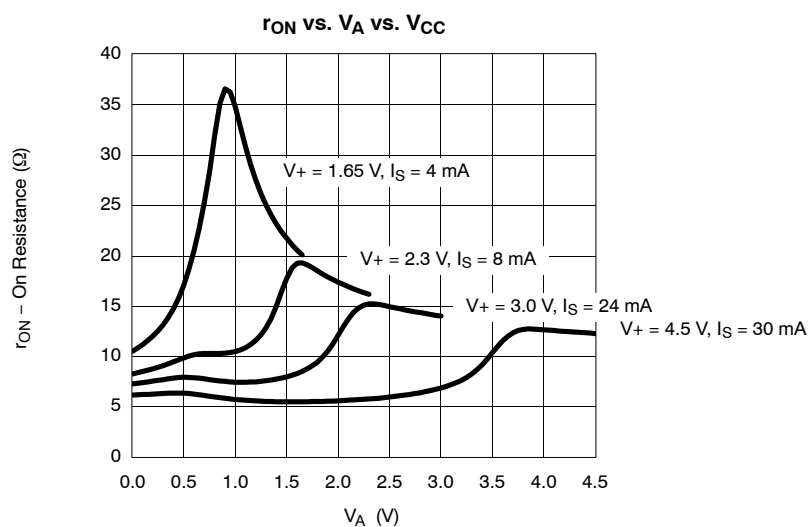


Figure 1.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



## AC LOADING AND WAVEFORMS

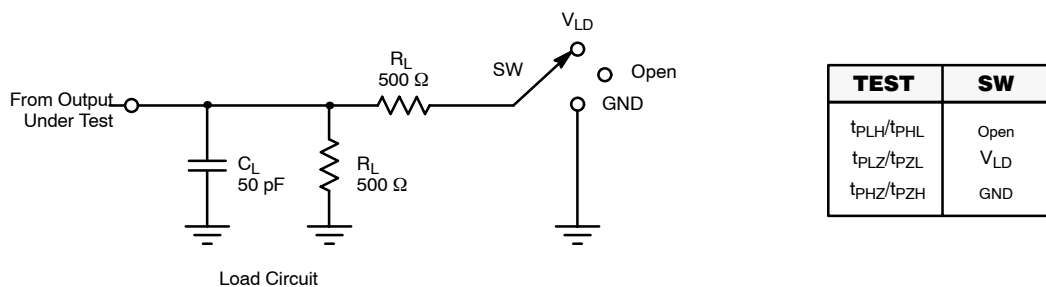


Figure 2. AC Test Circuit

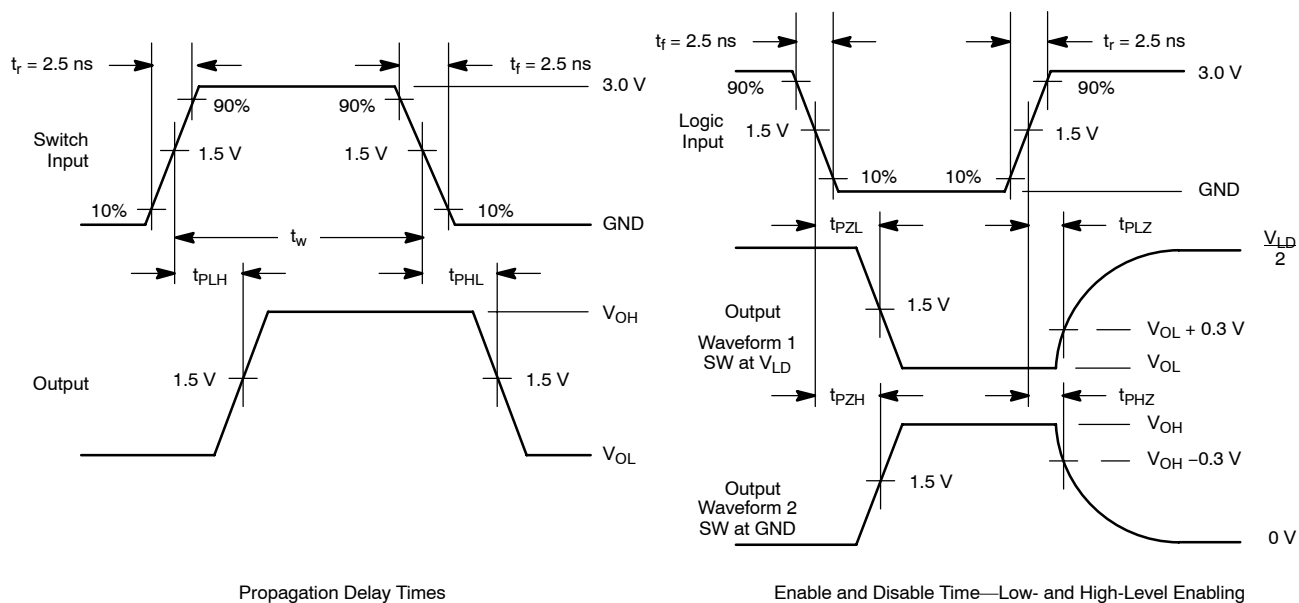
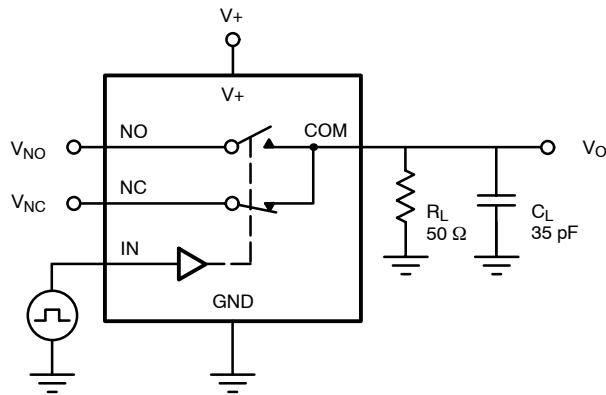


Figure 3. AC Waveforms

Notes:

- $C_L$  includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
- Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ .
- The outputs are measured one at a time with one transition per measurement.
- $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{dis}$ .
- $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{dis}$ .
- $V_{LD} = 2 \text{ V}+$ .

TEST CIRCUITS



$C_L$  (includes fixture and stray capacitance)

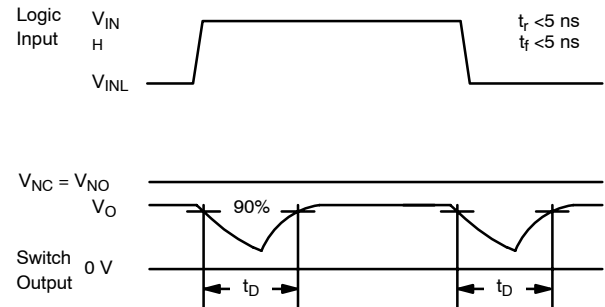
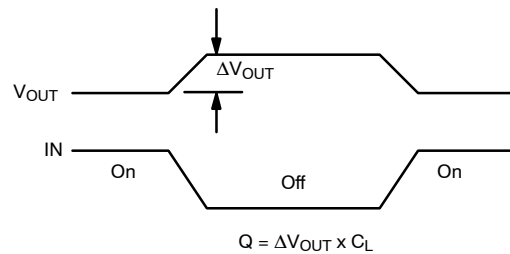
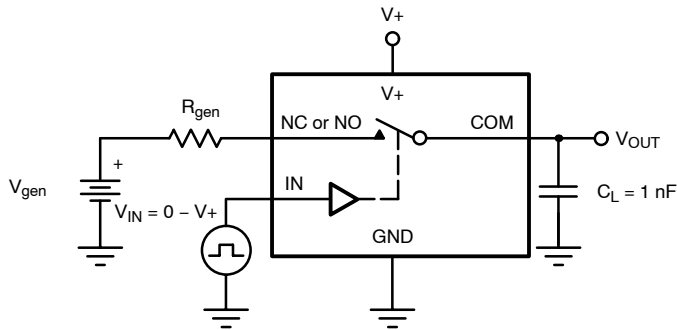


Figure 4. Break-Before-Make Interval



IN depends on switch configuration: input polarity determined by sense of switch.

Figure 5. Charge Injection

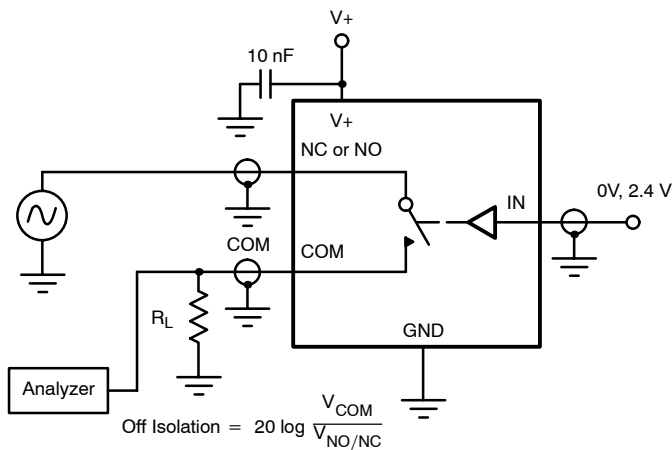


Figure 6. Off-Isolation

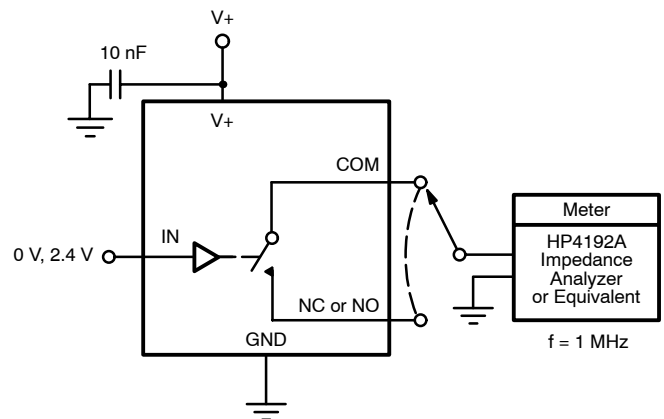


Figure 7. Channel Off/On Capacitance