Low-Voltage Single SPDT Analog Switch

FEATURES

- Low Voltage Operation (2.25 V to 5.5 V)
- Low On-Resistance - $r_{DS(on)}$: 7 Ω
- Fast Switching - t_{ON} : 9 ns, t_{OFF}: 5 ns
- Low Charge Injection - Q_{INJ}: 5 pC
- Low Power Consumption
- TTL/CMOS Compatible
- 6-Pin SC-70 Package

BENEFITS

- Reduced Power Consumption
- Simple Logic Interface
- High Accuracy
- Reduce Board Space

APPLICATIONS

- Cellular Phones
- Communication Systems
- Portable Test Equipment
- Battery Operated Systems
- Sample and Hold Circuits

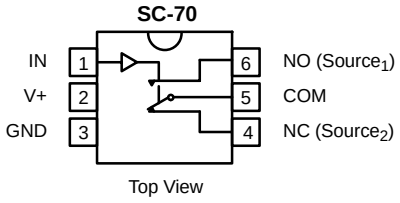
DESCRIPTION

The DG9411 is a single-pole/double-throw monolithic CMOS analog switch designed for high performance switching of analog signals. Combining low power, high speed (t_{ON}: 9 ns, t_{OFF}: 5 ns), low on-resistance ($r_{DS(on)}$: 7 Ω) and small physical size (SC70), the DG9411 is ideal for portable and battery powered applications requiring high performance and efficient use of board space.

The DG9411 is built on Vishay Siliconix's low voltage JI2 process. An epitaxial layer prevents latchup. Break-before -make is guaranteed for DG9411.

Each switch conducts equally well in both directions when on, and blocks up to the power supply level when off.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



Top View

TRUTH TABLE		
Logic	**NC**	**NO**
0	ON	OFF
1	OFF	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

ORDERING INFORMATION		
Temp Range	**Package**	**Part Number**
-40 to 85°C	SC70-6	DG9411DL

ABSOLUTE MAXIMUM RATINGS

Reference to GND
V+ ..... -0.3 to +6 V
IN, COM, NC, NO[a] ..... -0.3 to (V+ + 0.3 V)
Continuous Current (Any terminal) ..... ±50 mA
Peak Current ..... ±200 mA
(Pulsed at 1 ms, 10% duty cycle)
Storage Temperature (D Suffix) ..... -65 to 125°C

Power Dissipation (Packages)[b]
6-Pin SO70[c] ..... 250 mW

Notes:
a. Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 6.5 mW/°C above 25°C

SPECIFICATIONS (V+ = 2.5 V)

Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 2.5 V, ±10%, V_{IN} = 0.4 or 2.0 V[e]	Temp[a]	Limits –40 to 85°C Min[b]	Typ[c]	Max[b]	Unit
Analog Switch							
Analog Signal Range[d]	V_{NO}, V_{NC}, V_{COM}		Full	0		V+	V
Drain-Source On-Resistance	$r_{DS(on)}$	V+ = 2.25 V, V_D = 1.0 V, I_S = 10 mA	Room Full[d]		26 29	35 40	Ω
$r_{DS(on)}$ Flatness[d]	$r_{DS(on)}$ Flatness	V+ = 2.5 V	Room		10		Ω
Switch Off Leakage Current[f]	$I_{S(off)}$	V+ = 2.75 V V_S = 0.5 V/1.5 V, V_D = 1.5 V/0.5 V	Room Full[d]	–250 –3.0		250 3.0	pA nA
	$I_{D(off)}$		Room Full[d]	–250 –3.0		250 3.0	pA nA
Channel-On Leakage Current[f]	$I_{D(on)}$	V+ = 2.75 V, V_S = V_D = 0.5 V/1.5 V	Room Full[d]	–250 –3.0		250 3.0	pA nA
Digital Control							
Input High Voltage	V_{INH}		Full	2			V
Input Low Voltage	V_{INL}		Full			0.4	V
Input Capacitance[d]	C_{in}		Full		3		pF
Input Current	I_{INL} or I_{INH}	V_{IN} = 0 or V+	Full	–1		1	µA
Dynamic Characteristics							
Turn-On Time	t_{ON}	V_D or V_S = 1.5 V, R_L = 300 Ω, C_L = 35 pF Figures 1 and 2	Room Full[d]		16	40 45	ns
Turn-Off Time	t_{OFF}		Room Full[d]		7	23 28	ns
Break-Before-Make Time	t_d		Room	1	12		ns
Charge Injection[d]	Q_{INJ}	C_L = 1 nF, V_S = 0 V V_{GEN} = 0 V, R_{GEN} = 0 Ω, Figure 3	Room		5	10	pC
Off-Isolation[d]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room		–73		dB
Crosstalk[d]	X_{TALK}		Room		–70		dB
Source-Off Capacitance[d]	$C_{S(off)}$	V_{IN} = 0 or V+, f = 1 MHz	Room		7		pF
Channel-On Capacitance[d]	$C_{D(on)}$		Room		20		pF
Drain-to-Source Capacitance[d]	$C_{DS(off)}$		Room		20		pF
Power Supply							
Power Supply Range	V+			2.25		2.75	V
Power Supply Current[d]	I+	V_{IN} = 0 or V+			0.01	1.0	µA
Power Consumption	P_C					0.3	µW

SPECIFICATIONS (V+ = 3 V)

Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 3 V, ±10%, V_{IN} = 0.4 or 2.0 V[e]	Temp[a]	Limits –40 to 85°C Min[b]	Typ[c]	Max[b]	Unit
Analog Switch							
Analog Signal Range[d]	V_{NO}, V_{NC}, V_{COM}		Full	0		V+	V
Drain-Source On-Resistance[d]	$r_{DS(on)}$	V+ = 2.7 V, V_D = 1.5 V, I_S = 10 mA	Room Full		15 19	25 30	Ω
$r_{DS(on)}$ Flatness[d]	$r_{DS(on)}$ Flatness	V_S = 0 to V+, I_S = 10 mA	Room		7.5		Ω
Switch Off Leakage Current[f]	$I_{S(off)}$	V+ = 3.3 V, V_S = 1 V/3 V, V_D = 3 V/1 V	Room Full	–500 –4.0		500 4.0	pA nA
	$I_{D(off)}$		Room Full	–500 –4.0		500 4.0	pA nA
Channel-On Leakage Current[f]	$I_{D(on)}$	V+ = 3.3 V, V_S = V_D = 1 V/3 V	Room Full	–500 –4.0		500 4.0	pA nA
Digital Control							
Input High Voltage	V_{INH}		Full	2			V
Input Low Voltage	V_{INL}		Full			0.8	V
Input Capacitance[d]	C_{in}		Full		3		pF
Input Current	I_{INL} or I_{INH}	V_{IN} = 0 or V+	Full	–1		1	µA
Dynamic Characteristics							
Turn-On Time[d]	t_{ON}	V_D or V_S = 2.0 V, R_L = 300 Ω, C_L = 35 pF Figure 1 and 2	Room Full		12	15 20	ns
Turn-Off Time[d]	t_{OFF}		Room Full		6	8 10	ns
Break-Before-Make Time[d]	t_d		Room	1	7		ns
Charge Injection[d]	Q_{INJ}	C_L = 1 nF, V_{GEN} = 0 V, V_S = 0 V R_{GEN} = 0 Ω, Figure 3	Room		5	10	pC
Off-Isolation[d]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room		–73		dB
Crosstalk[d]	X_{TALK}		Room		–70		dB
Source-Off Capacitance[d]	$C_{S(off)}$	V_{IN} = 0 or V+, f = 1 MHz	Room		7		pF
Channel-On Capacitance[d]	$C_{D(on)}$		Room		20		pF
Drain-to-Source Capacitance[d]	$C_{DS(off)}$		Room		20		pF
Power Supply							
Power Supply Range	V+			2.7		3.3	V
Power Supply Current	I+	V_{IN} = 0 or V+			0.01	1.0	µA
Power Consumption	P_C					0.4	µW

SPECIFICATIONS (V+ = 5 V)

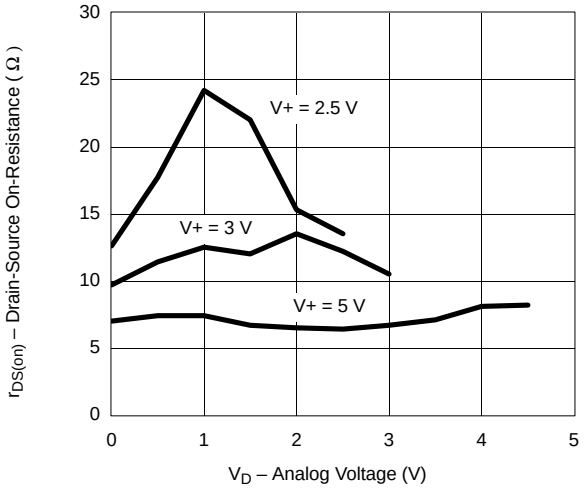
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 5 V, ±10%, V_{IN} = 0.8 or 2.4 V[e]	Temp[a]	Limits –40 to 85°C Min[b]	Typ[c]	Max[b]	Unit
Analog Switch							
Analog Signal Range[d]	V_{NO}, V_{NC}, V_{COM}		Full	0		V+	V
Drain-Source On-Resistance	$r_{DS(on)}$	V+ = 4.5 V, V_D = 3 V, I_S = 10 mA	Room Full		7 10	12 16	Ω
$r_{DS(on)}$ Flatness[d]	$r_{DS(on)}$ Flatness	V+ = 2.5 V	Room		2		Ω
Switch Off Leakage Current	$I_{S(off)}$	V+ = 5.5 V V_S = 1 V/4.5 V, V_D = 4.5 V/1 V	Room Full	–1.0 –4.0		1.0 4.0	nA
	$I_{D(off)}$		Room Full	–1.0 –4.0		1.0 4.0	nA
Channel-On Leakage Current	$I_{D(on)}$	V+ = 5.5 V, V_S = V_D = 1 V/4.5 V	Room Full	–1.0 –3.0		1.0 4.5	nA
Digital Control							
Input High Voltage	V_{INH}		Full	2.4			V
Input Low Voltage	V_{INL}		Full			0.8	V
Input Capacitance	C_{in}		Full		3		pF
Input Current	I_{INL} or I_{INH}	V_{IN} = 0 or V+	Full	–1		1	µA
Dynamic Characteristics							
Turn-On Time[d]	t_{ON}	V_D or V_S = 3 V, R_L = 300 Ω, C_L = 35 pF Figure 1 and 2	Room Full		9	11 15	ns
Turn-Off Time[d]	t_{OFF}		Room Full		5	7 9	ns
Break-Before-Make Time[d]	t_d		Room	1	4		ns
Charge Injection[d]	Q_{INJ}	C_L = 1 nF, V_S = 0 V V_{GEN} = 0 V, R_{GEN} = 0 Ω, Figure 3	Room		5	10	pC
Off-Isolation[d]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room		–73		dB
Crosstalk[d]	X_{TALK}		Room		–70		dB
Source-Off Capacitance[d]	$C_{S(off)}$	V_{IN} = 0 or V+, f = 1 MHz	Room		7		pF
Channel-On Capacitance[d]	$C_{D(on)}$		Room		20		pF
Drain-to-Source Capacitance[d]	$C_{DS(off)}$		Room		20		pF
Power Supply							
Power Supply Range	V+			4.5		5.5	V
Power Supply Current	I+	V_{IN} = 0 or V+			0.01	1.0	µA
Power Consumption	P_C					0.6	µW

Notes:

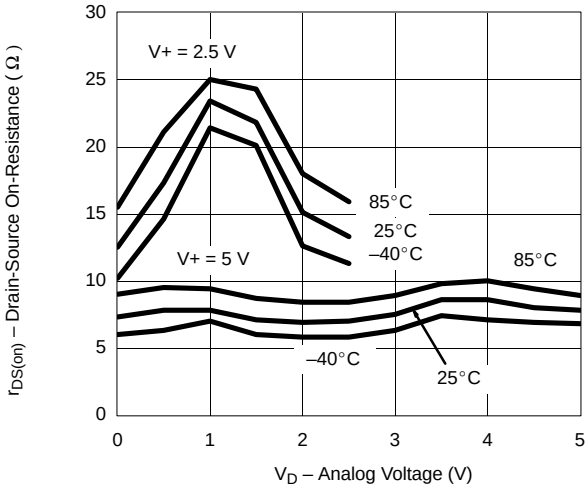
a. Room = 25°C, Full = as determined by the operating suffix.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Typical values are for design aid only, not guaranteed nor subject to production testing.
d. Guarantee by design, nor subjected to production test.
e. V_{IN} = input voltage to perform proper function.
f. Guaranteed by 5-V leakage testing, not production tested.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

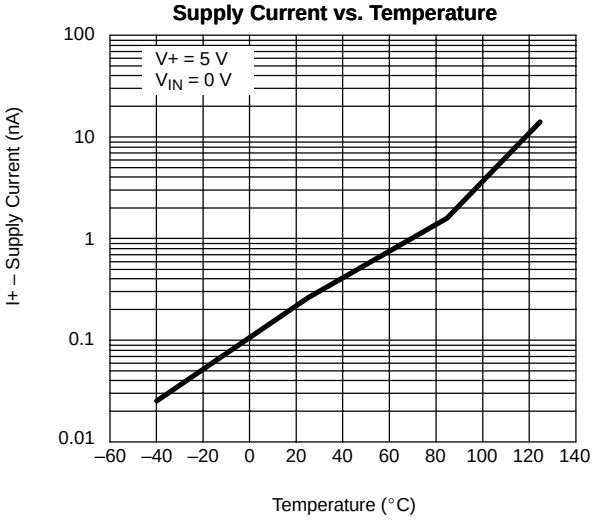
$r_{DS(on)}$ vs. Analog and Power Voltage



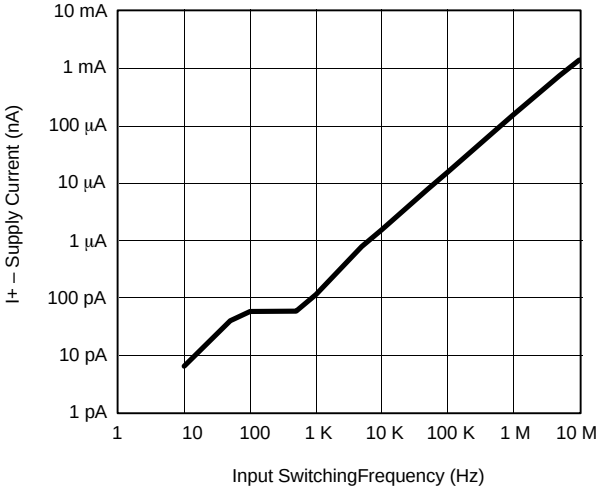
$r_{DS(on)}$ vs. Analog Voltage and Temperature



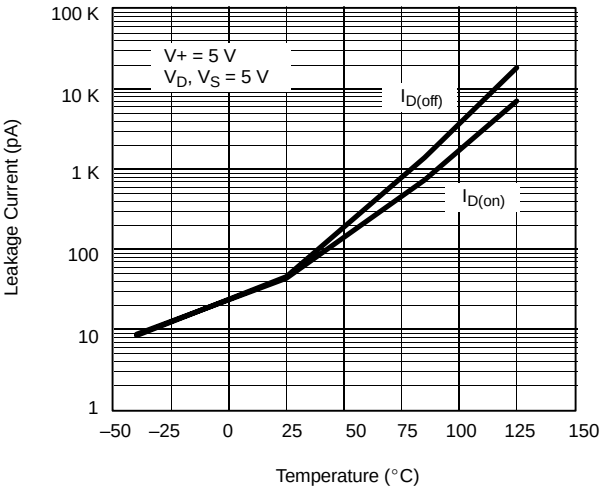
Supply Current vs. Temperature



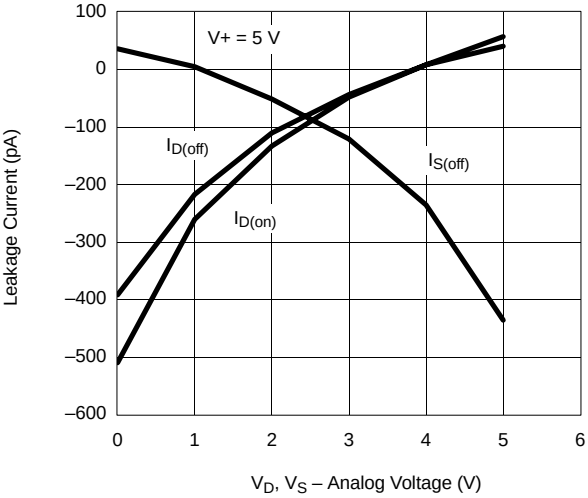
Supply Current vs. Input Switching Frequency



Leakage Current vs. Temperature

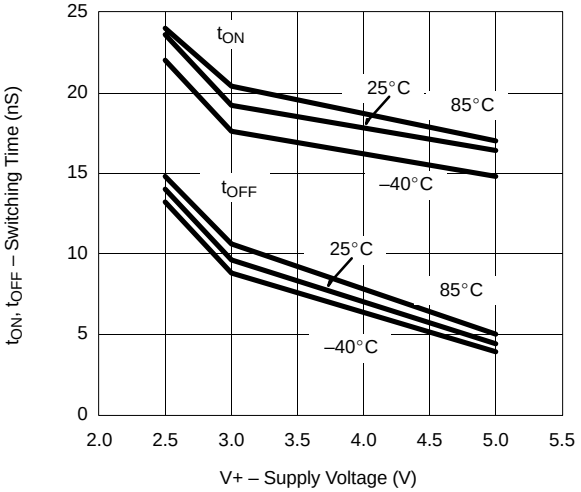


Leakage vs. Analog Voltage

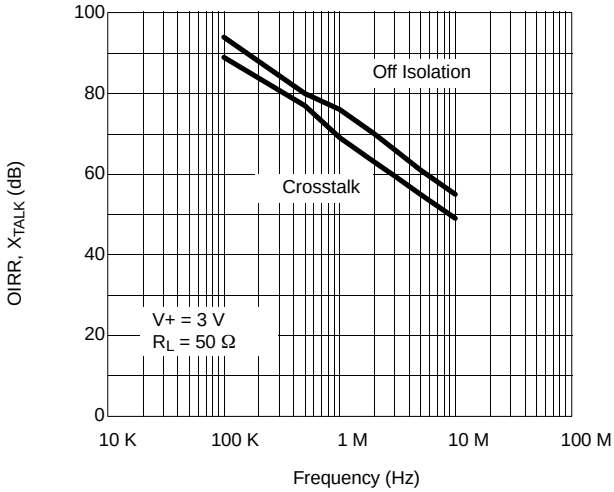


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

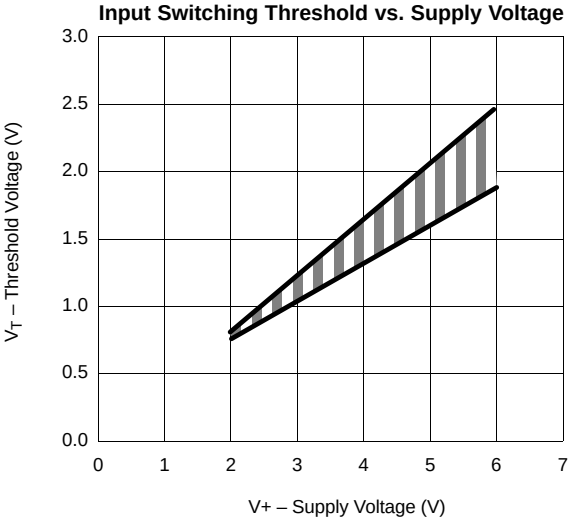
Switching Time vs. Temperature and Supply Voltage



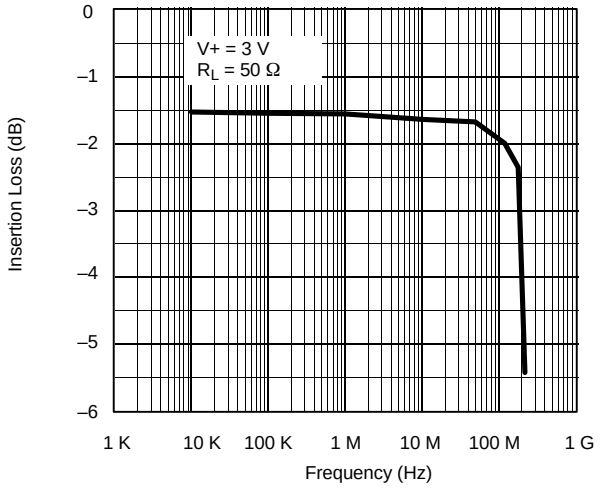
Crosstalk and Off Isolation vs. Frequency



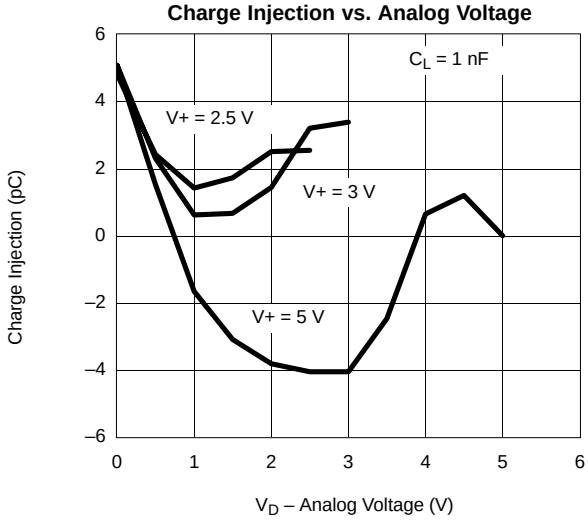
Input Switching Threshold vs. Supply Voltage



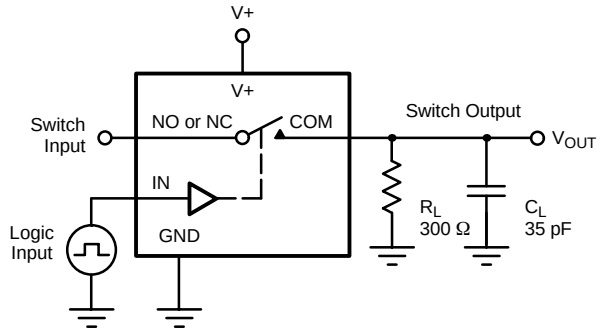
Insertion Loss vs. Frequency



Charge Injection vs. Analog Voltage

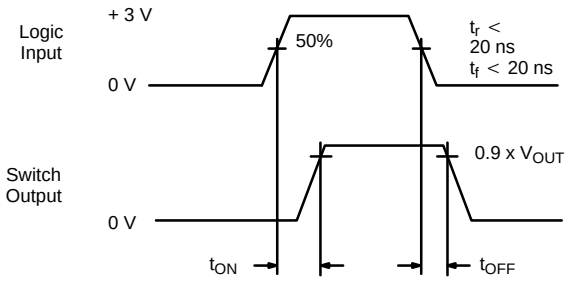


TEST CIRCUITS



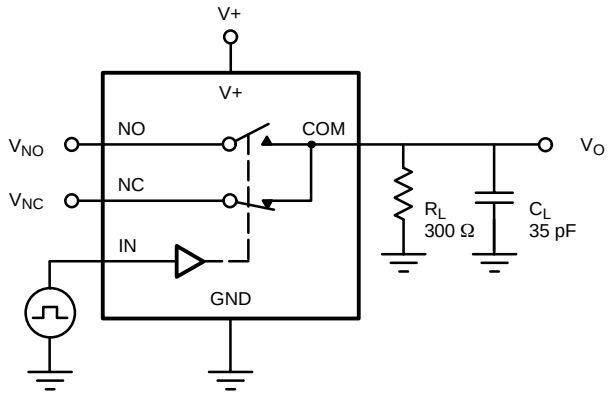
C_L (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM}\left(\frac{R_L}{R_L + R_{ON}}\right)$$



Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

FIGURE 1. Switching Time



C_L (includes fixture and stray capacitance)

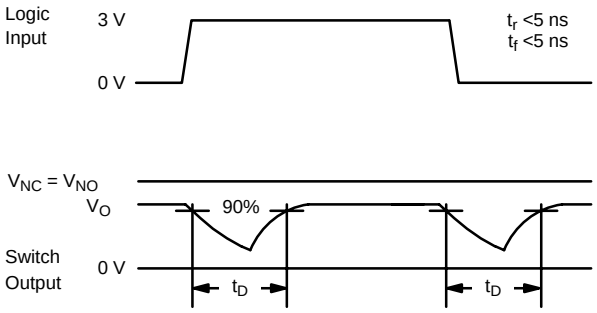
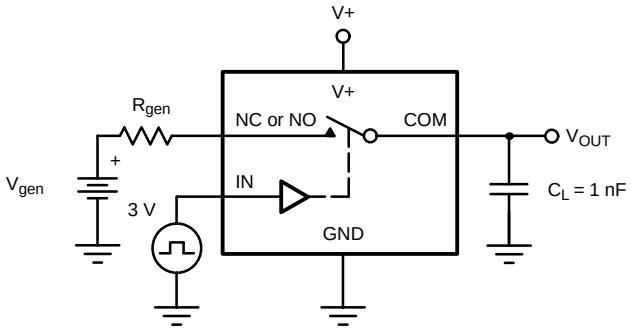
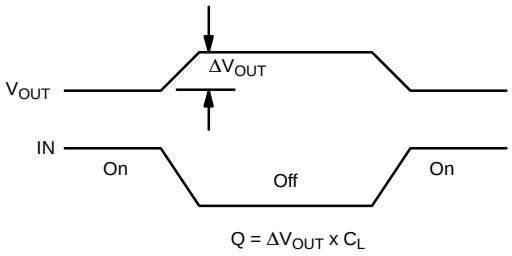


FIGURE 2. Break-Before-Make Interval





$Q = \Delta V_{OUT} \times C_L$

IN depends on switch configuration: input polarity determined by sense of switch.

FIGURE 3. Charge Injection

TEST CIRCUITS

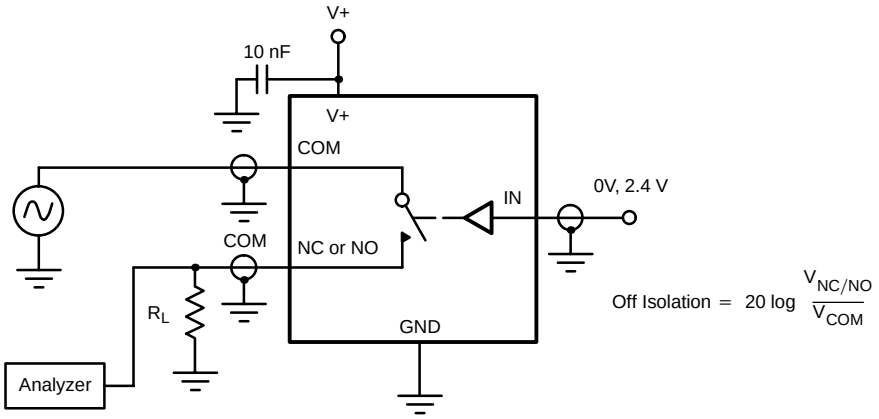


FIGURE 4. Off-Isolation

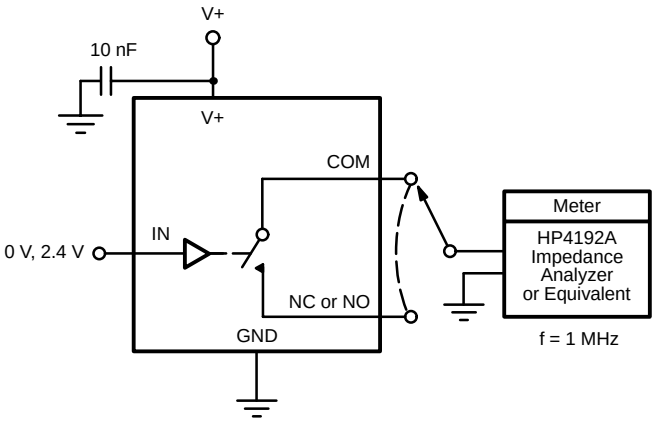


FIGURE 5. Channel Off/On Capacitance