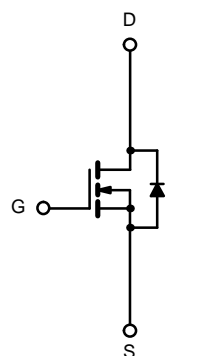
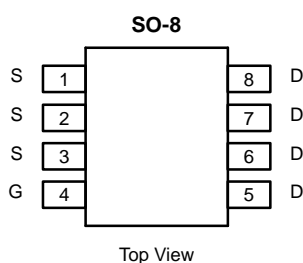




## N-Channel Reduced $Q_g$ , Fast Switching MOSFET

PRODUCT SUMMARY		
$V_{DS}$ (V)	$r_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)
200	0.420 @ $V_{GS} = 10$ V	$\pm 1.7$

**High-Efficiency**  
**PWM Optimized**



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		$V_{DS}$	200	V
Gate-Source Voltage		$V_{GS}$	$\pm 20$	
Continuous Drain Current ( $T_J = 150^\circ\text{C}$ ) <sup>a, b</sup>	$T_A = 25^\circ\text{C}$	$I_D$	$\pm 1.7$	A
	$T_A = 70^\circ\text{C}$		$\pm 1.3$	
Pulsed Drain Current		$I_{DM}$	$\pm 12$	
Avalanche Current		$I_{AS}$	$\pm 12.5$	mJ
Single Avalanche Energy		$E_{AS}$	8	
Continuous Source Current (Diode Conduction) <sup>a, b</sup>		$I_S$	2.1	A
Maximum Power Dissipation <sup>a, b</sup>	$T_A = 25^\circ\text{C}$	$P_D$	2.5	W
	$T_A = 70^\circ\text{C}$		1.6	
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>a</sup>	$t \leq 10$ sec	$R_{thJA}$		50	$^\circ\text{C/W}$
	Steady State		80		

Notes

a. Surface Mounted on FR4 Board.

b.  $t \leq 10$  sec.

For SPICE model information via the Worldwide Web: <http://www.vishay.com/www/product/spice.htm>

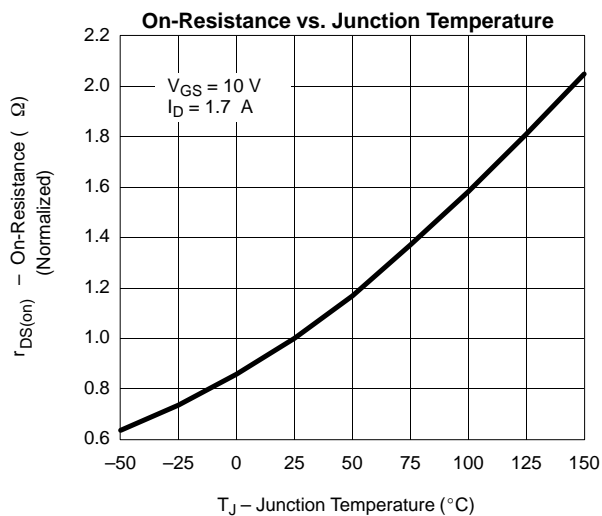
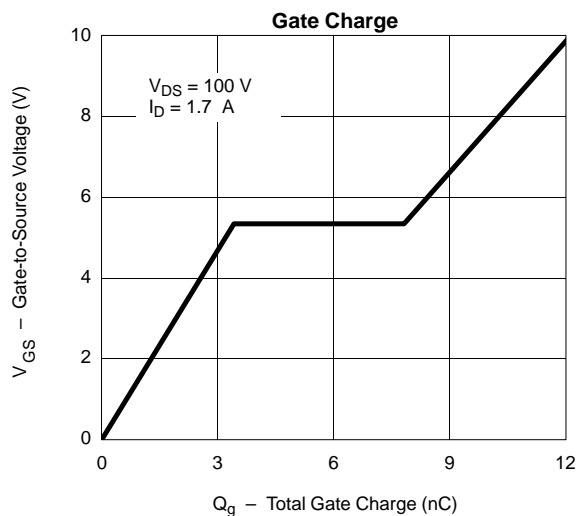
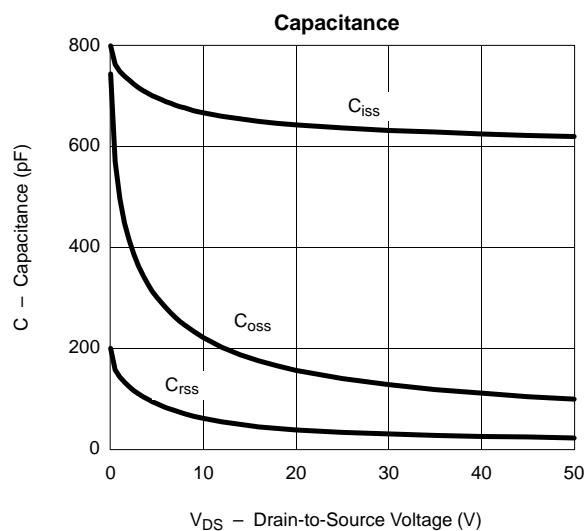
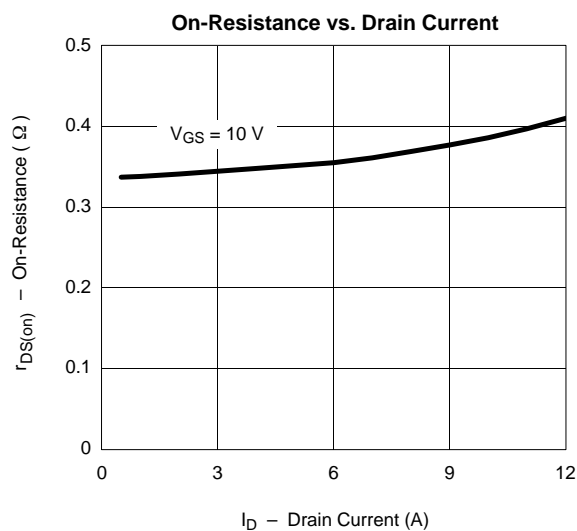
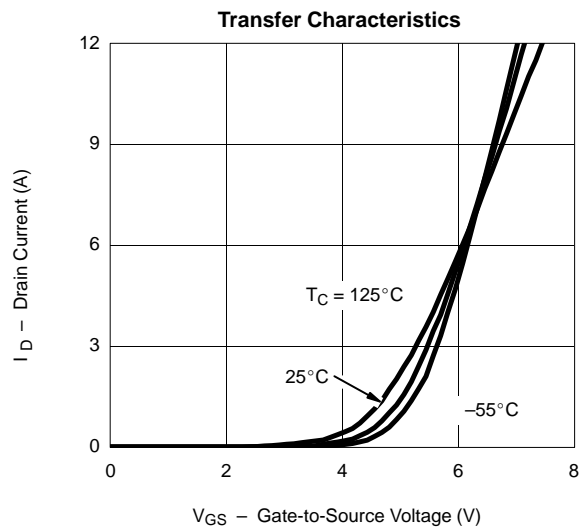
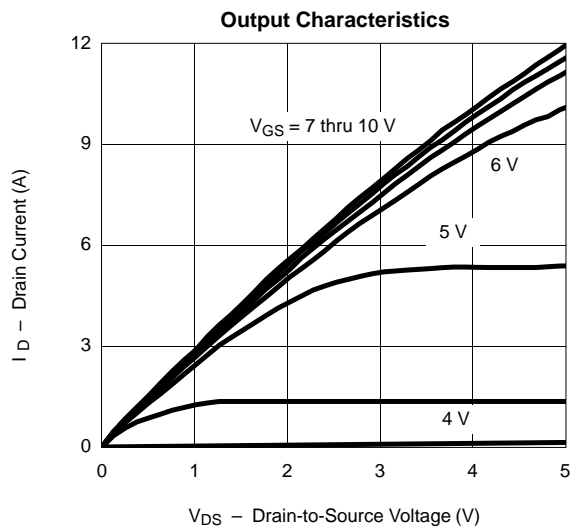
<b>SPECIFICATIONS (<math>T_J = 25^\circ\text{C}</math> UNLESS OTHERWISE NOTED)</b>						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Static</b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	2			V
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 20\ \text{V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 160\ \text{V}, V_{GS} = 0\ \text{V}$			1	$\mu\text{A}$
		$V_{DS} = 160\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 55^\circ\text{C}$			25	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 5\ \text{V}, V_{GS} = 10\ \text{V}$	5			A
Drain-Source On-State Resistance <sup>a</sup>	$r_{DS(on)}$	$V_{GS} = 10\ \text{V}, I_D = 1.7\ \text{A}$		0.340	0.420	$\Omega$
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 10\ \text{V}, I_D = 1.7\ \text{A}$		3.5		S
Diode Forward Voltage <sup>a</sup>	$V_{SD}$	$I_S = 2.1\ \text{A}, V_{GS} = 0\ \text{V}$		0.95	1.2	V
<b>Dynamic<sup>b</sup></b>						
Total Gate Charge	$Q_g$	$V_{DS} = 100\ \text{V}, V_{GS} = 10\ \text{V}, I_D = 1.7\ \text{A}$		13	25	nC
Gate-Source Charge	$Q_{gs}$			3.5		
Gate-Drain Charge	$Q_{gd}$			4.5		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 100\ \text{V}, R_L = 100\ \Omega$ $I_D \cong 1\ \text{A}, V_{GEN} = 10\ \text{V}, R_G = 6\ \Omega$		10	20	ns
Rise Time	$t_r$			10	20	
Turn-Off Delay Time	$t_{d(off)}$			20	40	
Fall Time	$t_f$			25	50	
Source-Drain Reverse Recovery Time	$t_{rr}$	$I_F = 2.1\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		115	150	

**Notes**

- a. Pulse test; pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .  
b. Guaranteed by design, not subject to production testing.



**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**



**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**

