



## N-Channel 100-V (D-S) 175°C MOSFET

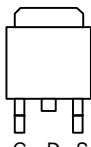
## PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)
100	0.035 @ $V_{GS} = 10$ V	34
	0.040 @ $V_{GS} = 6$ V	32

## FEATURES

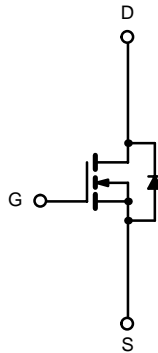
- TrenchFET® Power MOSFETS
- 175°C Junction Temperature
- New Low Thermal Resistance Package

TO-263



Top View

Ordering Information: SUM34N10-35



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ( $T_C = 25^\circ\text{C}$  UNLESS OTHERWISE NOTED)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		$V_{DS}$	100	V
Gate-Source Voltage		$V_{GS}$	$\pm 20$	
Continuous Drain Current ( $T_J = 175^\circ\text{C}$ )	$T_C = 25^\circ\text{C}$	$I_D$	34 <sup>a</sup>	A
	$T_C = 125^\circ\text{C}$		20 <sup>a</sup>	
Pulsed Drain Current		$I_{DM}$	60	
Avalanche Current		$I_{AR}$	34	
Repetitive Avalanche Energy <sup>b</sup>	$L = 0.1$ mH	$E_{AR}$	57.8	mJ
	$T_C = 25^\circ\text{C}$		100 <sup>c</sup>	
Maximum Power Dissipation <sup>b</sup>	$T_A = 25^\circ\text{C}^d$	$P_D$	3.75	W
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	-55 to 175	$^\circ\text{C}$

## THERMAL RESISTANCE RATINGS

Parameter	Symbol	Limit	Unit
Junction-to-Ambient (PCB Mounted) <sup>d</sup>	$R_{thJA}$	40	$^\circ\text{C/W}$
Junction-to-Case (Drain)	$R_{thJC}$	1.5	

## Notes

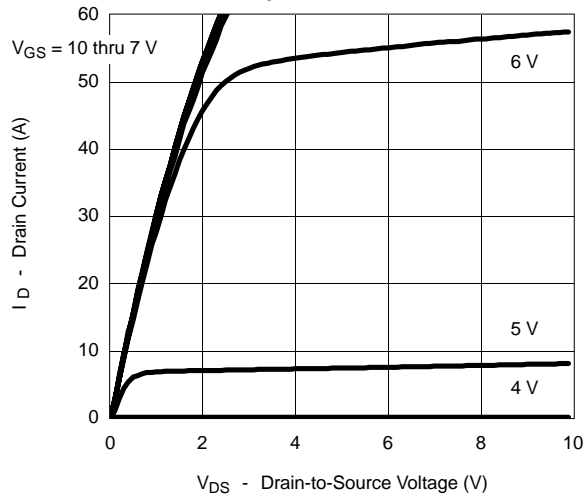
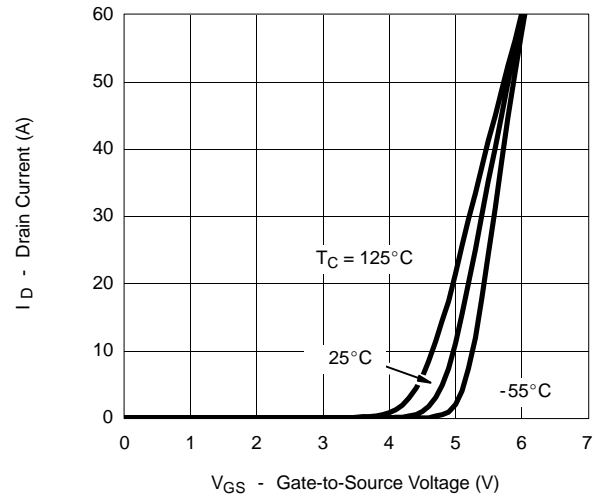
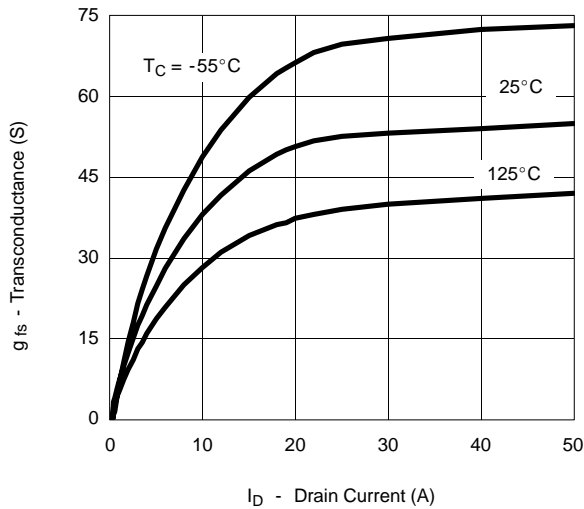
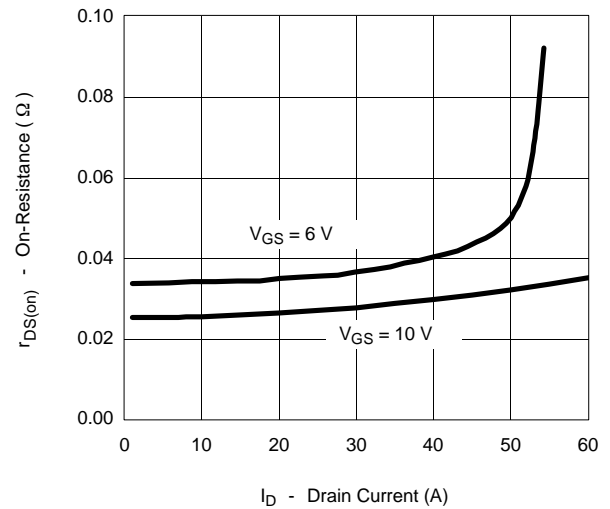
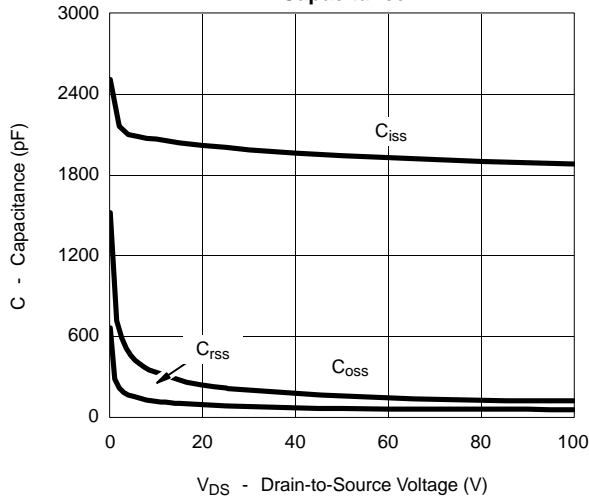
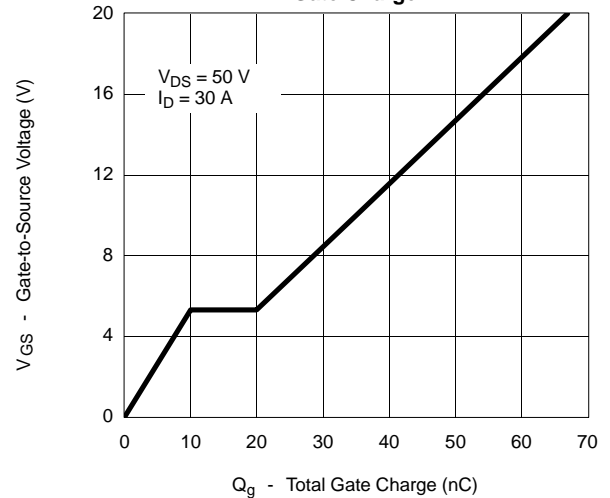
- Package limited.
- Duty cycle  $\leq 1\%$ .
- See SOA curve for voltage derating.
- When mounted on 1" square PCB (FR-4 material).

**SPECIFICATIONS (T<sub>J</sub> = 25 °C UNLESS OTHERWISE NOTED)**

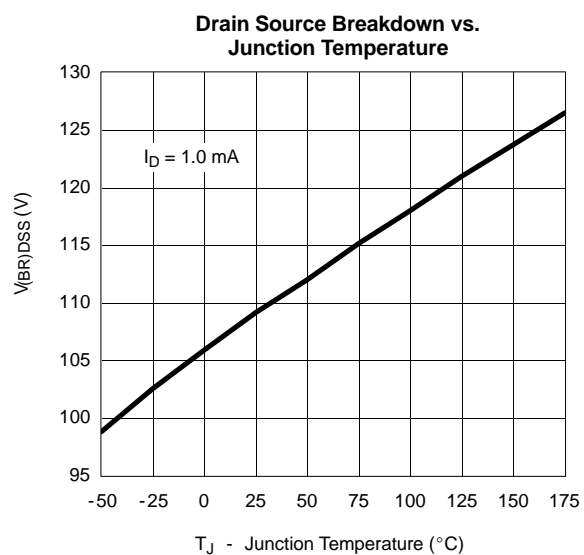
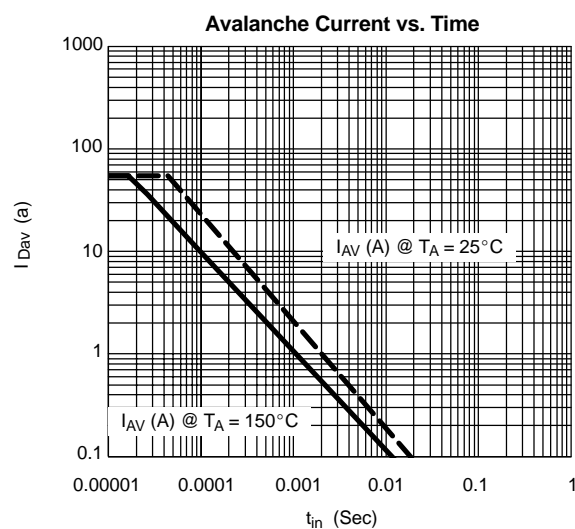
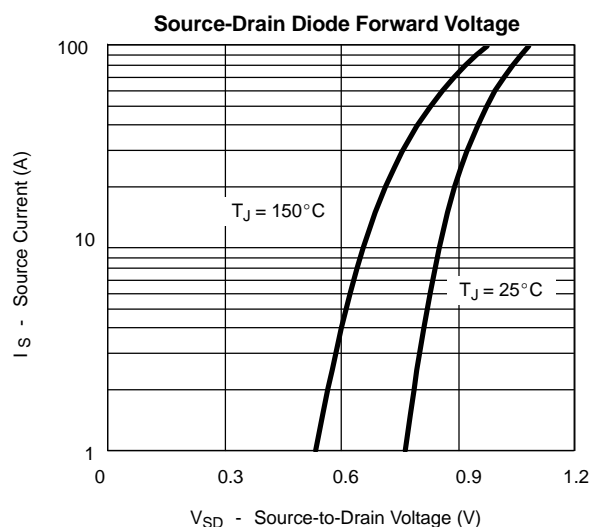
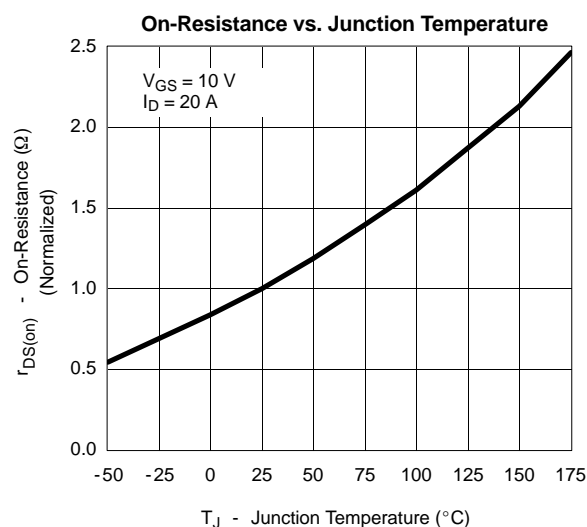
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>DS</sub> = 0 V, I <sub>D</sub> = 250 μA	100			V
Gate-Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2		4	
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 80 V, V <sub>GS</sub> = 0 V			1	μA
		V <sub>DS</sub> = 80 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125°C			50	
		V <sub>DS</sub> = 80 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 175°C			250	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ 5 V, V <sub>GS</sub> = 10 V	60			A
Drain-Source On-State Resistance <sup>a</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A		0.028	0.035	Ω
		V <sub>GS</sub> = 6 V, I <sub>D</sub> = 15 A		0.032	0.040	
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A, T <sub>J</sub> = 125°C			0.067	
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A, T <sub>J</sub> = 175°C			0.087	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 30 A	10			S
Dynamic <sup>b</sup>						
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 25 V, f = 1 MHz		2000		pF
Output Capacitance	C <sub>oss</sub>			210		
Reverse Transfer Capacitance	C <sub>rss</sub>			77		
Total Gate Charge <sup>c</sup>	Q <sub>g</sub>	V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 30 A		35	55	nC
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>			10		
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>			10		
Gate Resistance	R <sub>G</sub>			4.5		Ω
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>	V <sub>DD</sub> = 50 V, R <sub>L</sub> = 1.67 Ω I <sub>D</sub> ≅ 30 A, V <sub>GEN</sub> = 10 V, R <sub>G</sub> = 2.5 Ω		11	20	ns
Rise Time <sup>c</sup>	t <sub>r</sub>			65	100	
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>			30	45	
Fall Time <sup>c</sup>	t <sub>f</sub>			55	85	
Source-Drain Diode Ratings and Characteristics (T <sub>C</sub> = 25°C) <sup>b</sup>						
Continuous Current	I <sub>S</sub>				34	A
Pulsed Current	I <sub>SM</sub>				60	
Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>F</sub> = 20 A, V <sub>GS</sub> = 0 V		1.0	1.5	V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 60 A, di/dt = 100 A/μs		125	200	ns
Peak Reverse Recovery Current	I <sub>RM(REC)</sub>			4.5	7	A
Reverse Recovery Charge	Q <sub>rr</sub>			0.28	0.7	μC

## Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.  
b. Guaranteed by design, not subject to production testing.  
c. Independent of operating temperature.

**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)****Output Characteristics****Transfer Characteristics****Transconductance****On-Resistance vs. Drain Current****Capacitance****Gate Charge**

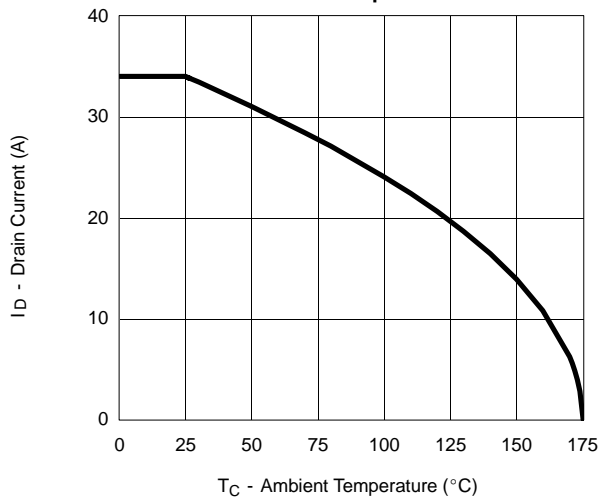
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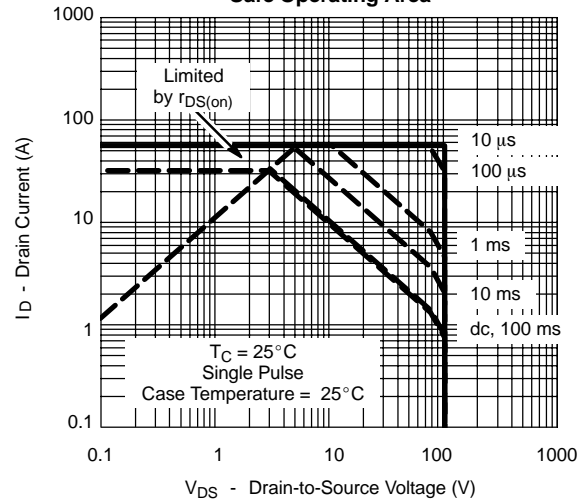


**THERMAL RATINGS**

Maximum Avalanche and Drain Current  
vs. Case Temperature



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case

