



N-Channel 20-V (D-S), 175°C MOSFET

CHARACTERISTICS

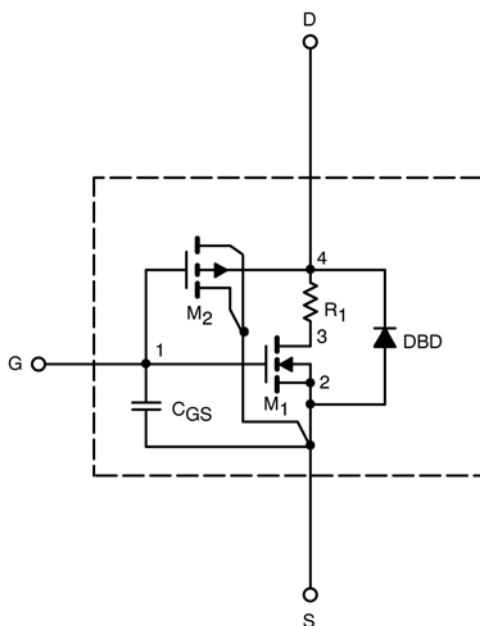
- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to 125°C temperature ranges under the pulsed 0 to 10V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.



| SPECIFICATIONS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED) | | | | | |
|---|--------------|---|----------------|---------------|----------|
| Parameter | Symbol | Test Conditions | Simulated Data | Measured Data | Unit |
| Static | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$ | 1.7 | | V |
| On-State Drain Current ^a | $I_{D(on)}$ | $V_{DS} = 5\ \text{V}$, $V_{GS} = 10\ \text{V}$ | 438 | | A |
| Drain-Source On-State Resistance ^a | $r_{DS(on)}$ | $V_{GS} = 10\ \text{V}$, $I_D = 20\ \text{A}$ | 0.0078 | 0.008 | Ω |
| | | $V_{GS} = 10\ \text{V}$, $I_D = 20\ \text{A}$, $T_J = 125^\circ\text{C}$ | 0.010 | | |
| | | $V_{GS} = 4.5\ \text{V}$, $I_D = 20\ \text{A}$ | 0.0136 | 0.0135 | |
| Forward Voltage ^a | V_{SD} | $I_F = 40\ \text{A}$, $V_{GS} = 0\ \text{V}$ | 0.91 | 1.1 | V |
| Dynamic^b | | | | | |
| Input Capacitance | C_{iss} | $V_{GS} = 0\ \text{V}$, $V_{DS} = 10\ \text{V}$, $f = 1\ \text{MHz}$ | 1212 | 1300 | pF |
| Output Capacitance | C_{oss} | | 470 | 470 | |
| Reverse Transfer Capacitance | C_{rss} | | 237 | 275 | |
| Total Gate Charge ^c | Q_g | $V_{DS} = 10\ \text{V}$, $V_{GS} = 4.5\ \text{V}$, $I_D = 40\ \text{A}$ | 10.6 | 10.5 | nC |
| Gate-Source Charge ^c | Q_{gs} | | 4.2 | 4.2 | |
| Gate-Drain Charge ^c | Q_{gd} | | 4 | 4 | |
| Turn-On Delay Time ^c | $t_{d(on)}$ | $V_{DD} = 10\ \text{V}$, $R_L = 0.25\ \Omega$ $I_D \cong 40\ \text{A}$, $V_{GEN} = 10\ \text{V}$, $R_G = 2.5\ \Omega$ | 9 | 8 | ns |
| Rise Time ^c | t_r | | 9 | 10 | |
| Turn-Off Delay Time ^c | $t_{d(off)}$ | | 32 | 25 | |
| Fall Time ^c | t_f | | 10 | 12 | |
| Source-Drain Reverse Recovery Time | t_{rr} | $I_F = 40\ \text{A}$, $di/dt = 100\ \text{A}/\mu\text{s}$ | 31 | 35 | |

Notes

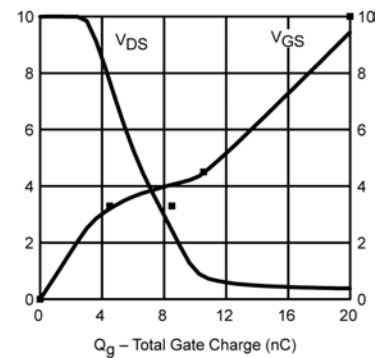
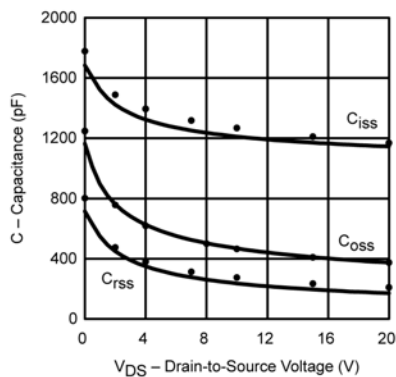
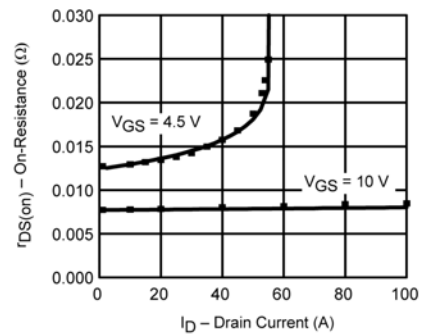
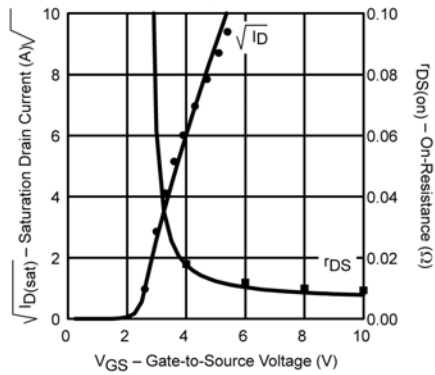
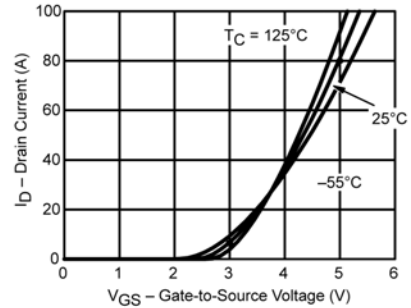
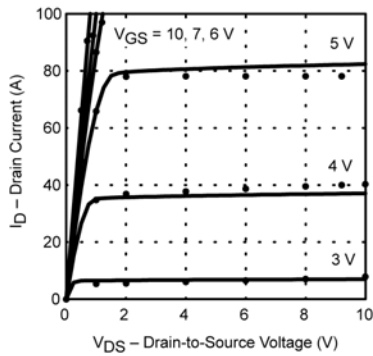
- Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.
- Independent of operating temperature.



SPICE Device Model SUM40N02-09P

Vishay Siliconix

COMPARISON OF MODEL WITH MEASURED DATA ($T_J=25^\circ\text{C}$ UNLESS OTHERWISE NOTED)



Note: Dots and squares represent measured data.