

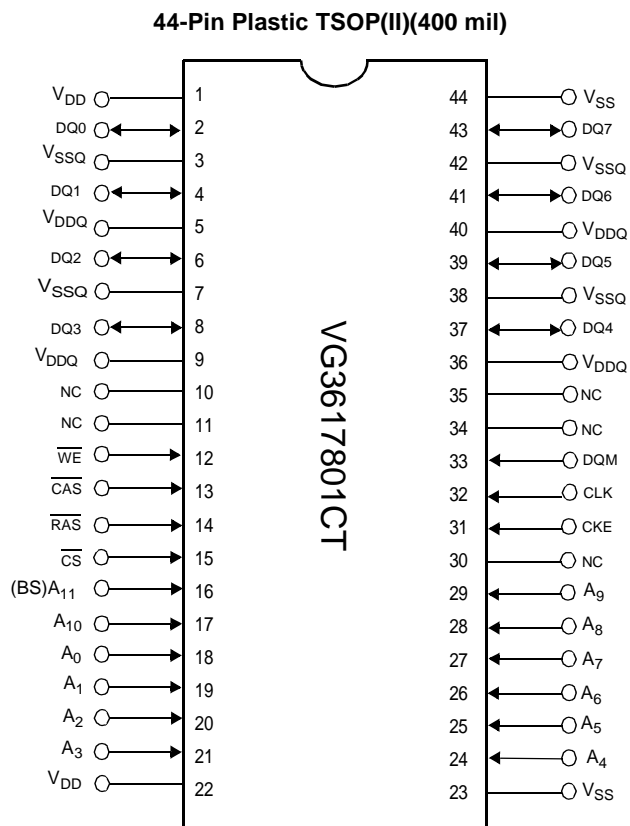
Description

The VG3617801CT is CMOS Synchronous Dynamic RAMs organized as 1,048,576-word X 8-bit X 2-bank. It is fabricated with an advanced submicron CMOS technology and is designed to operate from a single 3.3V power supply. This is packaged using JEDEC standard pinouts and standard plastic TSOP.

Features

- Single 3.3V($\pm 0.3V$) power supply
- Clock Frequency:100MHz
- Fully synchronous with all signals referenced to a positive clock edge
- Programmable $\overline{\text{CAS}}$ latency (2,3)
- Programmable burst length (1,2,4,8,& Full page)
- Programmable wrap sequence (Sequential/Interleave)
- Automatic precharge and controlled precharge
- Auto refresh and self refresh modes
- Dual Internal banks controlled by A11(Bank select)
- Simultaneous and independent two bank operation
- I/O level : LVTTTL interface
- Random column access in every cycle
- X8 organization
- Input/output control by DQM
- 2048 refresh cycles/32ms
- Burst termination by burst stop and precharge command
- Burst read single write option

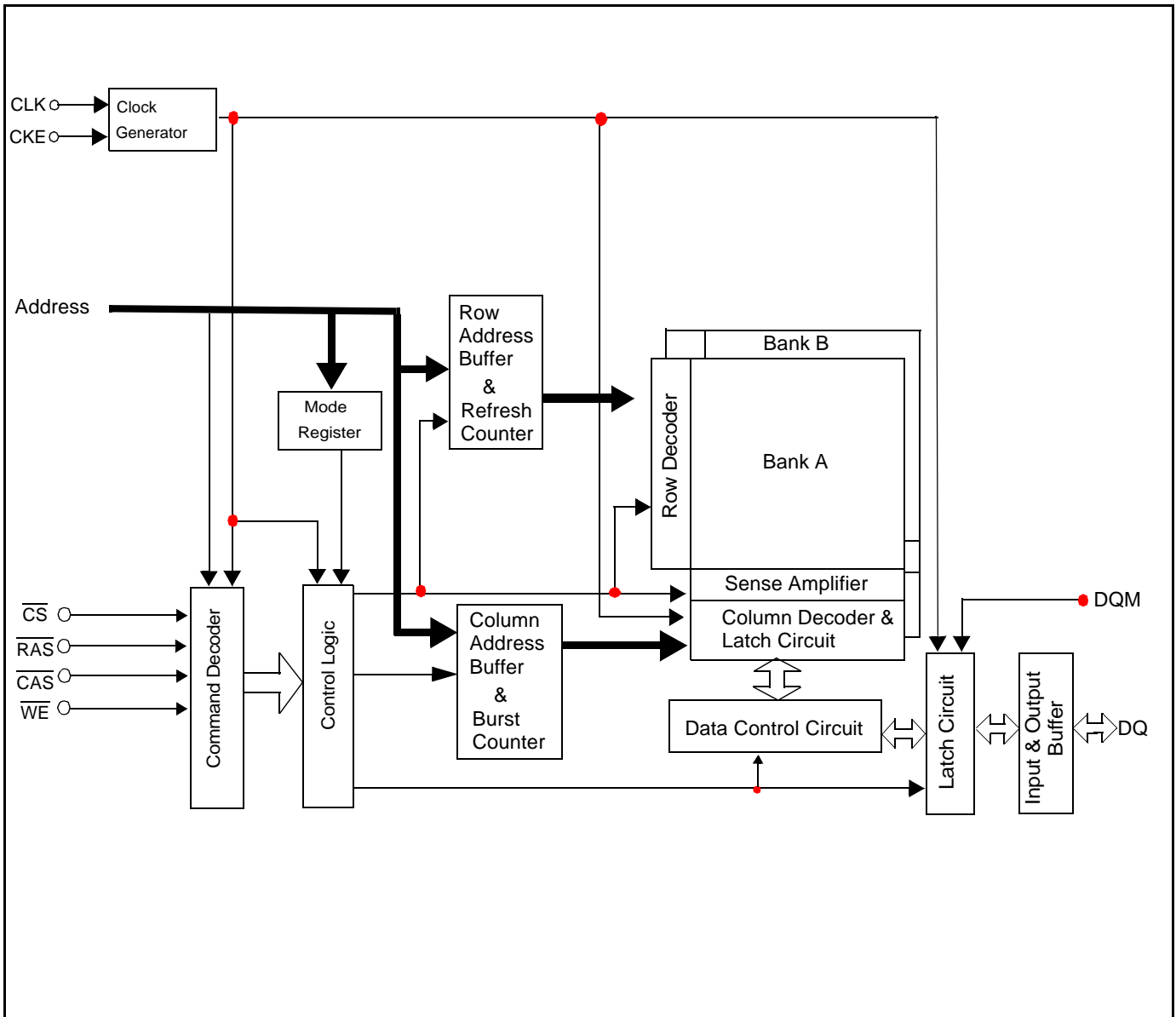
Pin Configuration



Pin Description (VG3617801CT)

| Pin Name | Function | Pin Name | Function |
|------------------|---|------------------|-----------------------|
| A0-A11 | Address inputs - Row address A0-A10 - Column address A0-A8 A11:Bank select | DQM | DQ mask enable |
| DQ0~DQ7 | Data-in/data-out | CLK | Clock input |
| \overline{RAS} | Row address strobe | CKE | Clock enable |
| \overline{CAS} | Column address strobe | \overline{CS} | Chip select |
| \overline{WE} | Write enable | V _{DDQ} | Supply voltage for DQ |
| V _{SS} | Ground | V _{SSQ} | Ground for DQ |
| V _{DD} | Power | | |

Block Diagram



Absolute Maximum Ratings

| Parameter | Symbol | Value | Unit |
|------------------------------------|-------------------|--------------|------|
| Voltage on any pin relative to Vss | V_{IN}, V_{OUT} | -1.0 to +4.6 | V |
| Supply voltage relative to Vss | V_{DD}, V_{DDQ} | -1.0 to +4.6 | V |
| Short circuit output current | I_{OUT} | 50 | mA |
| Power dissipation | P_D | 1.0 | W |
| Operating temperature | T_{OPT} | 0 to + 70 | °C |
| Operating temperature | T_{STG} | -55 to + 125 | °C |

Recommended DC Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|--------------------------------|----------|------|-----|--------------|------|------|
| Supply Voltage | V_{DD} | 3.0 | 3.3 | 3.6 | V | |
| Input High Voltage, all inputs | V_{IH} | 2.0 | °— | $V_{DD}+0.3$ | V | 1 |
| Input Low Voltage, all inputs | V_{IL} | -0.3 | °— | 0.8 | V | 2 |

Note 1.Overshoot limit : $V_{IH(MAX.)}=V_{DDQ}+2.0V$ with a pulse width < 3ns

2.Undershoot limit : $V_{IL}=V_{SSQ}-2.0V$ with a pulse < 3ns and -1.5V with a pulse < 5ns

Capacitance

(Ta=25°C, f=1MHZ)

| Parameter | Symbol | Min | Max | Unit |
|--|-----------|-----|-----|------|
| Input capacitance(CLK) | C_{11} | 2.5 | 4 | pF |
| Input capacitance(all input pins except data pins) | C_{12} | 2.5 | 5 | pF |
| Data input/output capacitance | $C_{I/O}$ | 4.0 | 6.5 | pF |

DC Characteristics(Recommended Operating Conditions unless otherwise noted)

| Parameter | Symbol | Test Conditions | | VG3617801CT | | | | | | Unit | Notes |
|---|--------------------|--|------|-------------|-----|-----|-----|-----|-----|------|-------|
| | | | | -8H | | -8L | | -10 | | | |
| | | | | Min | Max | Min | Max | Min | Max | | |
| Operating current | I _{CC1} | Burst length=1 | CL=3 | | 90 | | 90 | | 85 | mA | 1,2 |
| | | t _{RC} ≥ t _{RC (MIN.)} ,Io=0mA One bank active | CL=2 | | 85 | | 85 | | 80 | | |
| Precharge standby current in power down mode | I _{CC2P} | CKE ≤ V _{IL(MAX.)} t _{CK} =15ns | | | 3 | | 3 | | 3 | mA | |
| | I _{CC2PS} | CKE ≤ V _{IL(MAX.)} t _{CK} =∞ | | | 2 | | 2 | | 2 | | |
| Precharge standby current in Nonpower down mode | I _{CC2N} | CKE ≥ V _{IH(MIN.)} t _{CK} =15ns CS ≥ V _{IH(MIN.)} Input signals are changed. one time during 30ns. | | | 30 | | 30 | | 30 | mA | |
| | I _{CC2NS} | CKE ≥ V _{IH(MIN.)} , t _{CK} =∞ CLK ≤ V _{IL(MAX.)} Input signals are stable. | | | 6 | | 6 | | 6 | | |
| Active standby current in power down mode | I _{cc3P} | CKE ≤ V _{IL(MAX.)} ,t _{CK} =15ns | | | 3 | | 3 | | 3 | mA | |
| | I _{cc3PS} | CKE ≤ V _{IL(MAX.)} ,t _{CK} =∞ | | | 2 | | 2 | | 2 | | |
| Active standby current in nonpower down mode | I _{cc3N} | CKE ≥ V _{IL(MAX.)} ,t _{CK} =15ns CS ≥ V _{IL(MIN.)} Input signals are changed one time during 30ns | | | 30 | | 30 | | 30 | mA | |
| | I _{cc3NS} | CKE ≥ V _{IH(MIN.)} t _{CK} =∞ CLE ≤ V _{IL(MAX.)} Input signals are stable. | | | 15 | | 15 | | 15 | | |
| Operating current (Burst mode) | I _{cc4} | t _{CK} ≥ t _{CK (MIN.)} ,Io=0mA Burst length=4 | CL=3 | | 120 | | 120 | | 105 | mA | 1,2 |
| | | | CL=2 | | 115 | | 105 | | 100 | | |
| Refresh current | I _{cc5} | t _{RC} ≥ t _{RC (MIN.)} | CL=3 | | 110 | | 110 | | 100 | mA | 2 |
| | | | CL=2 | | 105 | | 105 | | 95 | | |
| Self refresh current | I _{cc6} | CKE ≤ 0.2V | | | 2 | | 2 | | 2 | mA | |
| Input leakage current | I _{LI} | V _{in} ≥ 0 , V _{in} ≤ V _{DD} +0.3V Pins not under test=0V | | -5 | 5 | -5 | 5 | -5 | 5 | uA | |
| Output leakage current | I _{LO} | V _{OUT} ≥ 0 , V _{OUT} ≤ V _{DD} +0.3V DQ# in H-Z., Dout disabled | | -5 | 5 | -5 | 5 | -5 | 5 | uA | |
| Output Low Voltage | V _{OL} | I _{OL} =2mA | | | 0.4 | | 0.4 | | 0.4 | V | |
| Output High Voltage | V _{OH} | I _{OH} =2mA | | 2.4 | | 2.4 | | 2.4 | | V | |

Notes 1. I_{CC} depends on output loading and cycle rates. Specified values are obtained with the output open.

2. I_{CC} is measured on condition that addresses are changed only one time during $t_{CK(MIN.)}$.

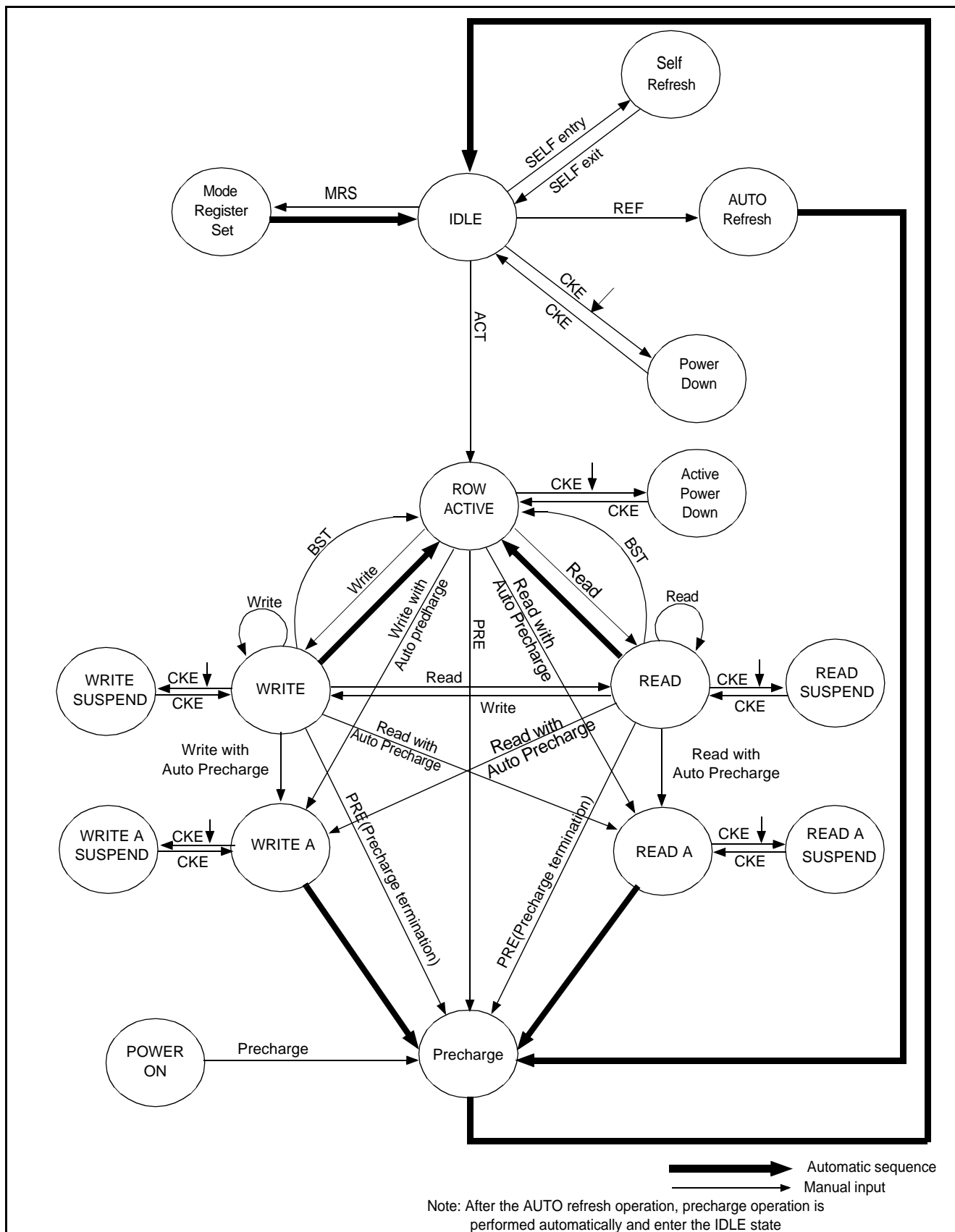
A.C Characteristics:
Test Conditions: (Ta=0 to 70°C V_{DD}=3.3V ±0.3V ,V_{SS}=0V)

| | | | |
|--|----------|--|------|
| AC input Levels(V _{IH} /V _{IL}) | 2.0/0.8V | Input timing reference level/ Output timing reference level | 1.4V |
| Input rise and fall time | 1ns | Output load condition | 50pF |

| Parameter | CAS Latency | symbol | VG3617801CT | | | | | | Unit |
|---|-------------|------------------|----------------------|---------|----------------------|---------|----------------------|---------|------|
| | | | -8H | | -8L | | -10 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| CLK cycle time | 3 | t _{Ck3} | 10 | | 10 | | 10 | | ns |
| | 2 | t _{Ck2} | 10 | | 13 | | 15 | | ns |
| CLK to valid output delay | 3 | t _{AC3} | | 6 | | 6 | | 8 | ns |
| | 2 | t _{AC2} | | 6 | | 7 | | 8 | ns |
| CLK high pulse width | | t _{CH} | 3 | | 3 | | 4 | | ns |
| CLK low pulse width | | t _{CL} | 3 | | 3 | | 4 | | ns |
| CKE setup time | | t _{CKS} | 3 | | 3 | | 3 | | ns |
| CKE hold time | | t _{CKH} | 1 | | 1 | | 1 | | ns |
| Address setup time | | t _{AS} | 2 | | 2 | | 3 | | ns |
| Address hold time | | t _{AH} | 1 | | 1 | | 1 | | ns |
| Data input setup time | | t _{DS} | 2 | | 2 | | 3 | | ns |
| Data input hold time | | t _{DH} | 1 | | 1 | | 1 | | ns |
| Command setup time | | t _{CMS} | 2 | | 2 | | 3 | | ns |
| Command hold time | | t _{CMH} | 1 | | 1 | | 1 | | ns |
| Output data hold time | | t _{OH} | 3 | | 3 | | 3 | | ns |
| CLK to output in low-Z | | t _{LZ} | 0 | | 0 | | 0 | | ns |
| CLK to output in Hi-Z | | t _{HZ} | 3 | 8 | 3 | 8 | 3 | 8 | ns |
| Row active to active delay | | t _{RRD} | 20 | | 20 | | 20 | | ns |
| RAS to CAS delay | | t _{RCD} | 20 | | 20 | | 26 | | ns |
| Row precharge time | | t _{RP} | 20 | | 20 | | 26 | | ns |
| ROW active time | | t _{RAS} | 50 | 120,000 | 50 | 120,000 | 60 | 120,000 | ns |
| ROW cycle time | | t _{RC} | 70 | | 70 | | 86 | | ns |
| Last data in to burst stop | | t _{BDL} | 1 CLK | | 1 CLK | | 1 CLK | | ns |
| Data-in to ACT(REF) Command (Auto Precharge) | | t _{DAL} | 1CLK+t _{RP} | | 1CLK+t _{RP} | | 1CLK+t _{RP} | | ns |
| Data-in to precharge | | t _{DPL} | 1 CLK | | 1 CLK | | 1 CLK | | ns |
| Transition time | | t _T | 1 | 10 | 1 | 10 | 1 | 10 | ns |
| Mode reg. set cycle | | t _{RSC} | 2 CLK | | 2 CLK | | 2 CLK | | ns |
| Power down exit setup time | | t _{PDE} | 8 | | 8 | | 8 | | ns |
| Self refresh exit time | | t _{SRX} | 8 | | 8 | | 8 | | ns |
| Refresh time | | t _{REF} | | 32 | | 32 | | 32 | ms |

Basic Features and Function description

1.simplified State diagram



2.Truth Table

2.1 Command Truth Table

| FUNCTION | Symbol | CKE | | $\overline{\text{CS}}$ | $\overline{\text{RAS}}$ | $\overline{\text{CAS}}$ | $\overline{\text{WE}}$ | A11 | A10 | A9-A0 |
|---------------------------|--------|-----|---|------------------------|-------------------------|-------------------------|------------------------|-----|-----|-------|
| | | n-1 | n | | | | | | | |
| Device deselect | DESL | H | X | H | X | X | X | X | X | X |
| No operation | NOP | H | X | L | H | H | H | X | X | X |
| Mode register set | MRS | H | X | L | L | L | L | L | X | V |
| Bank activate | ACT | H | X | L | L | H | H | V | V | V |
| Read | READ | H | X | L | H | L | H | V | L | V |
| Read with auto precharge | READA | H | X | L | H | L | H | V | H | V |
| Write | WRIT | H | X | L | H | L | L | V | L | V |
| Write with auto precharge | WRITA | H | X | L | H | L | L | V | H | V |
| Precharge select bank | PRE | H | X | L | L | H | L | V | L | X |
| Precharge all banks | PALL | H | X | L | L | H | L | X | H | X |
| Burst stop | BST | H | X | L | H | H | L | X | X | X |
| Auto refresh (CBR) | CBR | H | H | L | L | L | H | X | X | X |

2.2 DQM Truth Table

| FUNCTION | Symbol | CKE | | DQM | |
|---|--------|-----|-----|-----|---|
| | | n-1 | n-1 | U | L |
| Data write/output enable | ENB | H | X | L | |
| Data mask/output disable | MASK | H | X | H | |
| Upper byte write enable/output enable | ENBU | H | X | L | X |
| Lower byte write enable/output enable | ENBL | H | X | X | L |
| Upper byte write inhibit/output disable | MASKU | H | X | H | X |
| Lower byte inhibit/output disable | MASKL | H | X | X | H |

2.3 CKE Truth Table

| Current State | Function | Symbol | CKE | | $\overline{\text{CS}}$ | $\overline{\text{RAS}}$ | $\overline{\text{CAS}}$ | $\overline{\text{WE}}$ | Address |
|---------------|--------------------------|--------|-----|---|------------------------|-------------------------|-------------------------|------------------------|---------|
| | | | n-1 | n | | | | | |
| Activating | Clock suspend mode entry | | H | L | X | X | X | X | X |
| Any | Clock suspend | | L | L | X | X | X | X | X |
| Clock suspend | Clock suspend mode exit | | L | H | X | X | X | X | X |
| Idle | CBR refresh command | REF | H | H | L | L | L | H | X |
| Idle | Self refresh entry | SELF | H | L | L | L | L | H | X |
| Self refresh | Self refresh exit | | L | H | L | H | H | H | X |
| | | | L | H | H | X | X | X | X |
| Idle | Power down entry | | H | L | X | X | X | X | X |
| Power down | Power down exit | | L | H | X | X | X | X | X |

H : High level, L : Low level

X : high or Low level(Don't care), V : Valid Data input

2.4 Operative Command Table Notes 1

(1/3)

| Current state | $\overline{\text{CS}}$ | $\overline{\text{RAS}}$ | $\overline{\text{CAS}}$ | $\overline{\text{WE}}$ | Address | Command | Action | Notes |
|---------------|------------------------|-------------------------|-------------------------|------------------------|-----------|------------|--|-------|
| Idle | H | X | X | X | X | DESL | Nop or Power down | 2 |
| | L | H | H | X | X | NOP or BST | Nop or Power down | 2 |
| | L | H | L | H | BA,CA,A10 | READ/READA | ILLEGAL | 3 |
| | L | H | L | L | BA,CA,A10 | WRIT/WRITA | ILLEGAL | 3 |
| | L | L | H | H | BR,RA | ACT | Row active | |
| | L | L | H | L | BA,A10 | PRE/PALL | Nop | |
| | L | L | L | H | X | REF/SELF | Refresh or Self refresh | 4 |
| | L | L | L | L | Op-Code | MPS | Mode register access | |
| Row active | H | X | X | X | X | DESL | Nop | |
| | L | H | H | X | X | NOP or BST | Nop | |
| | L | H | L | H | BA,CA,A10 | READ/READA | Begin read:Determine AP | 5 |
| | L | H | L | L | BA,CA,A10 | WRIT/WRITA | Begin write:Determine AP | 5 |
| | L | L | H | H | BA,RA | ACT | ILLEGAL | 3 |
| | L | L | H | L | BA,A10 | PRE/PALL | Precharge | 6 |
| | L | L | L | H | X | REF/SELF | ILLEGAL | |
| | L | L | L | L | Op-Code | MRS | ILLEGAL | |
| Read | H | X | X | X | X | DESL | Continue burst to end → Row active | |
| | L | H | H | H | X | NOP | Continue burst to end → Row active | |
| | L | H | H | L | X | BST | Burst stop → Row active | |
| | L | H | L | H | BA,CA,A10 | READ/READA | Term burst, new read:Determine AP | 7 |
| | L | H | L | L | BA,CA,A10 | WRIT/WRITA | Term burst, start write:Determine AP | 7,8 |
| | L | L | H | H | BA,RA | ACT | ILLEGAL | 3 |
| | L | L | H | L | BA,A10 | PRE/PALL | Term burst,precharging | |
| | L | L | L | H | X | REF/SELF | ILLEGAL | |
| | L | L | L | L | Op-Code | MRS | ILLEGAL | |
| Write | H | X | X | X | X | DESL | Continue burst to end → write recovering | |
| | L | H | H | H | X | NOP | Continue burst to end → Write recovering | |
| | L | H | H | L | X | BST | Burst stop → Row active | |
| | L | H | L | H | BA,CA,A10 | READ/READA | Term burst, start read: determine AP | 7,8 |
| | L | H | L | L | BA,CA,A10 | WRIT/WRITA | Term burst, new write:Determine AP | 7 |
| | L | L | H | H | BA,RA | ACT | ILLEGAL | 3 |
| | L | L | H | L | BA,A10 | PRE/PALL | Term burst precharging | 9 |
| | L | L | L | H | X | REF/SELF | ILLEGAL | |
| | L | L | L | L | Op-Code | MRS | ILLEGAL | |

| Current state | \overline{CS} | \overline{RAS} | \overline{CA} | \overline{WE} | Address | Command | Action | Notes |
|---------------------------|-----------------|------------------|-----------------|-----------------|-----------|------------|--|-------|
| Read with auto precharge | H | X | X | X | X | DESL | Continue burst to end → Precharging | |
| | L | H | H | H | X | NOP | Continue burst to end → Precharging | |
| | L | H | H | L | X | BST | ILLEGAL | |
| | L | H | L | H | BA,CA,A10 | READ/READA | ILLEGAL | |
| | L | H | L | L | BA,CA,A10 | WRIT/WRITA | ILLEGAL | |
| | L | L | H | H | BA,RA | ACT | ILLEGAL | 3 |
| | L | L | H | L | BA,A10 | PRE/PALL | ILLEGAL | 3 |
| | L | L | L | H | X | PEF/SELF | ILLEGAL | |
| | L | L | L | L | Op-Code | MRS | ILLEGAL | |
| Write with auto precharge | H | X | X | X | X | DESL | Continue burst to end → Write recovering with auto precharge | |
| | L | H | H | H | X | NOP | Continue burst to end → Write recovering with auto precharge | |
| | L | H | H | L | X | BST | ILLEGAL | |
| | L | H | L | H | BA,CA,A10 | READ/READA | ILLEGAL | |
| | L | H | L | L | BA,CA,A10 | WRIT/WRITA | ILLEGAL | |
| | L | L | H | H | BA,RA | ACT | ILLEGAL | 3 |
| | L | L | H | L | BA,A10 | PRE/PALL | ILLEGAL | 3 |
| | L | L | L | H | X | REF/SELF | ILLEGAL | |
| | L | L | L | L | Op-code | MRS | ILLEGAL | |
| Precharging | H | X | X | X | X | DESL | Nop → Enter idle after t_{RP} | |
| | L | H | H | H | X | NOP | Nop → Enter idle after t_{RP} | |
| | L | H | H | L | X | BST | Nop → Enter idle after t_{RP} | |
| | L | H | L | H | BA,CA,A10 | READ/READA | ILLEGAL | 3 |
| | L | H | L | L | BA,CA,A10 | WRIT/WRITA | ILLEGAL | 3 |
| | L | L | H | H | BA,RA | ACT | ILLEGAL | 3 |
| | L | L | H | L | BA,A10 | PRE/PALL | Nop → Enter idle after t_{RP} | |
| | L | L | L | H | X | REF/SELF | ILLEGAL | |
| | L | L | L | L | Op-Code | MRS | ILLEGAL | |
| Row activating | H | X | X | X | X | DESL | Nop → Enter row active after t_{RCD} | |
| | L | H | H | H | X | NOP | Nop → Enter row active after t_{RCD} | |
| | L | H | H | L | X | BST | Nop → Enter row active after t_{RCD} | |
| | L | H | L | H | BA,CA,A10 | READ/READA | ILLEGAL | 3 |
| | L | H | L | L | BA,CA,A10 | WRIT/WRITA | ILLEGAL | 3 |
| | L | L | H | H | BA,RA | ACT | ILLEGAL | 3,10 |
| | L | L | H | L | BA,A10 | PRE/PALL | ILLEGAL | 3 |
| | L | L | L | H | X | REF/SELF | ILLEGAL | |
| | L | L | L | L | Op-Code | MRS | ILLEGAL | |

(3/3)

| Current state | \overline{CS} | \overline{RAS} | \overline{CA} | \overline{WE} | Address | Command | Action | Notes |
|--------------------------------------|-----------------|------------------|-----------------|-----------------|-----------|---------------------------|--|-------|
| Write recovering | H | X | X | X | X | DESL | Nop → Enter row active after t_{DPL} | |
| | L | H | H | H | X | NOP | Nop → Enter row active after t_{DPL} | |
| | L | H | H | L | X | BST | Nop → Enter row active after t_{DPL} | |
| | L | H | L | H | BA,CA,A10 | READ/READA | Start read, Determine AP | 8 |
| | L | H | L | L | BA,CA,A10 | WRIT/WRITA | New write, Determine AP | |
| | L | L | H | H | BA,RA | ACT | ILLEGAL | 3 |
| | L | L | H | L | BA,A10 | PRE/PALL | ILLEGAL | 3 |
| | L | L | L | H | X | PEF/SELF | ILLEGAL | |
| | L | L | L | L | Op-Code | MRS | ILLEGAL | |
| Write recovering with auto precharge | H | X | X | X | X | DESL | Nop → Enter precharge after t_{DPL} | |
| | L | H | H | H | X | NOP | Nop → Enter precharge after t_{DPL} | |
| | L | H | H | L | X | BST | Nop → Enter precharge after t_{DPL} | |
| | L | H | L | H | BA,CA,A10 | READ/READA | ILLEGAL | 3,8 |
| | L | H | L | L | BA,CA,A10 | WRIT/WRITA | ILLEGAL | 3 |
| | L | L | H | H | BA,RA | ACT | ILLEGAL | 3 |
| | L | L | H | L | BA,A10 | REF/PALL | ILLEGAL | 3 |
| | L | L | L | H | X | REF/SELF | ILLEGAL | |
| | L | L | L | L | Op-Code | MRS | ILLEGAL | |
| Refreshing | H | X | X | X | X | DESL | Nop → Enter idle after t_{RC} | |
| | L | H | H | X | X | NOP/BST | Nop → Enter idle after t_{RC} | |
| | L | H | L | X | X | READ/WRIT | ILLEGAL | |
| | L | L | H | X | X | ACT/PRE/PALL | ILLEGAL | |
| | L | L | L | X | X | REF/SELF/MRS | ILLEGAL | |
| Mode register accessing | H | X | X | X | X | DESL | Nop → Enter idle after 2 Clocks | |
| | L | H | H | H | X | NOP | Nop → Enter idle after 2 Clocks | |
| | L | H | H | L | X | BST | ILLEGAL | |
| | L | H | L | X | X | READ/WRITE | ILLEGAL | |
| | L | L | X | X | X | ACT/PRE/PALL/REF/SELF/MRS | ILLEGAL | |

- Note 1. All entries assume that CKE was active (High level) during the preceding clock cycle.
2. If both banks are idle, and CKE is inactive (Low level), the device will enter Power down mode.
All input buffers except CKE will be disabled.
3. Illegal to bank in specified states; Function may be legal in the bank indicated by Bank Address (BA), depending on the state of that bank.
4. If both banks are idle, and CKE is inactive (Low level), the device will enter Self refresh mode.
All input buffers except CKE will be disabled.
5. Illegal if t_{RCD} is not satisfied.
6. Illegal if t_{RAS} is not satisfied.
7. Must satisfy burst interrupt condition.
8. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
9. Must mask preceding data if t_{DPL} is not satisfied.
10. Illegal if t_{RRD} is not satisfied.

2.5 Command Truth Table for CKE Note 1

| Current state | $\overline{\text{CKE}}_{n-1}$ | $\overline{\text{RAS}}_n$ | $\overline{\text{CS}}$ | $\overline{\text{RAS}}$ | $\overline{\text{CAS}}$ | $\overline{\text{WE}}$ | Address | Action | Notes |
|-----------------------------------|-------------------------------|---------------------------|------------------------|-------------------------|-------------------------|------------------------|---------|--|-------|
| Self refresh (S.R.) | H | X | X | X | X | X | X | INVALID, CLK(n-1) would exit S.R. | |
| | L | H | H | X | X | X | X | S.R. Recovery | 2 |
| | L | H | L | H | H | X | X | S.R. Recovery | 2 |
| | L | H | L | H | L | X | X | ILLEGAL | 2 |
| | L | H | L | L | X | X | X | ILLEGAL | 2 |
| | L | L | X | X | X | X | X | Maintain S.R. | |
| Self refresh recovery | H | H | H | X | X | X | X | Idle after t_{RC} | |
| | H | H | L | H | H | X | X | Idle after t_{RC} | |
| | H | H | L | H | L | X | X | ILLEGAL | |
| | H | H | L | L | X | X | X | ILLEGAL | |
| | H | L | H | X | X | X | X | Begin clock suspend next cycle | 5 |
| | H | L | L | H | H | X | X | Begin clock suspend next cycle | 5 |
| | H | L | L | H | L | X | X | ILLEGAL | |
| | H | L | L | L | X | X | X | ILLEGAL | |
| | L | H | X | X | X | X | X | Exit clock suspend next cycle | 2 |
| | L | L | X | X | X | X | X | Maintain clock suspend | |
| Power down (P.D.) | H | X | X | X | X | X | | INVALID, CLK(n-1) would exit P.D. | |
| | L | H | X | X | X | X | X | EXIT P.D. → Idle | 2 |
| | L | L | X | X | X | X | X | Maintain power down mode | |
| Both banks idle | H | H | H | X | X | X | | Refer to operations in Operative Command Table | |
| | H | H | L | H | X | X | | Refer to operations in Operative Command Table | |
| | H | H | L | L | H | X | | Refer to operation in Operative Command Table | |
| | H | H | L | L | L | H | X | Refresh | |
| | H | H | L | L | L | L | Op-Code | Refer to operations in Operative Command Table | |
| | H | L | H | X | X | X | | Refer to operations in Operative Command Table | |
| | H | L | L | H | X | X | | Refer to operations in Operative Command Table | |
| | H | L | L | L | H | X | | Refer to operations in Operative Command Table | |
| | H | L | L | L | L | H | X | Self refresh | 3 |
| | H | L | L | L | L | L | Op-Code | Refer to operations in Operative Command Table | |
| | L | X | X | X | X | X | X | Power down | 3 |
| Any state other than listed above | H | H | X | X | X | X | X | Refer to operations in Operative Command Table | |
| | H | L | X | X | X | X | X | Begin clock suspend next cycle | 4 |
| | L | H | X | X | X | X | X | Exit clock suspend next cycle | |
| | L | L | X | X | X | X | X | Maintain clock suspend | |

Note 1. H : Hight level, L : low level, X : High or low level(Don't care).

2. CKE Low to High transition will re-enable CLK and other inputs asynchronously. A minimum setup time must be satisfied before any command other than EXIT.

3. Power down and Self refresh can be entered only from the both banks idle state.

4. Must be legal command as defined in Operative Command Table.

5. Illegal if t_{SREX} is not satisfied.

3. Initialization

The synchronous DRAM is initialized in the power on sequence. Once power has been applied, a 100 μ s minimum delay is needed in which stable power and input signals are maintained. During this delay, CKE and DQM recommend to be held high.

After the 100 μ s delay, both banks must be precharged using the precharge command. Once precharge is completed and the minimum t_{RP} is satisfied, the mode register can be programmed.

Minimum two CBR refresh commands must be performed before or after the mode register set command.

4. Programming the Mode Register

The mode register is programmed by the mode register set command using address bits A11 through A0 as data inputs. The register retains data until it is reprogrammed or until the device loses power.

The mode register has four fields;

| | |
|--------------|------------------|
| Options | : A11 through A7 |
| CAS latency | : A6 through A4 |
| Wrap type | : A3 |
| Burst length | : A2 through A0 |

Following mode register programming, no command can be asserted before at least two clock cycles have elapsed.

CAS Latency

CAS latency is the most critical parameter to be set. It tells the device how many clocks must elapse before the data will be available. The SDRAM is capable of reconfiguring its internal architecture based on the value of CAS latency.

The value is determined by the frequency of the clock and the speed grade of the device. The value can be programmed as 2 or 3.

Burst Length

Burst Length is the number of words that will be output or input in read or write cycle. After a read burst is completed, the output bus will become high impedance.

The burst length is programmable as 1,2,4,8 or full page.

Wrap Type (Burst Sequence)

The wrap type specifies the order in which the burst data will be addressed. The order is programmable as either "Sequential" or "Interleave". The method chosen will depend on the type of CPU in the system.

Some microprocessor cache systems are optimized for sequential addressing and others for interleaved addressing. Both sequences support bursts of 1,2,4 and 8. Only the sequential burst supports the full-page length.

5.Mode Register

| 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | | | | | | | |

Reserved Test Set

| 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|---|---|---|--------|---|----|----|---|---|---|
| x | x | 1 | 0 | 0 | LTMODE | | WT | BL | | | |

Burst Read and Single Write

X=Don't care

| 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|---|---|---|--------|---|----|----|---|---|---|
| x | x | 0 | 0 | 0 | LTMODE | | WT | BL | | | |

Mode Register Set

| Burst length | Bits2-0 | WT=0 | WT=1 |
|--------------|---------|-----------|------|
| | 000 | 1 | 1 |
| | 001 | 2 | 2 |
| | 010 | 4 | 4 |
| | 011 | 8 | 8 |
| | 100 | R | R |
| | 101 | R | R |
| | 110 | R | R |
| | 111 | Full page | R |

| Wrap type | 0 | Sequential |
|-----------|---|------------|
| | 1 | Interleave |

| Latency mode | Bits6-4 | CAS latency |
|--------------|---------|-------------|
| | 000 | R |
| | 001 | R |
| | 010 | 2 |
| | 011 | 3 |
| | 100 | R |
| | 101 | R |
| | 110 | R |
| | 111 | R |

Remark R:Reserved

5.1 Burst Length and Sequence

(Burst of Two)

| Starting Address (column address A0, binary) | Sequential Addressing Sequence (decimal) | Interleave Addressing Sequence(decimal) |
|---|---|--|
| 0 | 0,1 | 0,1 |
| 1 | 1,0 | 1,0 |

(Burst of Four)

| Starting Address (column address A1-A0, binary) | Sequential Addressing Sequence (decimal) | Interleave Addressing Sequence(decimal) |
|--|---|--|
| 00 | 0,1,2,3 | 0,1,2,3 |
| 01 | 1,2,3,0 | 1,0,3,2 |
| 10 | 2,3,0,1 | 2,3,0,1 |
| 11 | 3,0,1,2 | 3,2,1,0 |

(Burst of Eight)

| Starting Address (column address A2-A0, binary) | Sequential Addressing Sequence (decimal) | Interleave Addressing Sequence(decimal) |
|--|---|--|
| 000 | 0,1,2,3,4,5,6,7 | 0,1,2,3,4,5,6,7 |
| 001 | 1,2,3,4,5,6,7,0 | 1,0,3,2,5,4,7,6 |
| 010 | 2,3,4,5,6,7,0,1 | 2,3,0,1,6,7,4,5 |
| 011 | 3,4,5,6,7,0,1,2 | 3,2,1,0,7,6,5,4 |
| 100 | 4,5,6,7,0,1,2,3 | 4,5,6,7,0,1,2,3 |
| 101 | 5,6,7,0,1,2,3,4 | 5,4,7,6,1,0,3,2 |
| 110 | 6,7,0,1,2,3,4,5 | 6,7,4,5,2,3,0,1 |
| 111 | 7,0,1,2,3,4,5,6 | 7,6,5,4,3,2,1,0 |

Full page burst is an extension of the above tables of sequential addressing, with the length being 512/256 words for 2Mx8/1Mx16 devices, respectively.

6.Address Bits of Bank-Select and Precharge

| | | | | | | | | | | | | | | |
|--------------------|----|----|----|----|----|----|----|----|----|----|-----|-----|---|----------------------------------|
| Row | A0 | A1 | A2 | A3 | A4 | A5 | A6 | A7 | A8 | A9 | A10 | A11 | 0 | Select Bank A "Activate" command |
| (Activate command) | | | | | | | | | | | | | 1 | Select Bank B "Activate" command |

| | | | | | | | | | | | | | | | |
|-------------|----|----|----|----|----|----|----|----|----|----|-----|-----|-----|-----|---------------------|
| Row | A0 | A1 | A2 | A3 | A4 | A5 | A6 | A7 | A8 | A9 | A10 | A11 | A10 | A11 | Result |
| (Precharge) | | | | | | | | | | | | | 0 | 0 | Precharge Bank A |
| | | | | | | | | | | | | | 0 | 1 | Precharge Bank B |
| | | | | | | | | | | | | | 1 | x | Precharge All Banks |

x:Don't care

| | | | | | | | | | | | | | | |
|--|--|--|--|--|--|--|--|--|--|--|--|--|---|--|
| | | | | | | | | | | | | | 0 | Disables Auto-Precharge (End of Burst) |
| | | | | | | | | | | | | | 1 | Enables Auto-Precharge (End of Burst) |

| | | | | | | | | | | | | | | |
|---------------|----|----|----|----|----|----|----|----|----|----|-----|-----|---|---------------------------------------|
| Col. | A0 | A1 | A2 | A3 | A4 | A5 | A6 | A7 | A8 | A9 | A10 | A11 | 0 | Enable Read/Write commands for Bank A |
| (CAS strobes) | | | | | | | | | | | | | 1 | Enable Read/Write commands for Bank B |

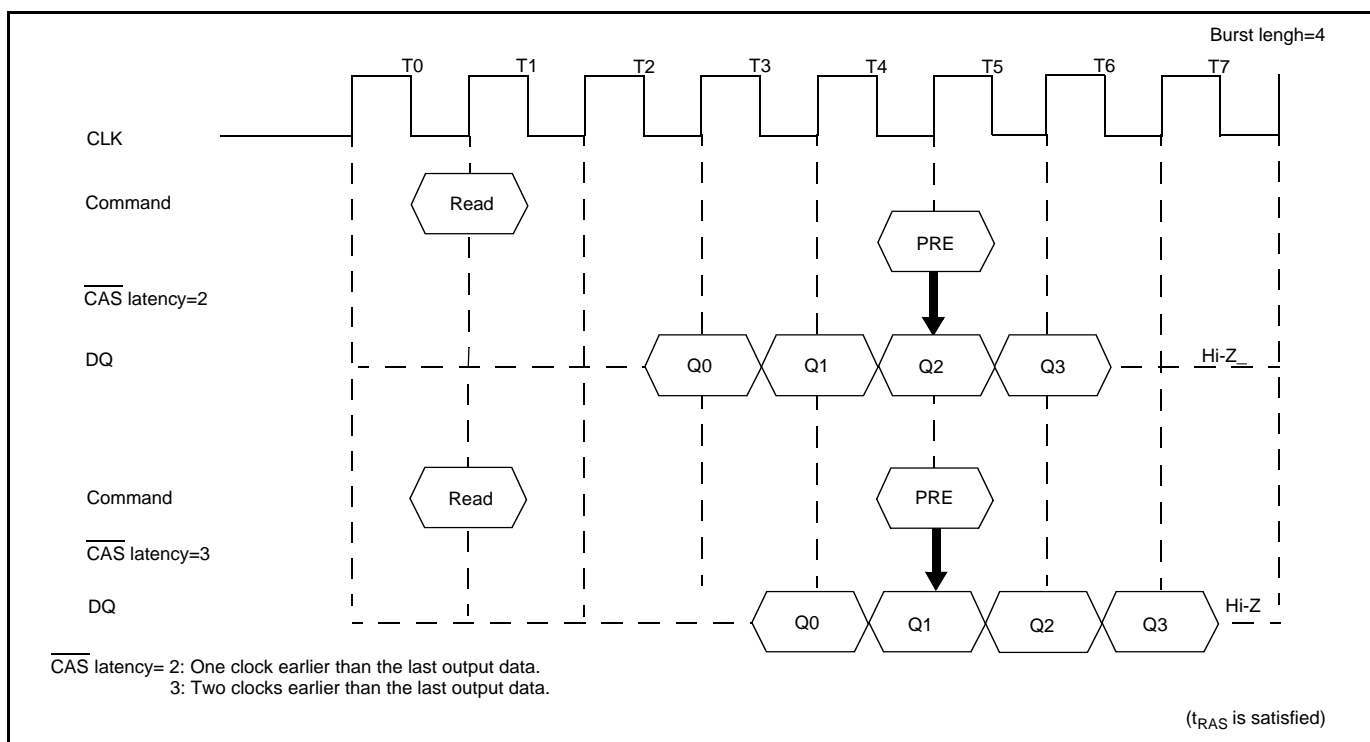
7.PRECHARGE

The PRECHARGE command can be asserted anytime after $t_{RAS(min)}$ is satisfied.

Soon after the PRECHARGE command is asserted, PRECHARGE operation is performed. The synchronous DRAM enters the idle state after $t_{RP(min)}$ is satisfied. The parameter t_{RP} is the time required to perform the PRECHARGE.

The earliest timing in a READ cycle that a PRECHARGE command can be asserted without losing any data in the burst is as followed.

PRECHARGE



In order to write all data to the memory cell correctly, the asynchronous parameter " t_{DPL} " must be satisfied.

The $t_{DPL(min)}$ specification defines the earliest time that a PRECHARGE command can be asserted after a WRITE cycle. The minimum number of clocks are calculated by dividing $t_{DPL(min)}$ by the clock cycle time.

In summary, the PRECHARGE command can be asserted relative to the reference clock of the last valid data. In the following table, minus means clocks before the reference, plus means time after the reference.

| CAS latency | READ | WRITE |
|-------------|------|-----------------|
| 2 | -1 | $+t_{DPL(min)}$ |
| 3 | -2 | $+t_{DPL(min)}$ |

8.AUTO PRECHARGE

During a READ or WRITE command cycle, A10 controls whether AUTO PRECHARGE is selected. If A10 is high in the READ or WRITE command (READ with AUTO PRECHARGE command or WRITE with AUTO PRECHARGE command), AUTO PRECHARGE is selected and precharging begins automatically after the burst access.

In the WRITE cycle, $t_{DAL(min.)}$ must be satisfied to assert the next active command to the bank being pre-charged.

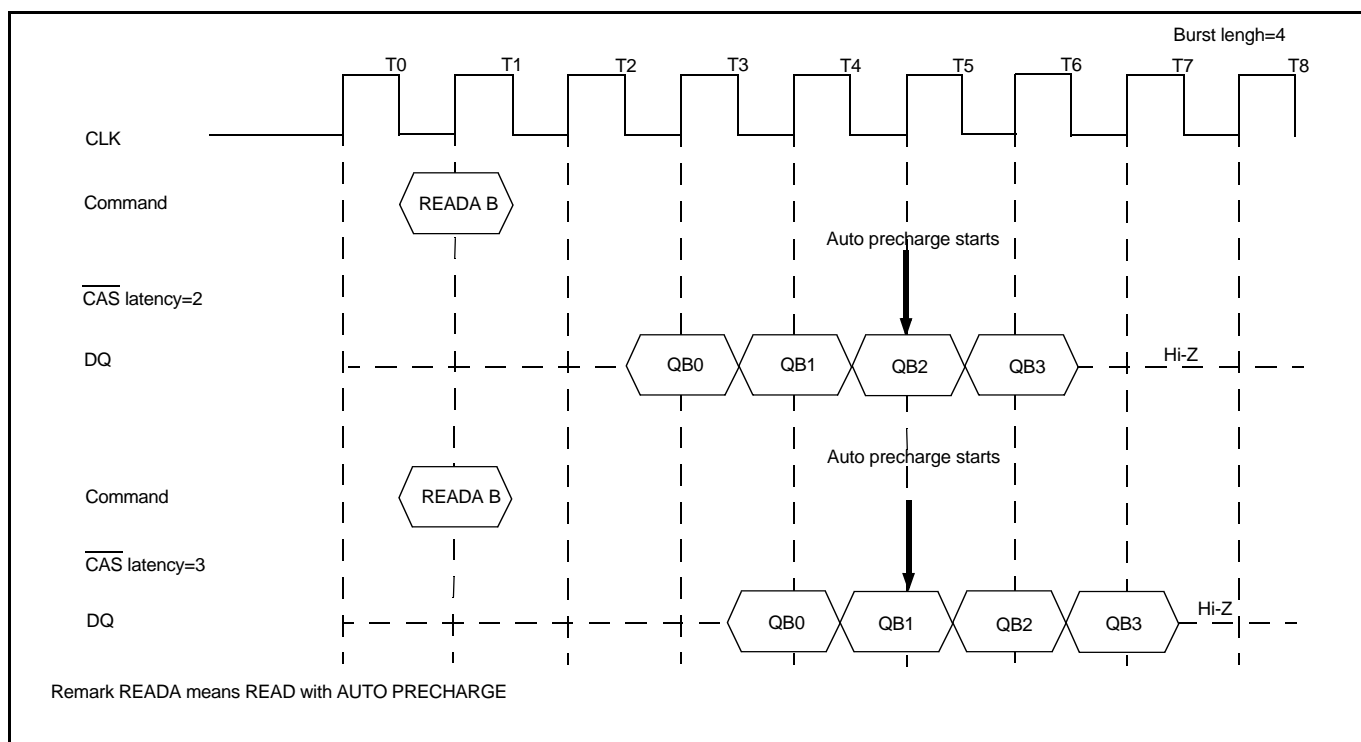
When using AUTO PRECHARGE in the READ cycle, knowing when the PRECHARGE starts is important because the t_{RAS} must be satisfied. Once AUTO PRECHARGE has started, an active command to the bank can be asserted after $t_{RP(min.)}$ has been satisfied.

The timing at which the AUTO PRECHARGE cycle begins depends both on the \overline{CAS} latency programmed into the mode register and on whether the cycle is READ or WRITE.

8.1 READ with AUTO PRECHARGE

During a READA cycle, the AUTO PRECHARGE begins one clock earlier (\overline{CAS} latency of 2) or two clocks earlier (\overline{CAS} latency of 3) than the last data word output.

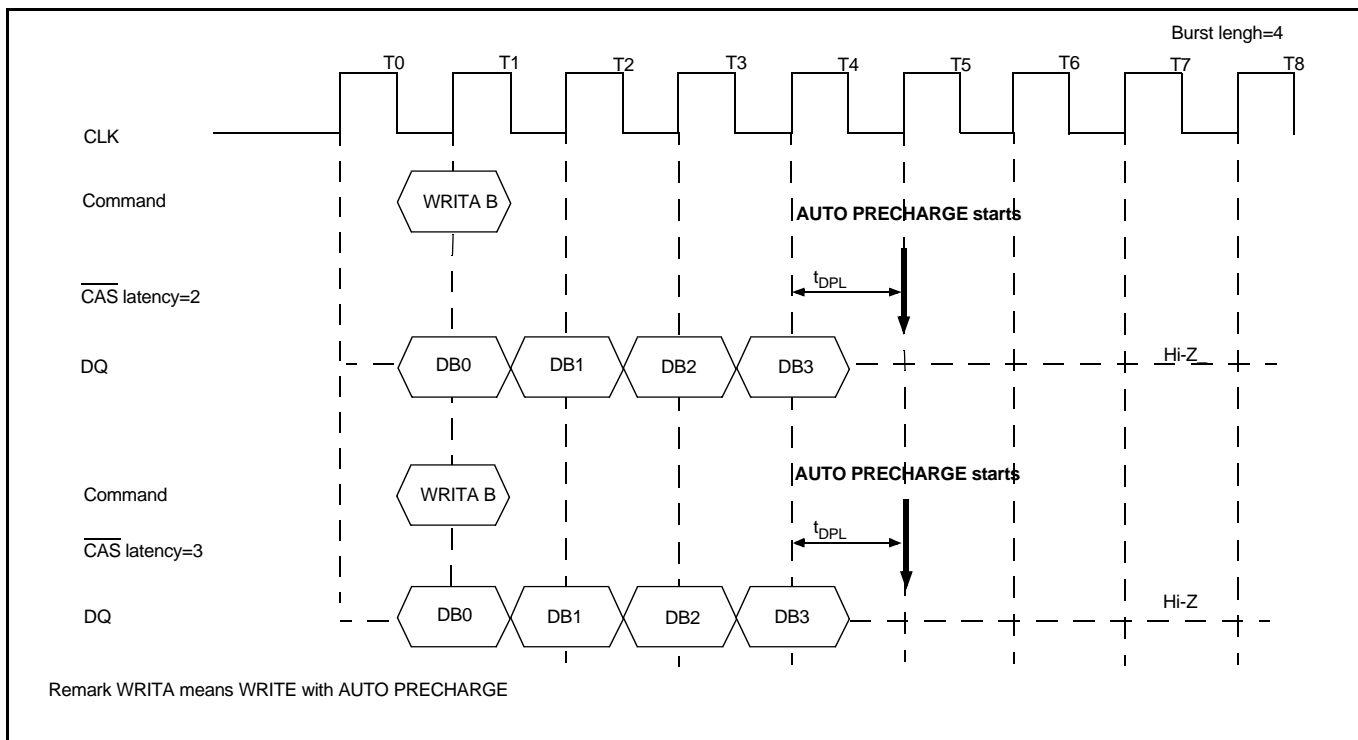
READ with AUTO PRECHARGE



8.2 WRITE with AUTO PRECHARGE

During a WRITA cycle, the AUTO PRECHARGE starts at $t_{DPL(min.)}$ after the last data word input to the device

WRITE with AUTO PRECHARGE



In summary, the auto precharge cycle begins relative to a reference clock that indicates the last data word is valid.

In the table below, minus means clocks before the reference; plus means clocks after the reference.

| CAS latency | READ | WRITE |
|-------------|------|------------------|
| 2 | -1 | $+t_{DPL(min.)}$ |
| 3 | -2 | $+t_{DPL(min)}$ |

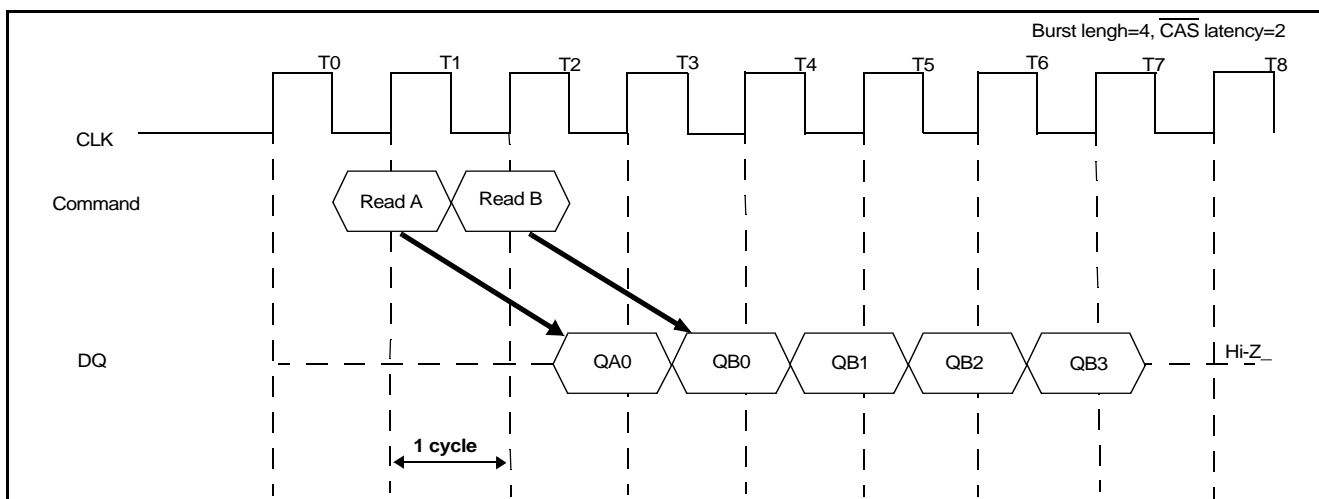
9.READ/WRITE Command Interval

9.1 READ to READ command interval

When a new READ command is asserted during a READ cycle, it will be effective after the CAS latency, even if the previous READ operation has not completed. READ will be interrupted by another READ.

A READ command can be asserted in every clock without restriction.

READ to READ Command Interval

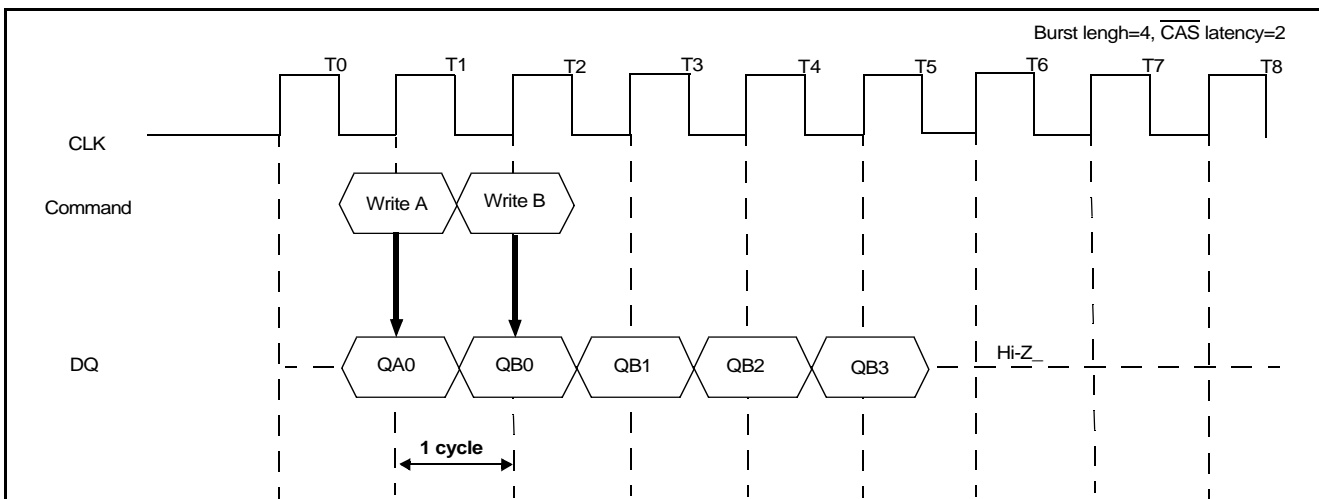


9.2 WRITE to WRITE Command Interval

When a new WRITE command is asserted during a WRITE cycle, the previous burst will be terminated and the new burst will begin with the new WRITE command. WRITE will be interrupted by another WRITE.

A WRITE command can be asserted in every clock without restriction.

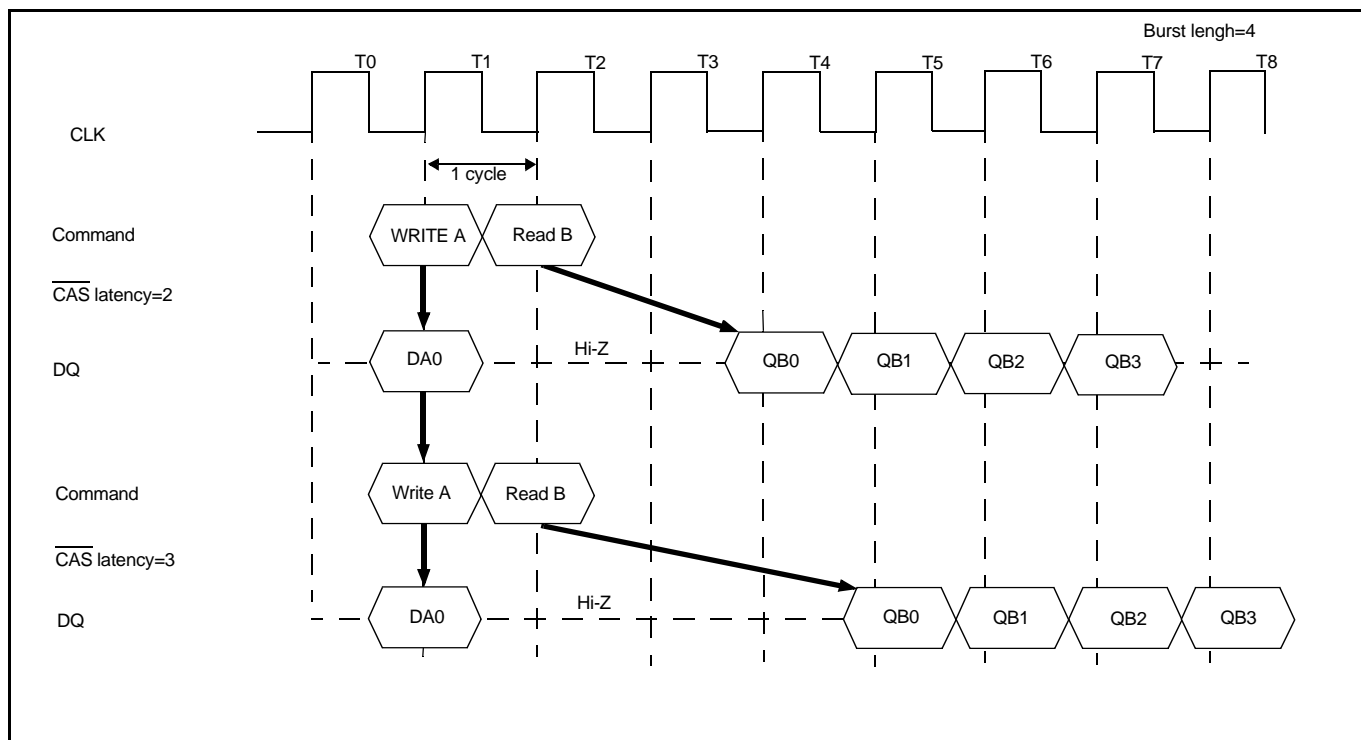
WRITE to WRITE Command Interval



9.3 WRITE to READ Command Interval

The WRITE command to READ command interval is a minimum of 1 cycle. Only the WRITE data preceding the READ command will be written. The data bus must be in high-impedance at least one cycle prior to the first D_{OUT}.

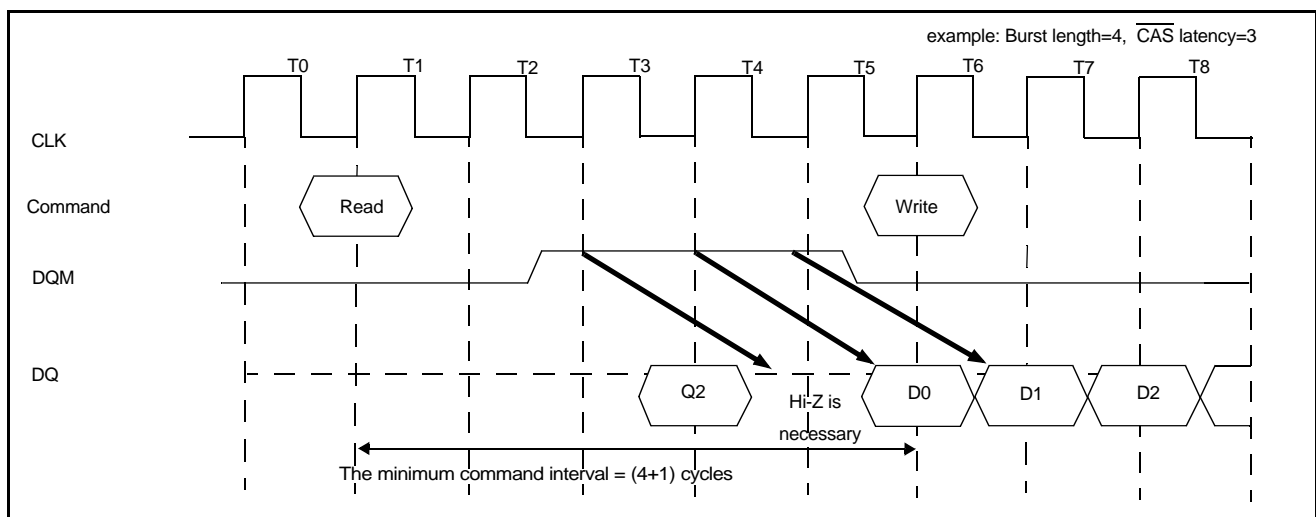
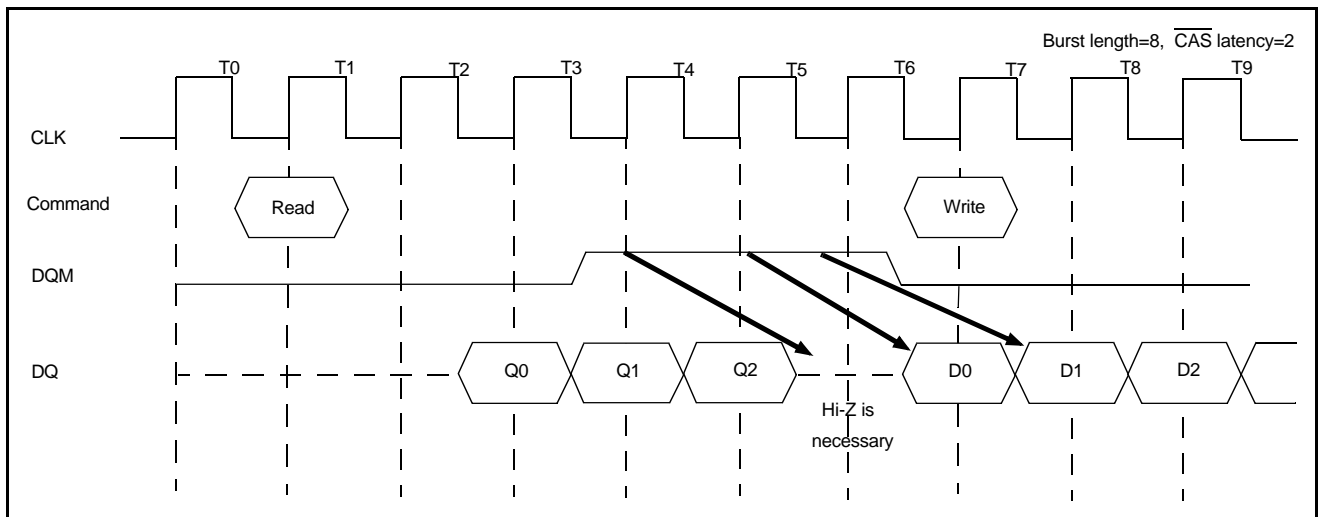
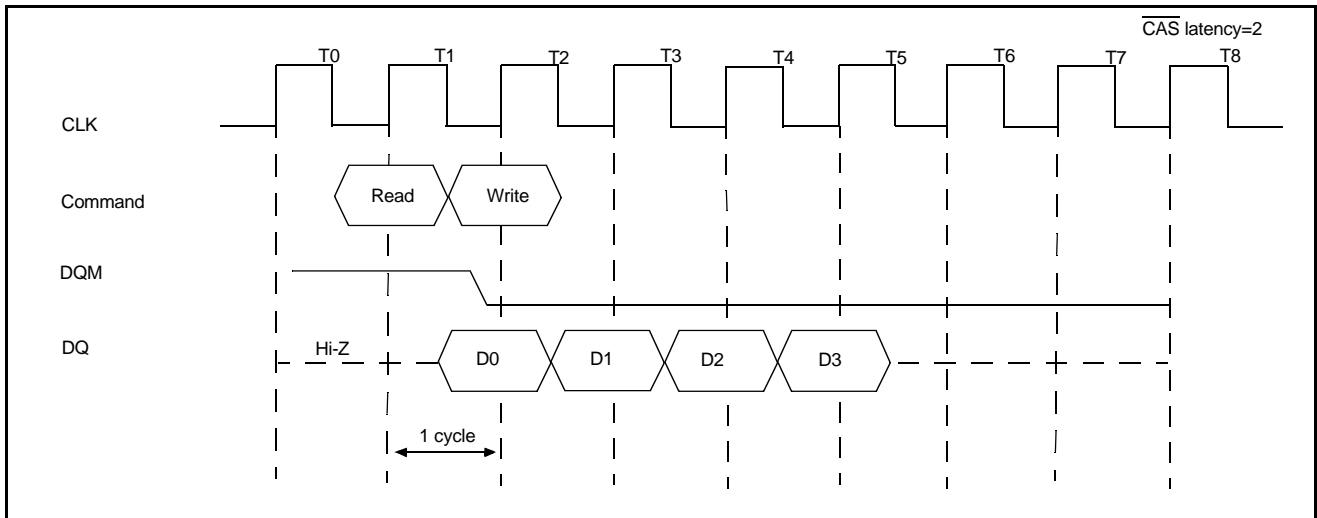
WRITE to READ Command Interval



9.4 READ to WRITE Command Interval

During READ cycle, READ can be interrupted by WRITE. The data bus must be in high-impedance using DQM before the WRITE command. DQM must be high at least 3 clocks prior to the WRITE command. This restriction is necessary to avoid a data bus conflict.

READ to WRITE Command Interval



10.BURST TERMINATION

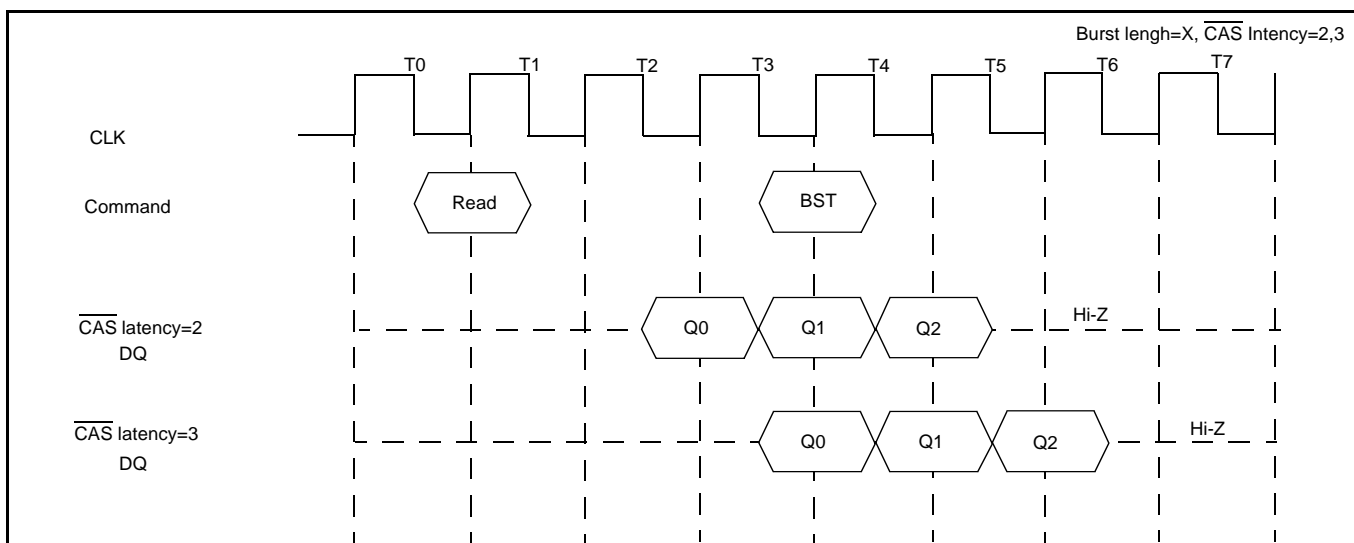
There are two methods to terminate a BURST operation other than using a READ or a WRITE command. One is the BURST STOP command and the other is the PRECHARGE command.

10.1 BURST STOP Command

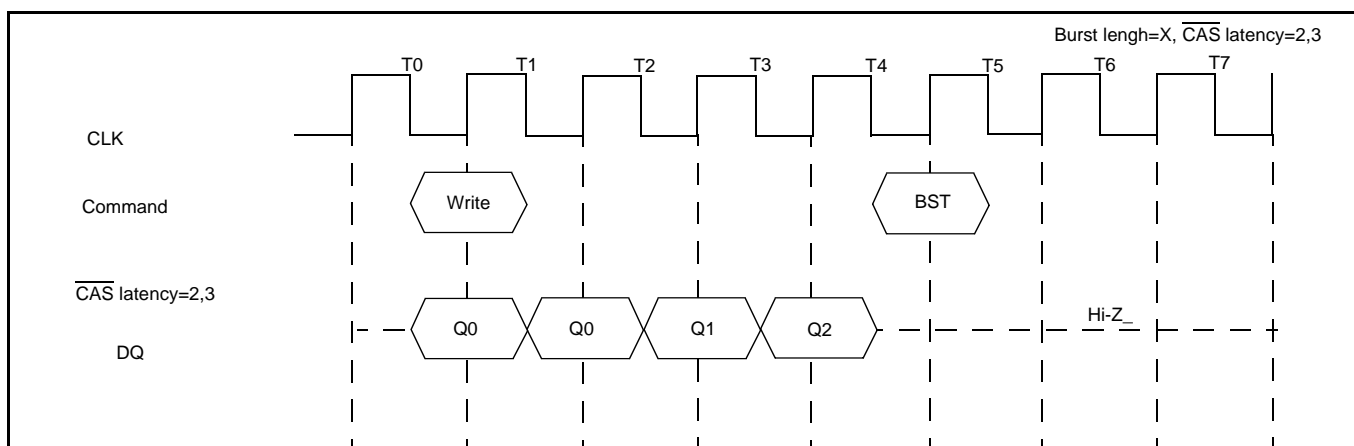
During a READ BURST, when the BURST STOP command is asserted, the BURST READ outputs are terminated and the data bus goes to high-impedance after the $\overline{\text{CAS}}$ latency from the BURST STOP command.

During a WRITE BURST, when the BURST STOP command is asserted, any data provided at that cycle will not be written. The BURST WRITE is effectively terminated and no further data can be written until a new WRITE command is asserted.

Burst Termination



Remark BST: Burst stop command



Remark BST: Burst stop command

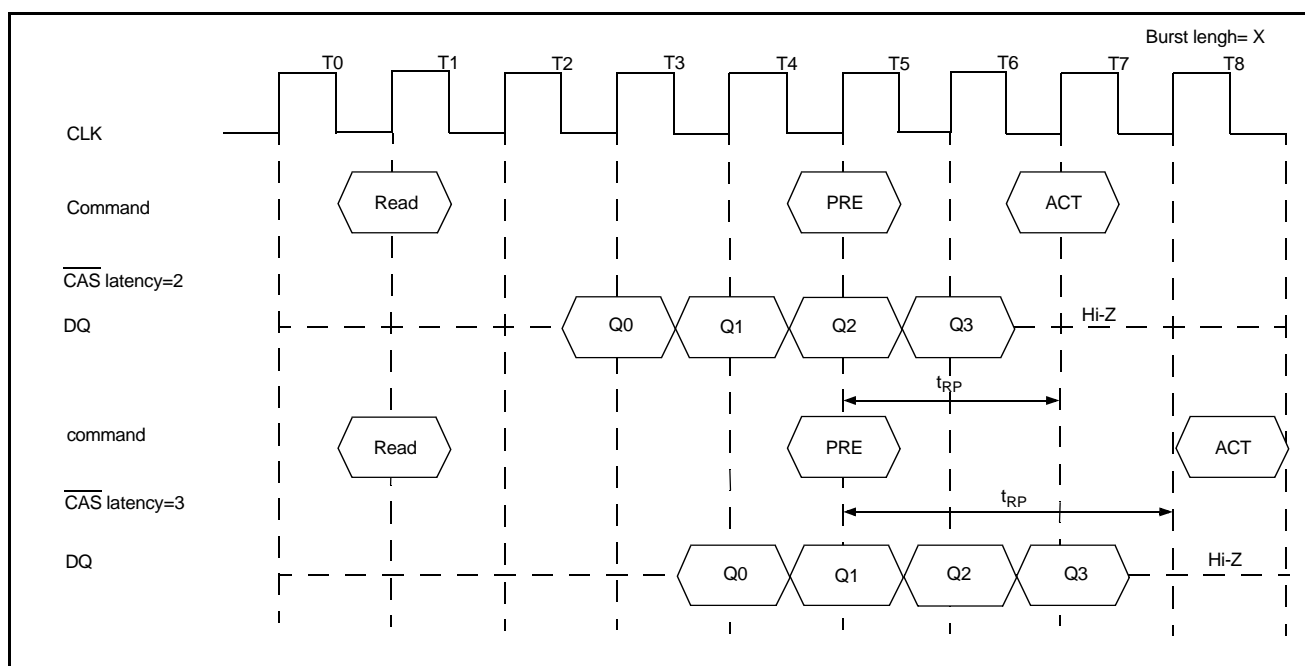
10.2 PRECHARGE TERMINATION

10.2.1 PRECHARGE TERMINATION in READ Cycle

During a READ cycle, the BURST READ operation can be terminated by a PRECHARGE command. When the PRECHARGE command is asserted, the BURST READ operation is terminated and PRECHARGE starts.

Read data will remain valid until one clock ($\overline{\text{CAS}}$ latency of 2) or two clocks ($\overline{\text{CAS}}$ latency of 3) after the PRECHARGE command and the same bank can be activated again after $t_{RP(\text{min})}$ from the PRECHARGE command.

PRECHARGE TERMINATION in READ Cycle



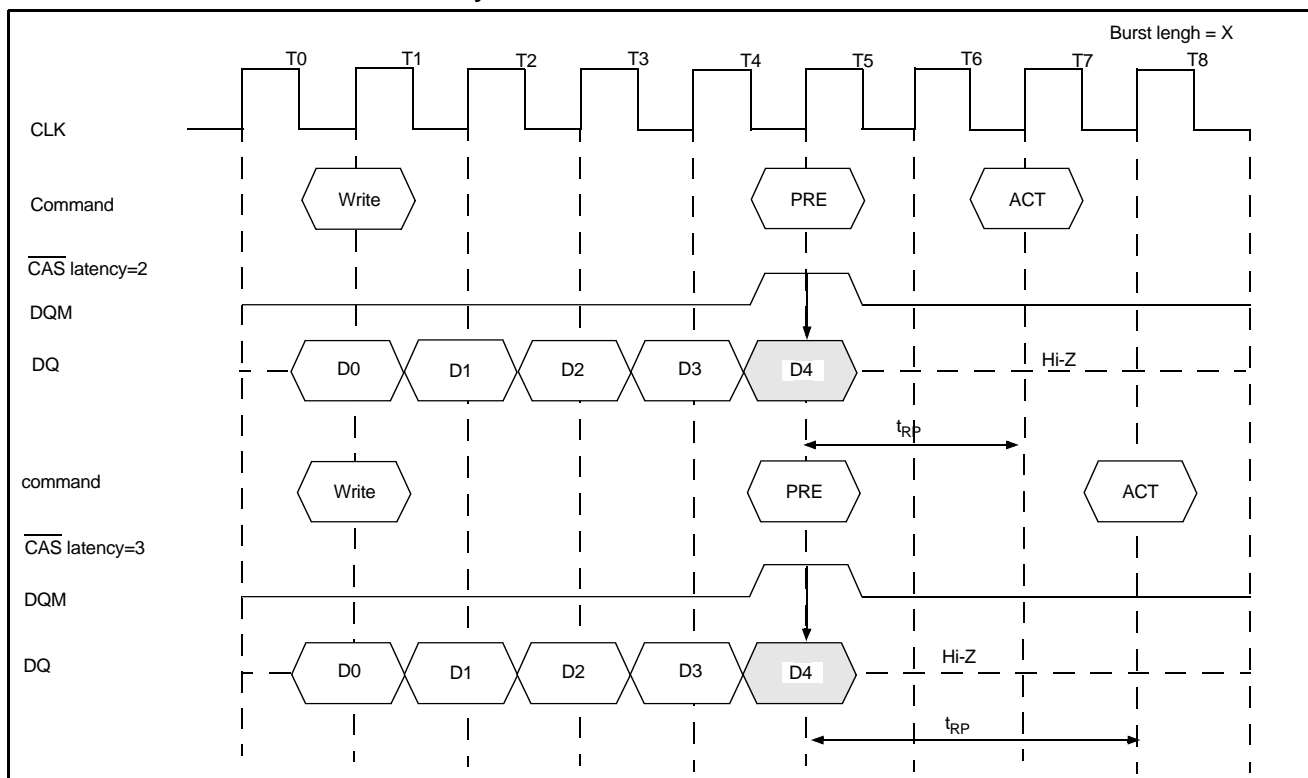
10.2.2 PRECHARGE TERMINATION in WRITE Cycle

During a WRITE cycle, the BURST WRITE operation can be terminated by a PRECHARGE command. when the PRECHARGE command is asserted, the BURST WRITE operation is immediately terminated and PRECHARGE starts.

The same bank can be activated again after $t_{RP}(\text{min.})$ from the PRECHARGE command. The DQM must be high to mask invalid data in.

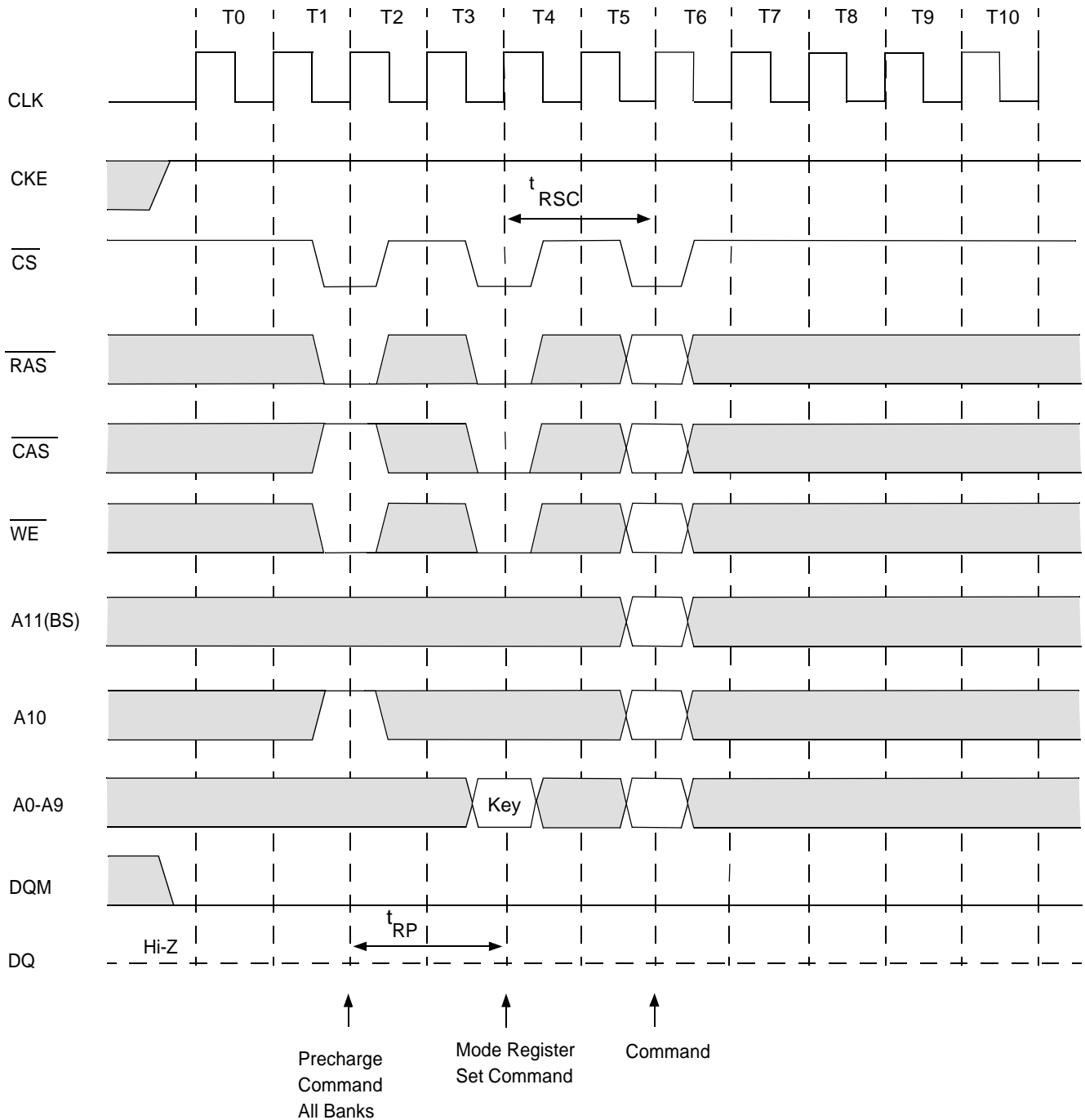
When CAS latency is 2 or 3, the data written prior to the PRECHARGE command will be correctly stored. However, invalid data may be written at the same clock as the PRECHARGE command. To prevent this from happening, DQM must be high at the same clock as the PRECHARGE command. This will mask the invalid data.

PRECHARGE TERMINATION in WRITE Cycle33



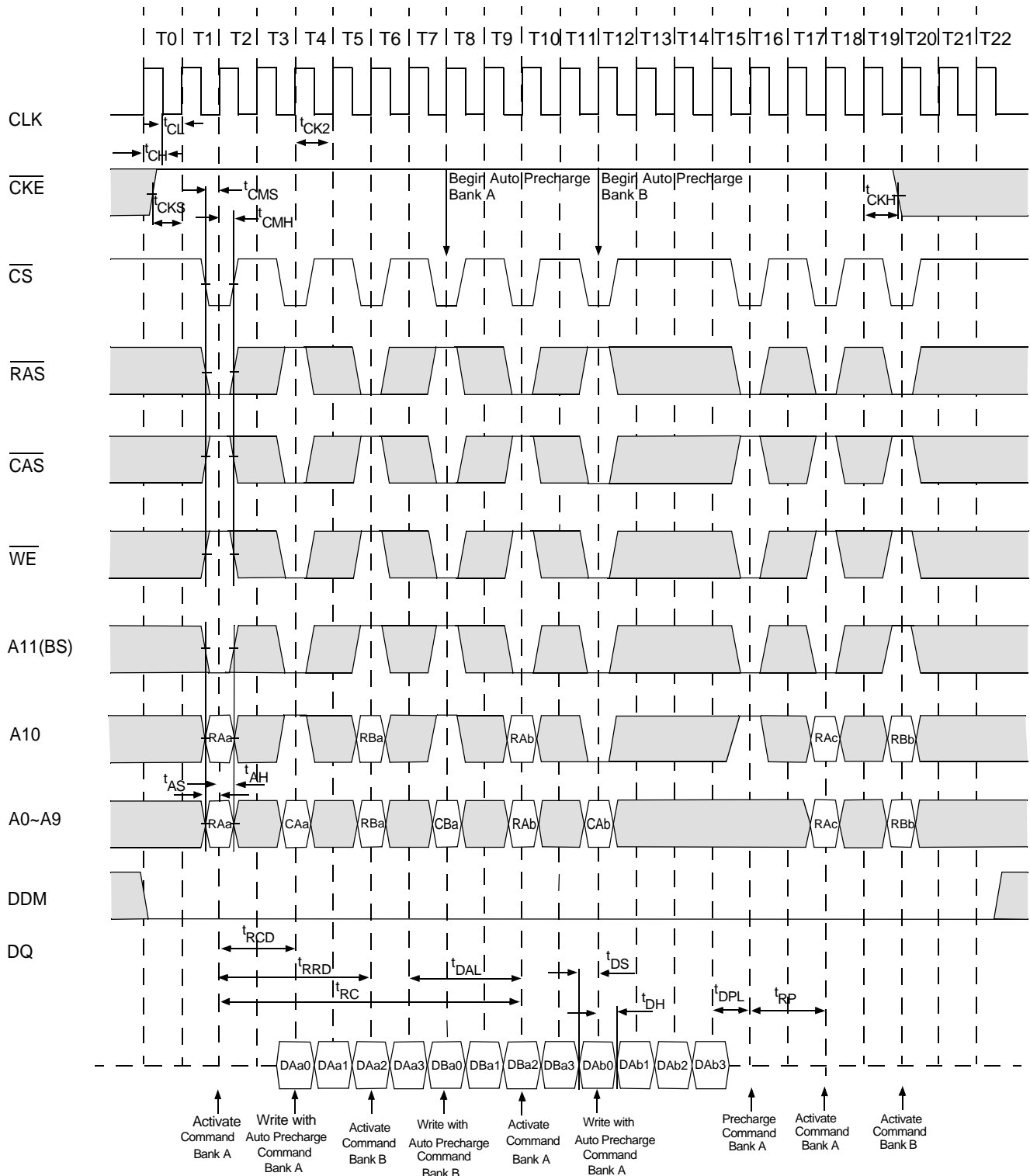
Timing Diagram

Mode Register Set



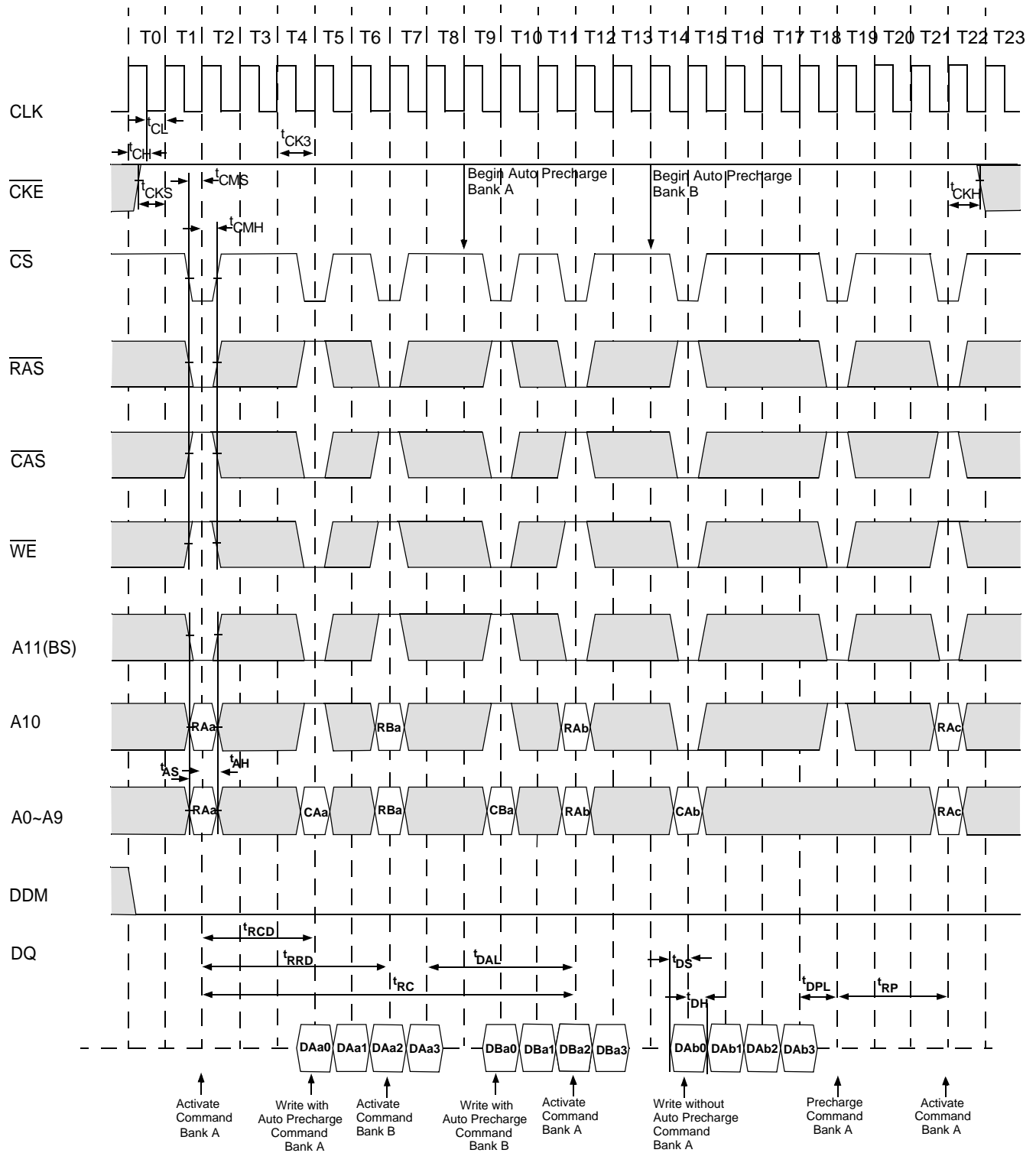
AC Parameters for Write Timing (1 of 2)

Burst Length=4, CAS Latency=2



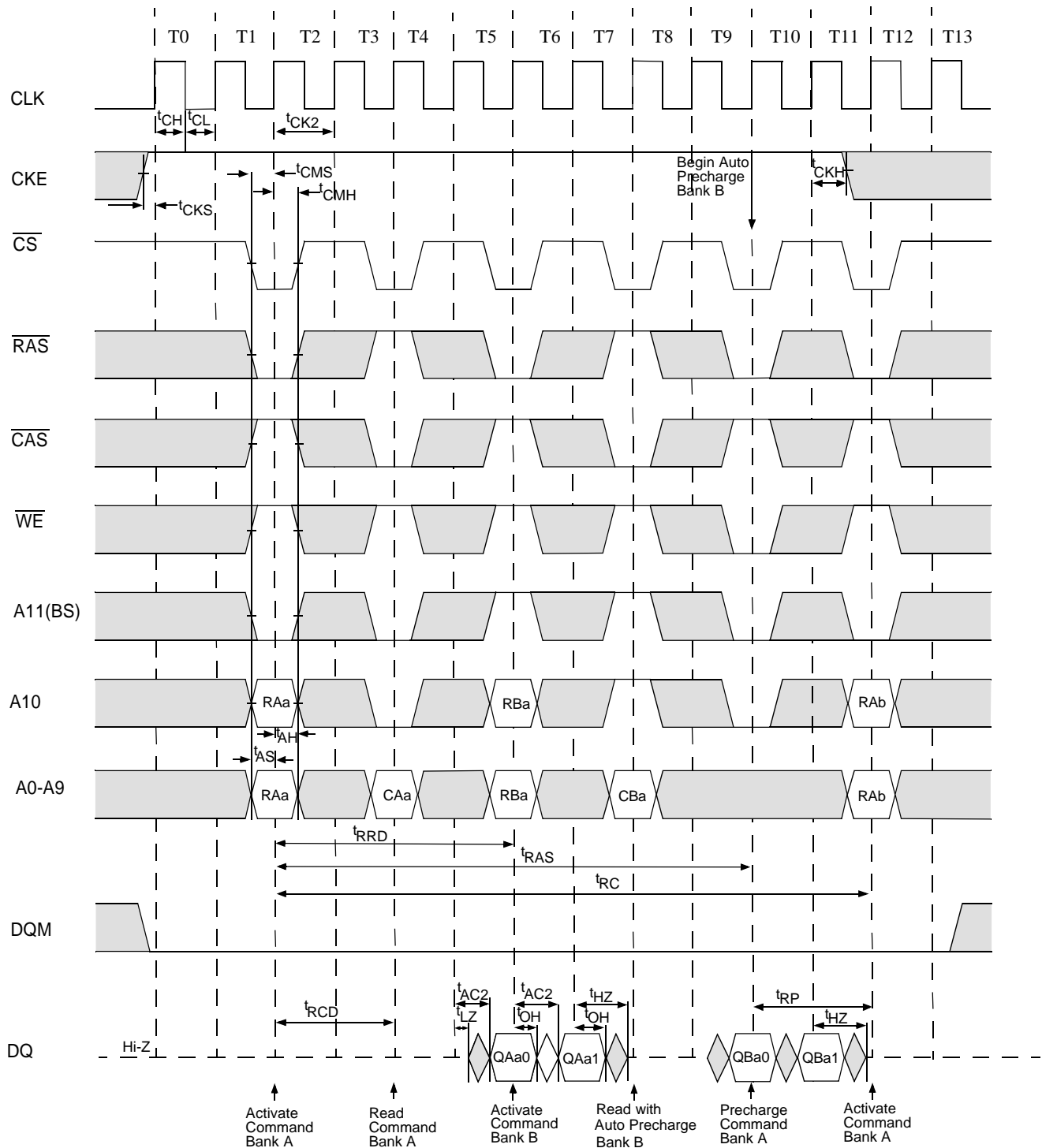
AC Parameters for Write Timing (2 of 2)

Burst Length=4, $\overline{\text{CAS}}$ Latency=3



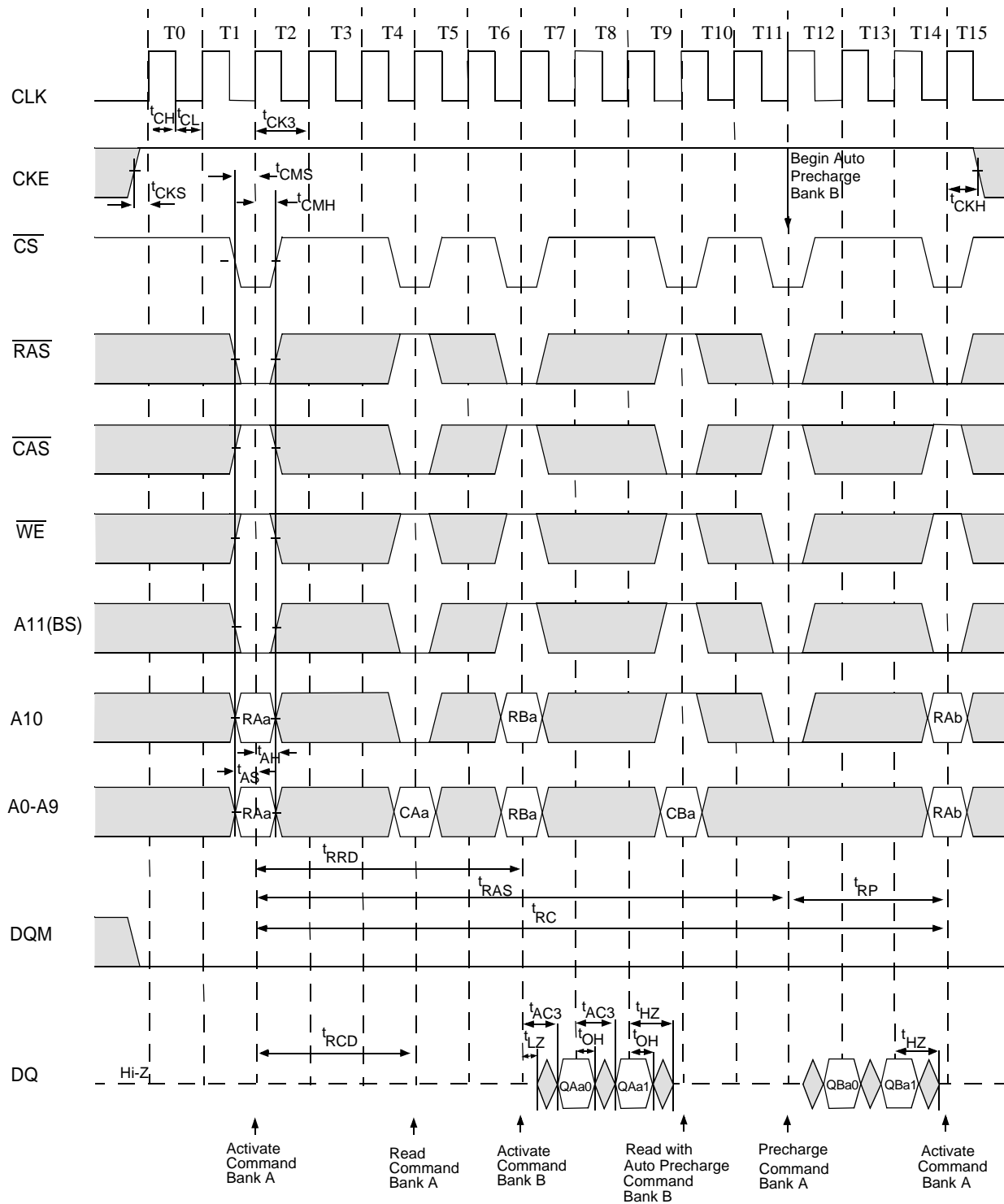
AC Parameters for Read Timing (1 of 2)

Burst Length=2, $\overline{\text{CAS}}$ Latency=2

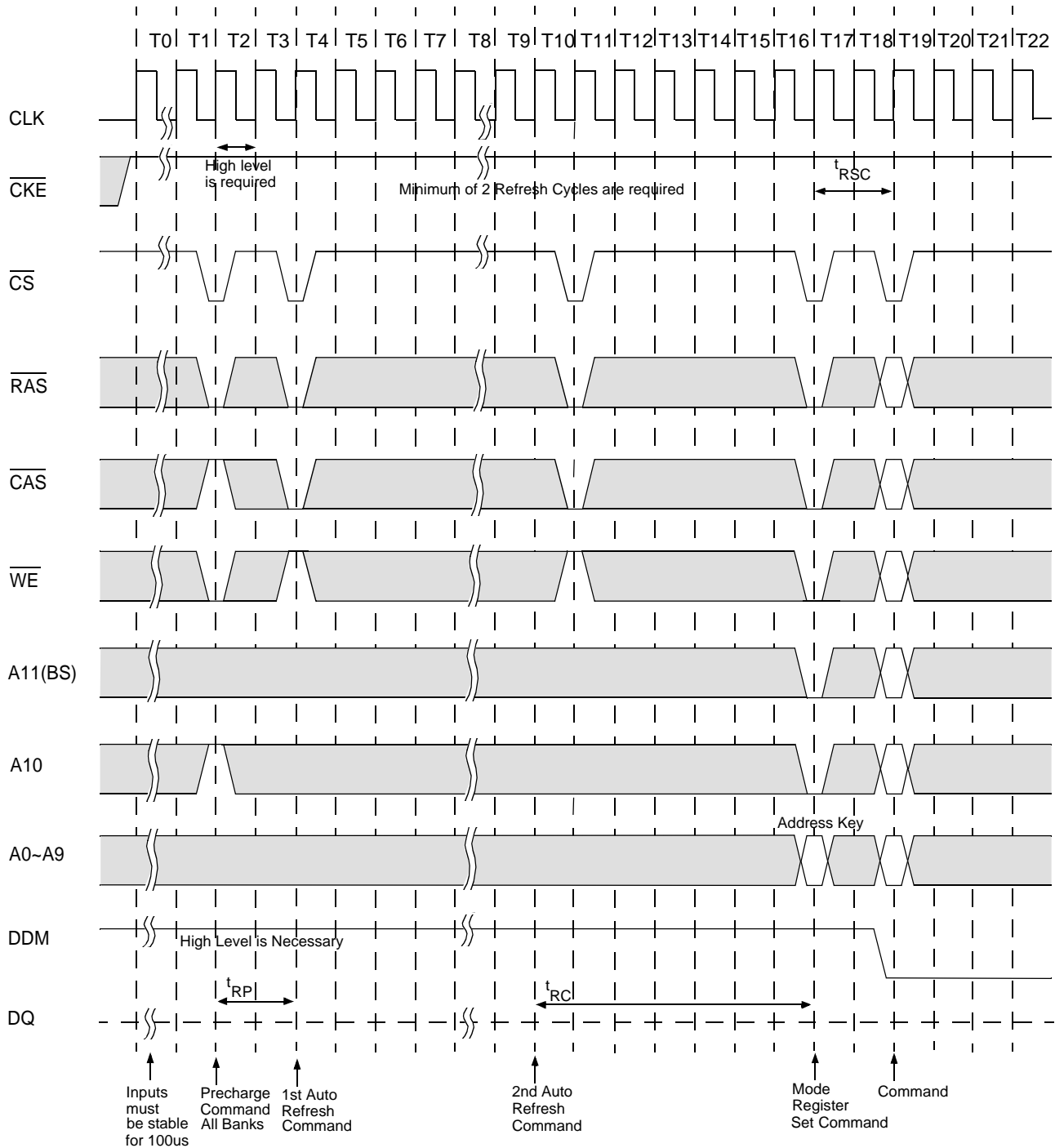


AC Parameters for Read Timing (2 of 2)

Burst Length=2, $\overline{\text{CAS}}$ Latency=3

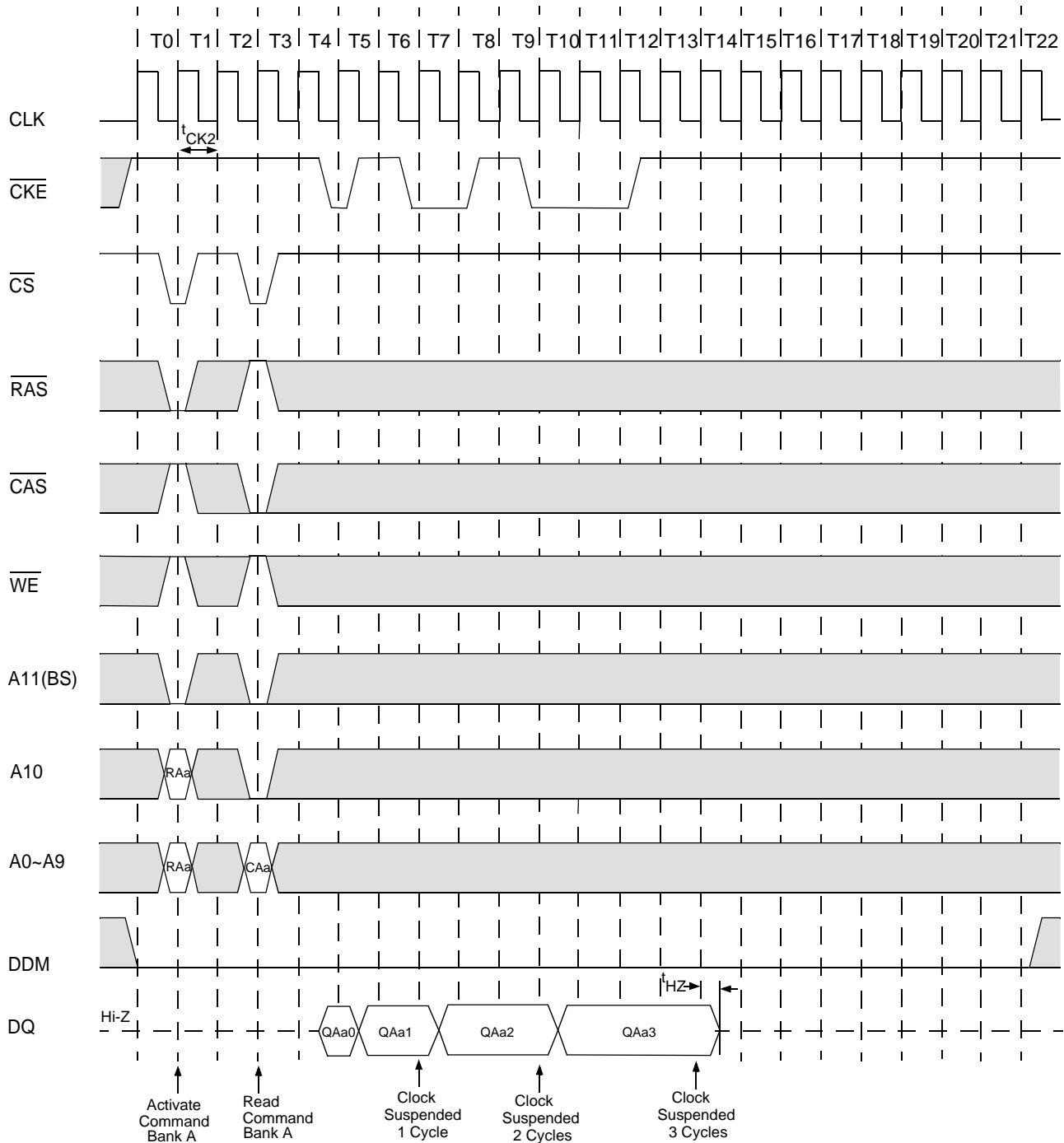


Power on Sequence and Auto Refresh (CBR)



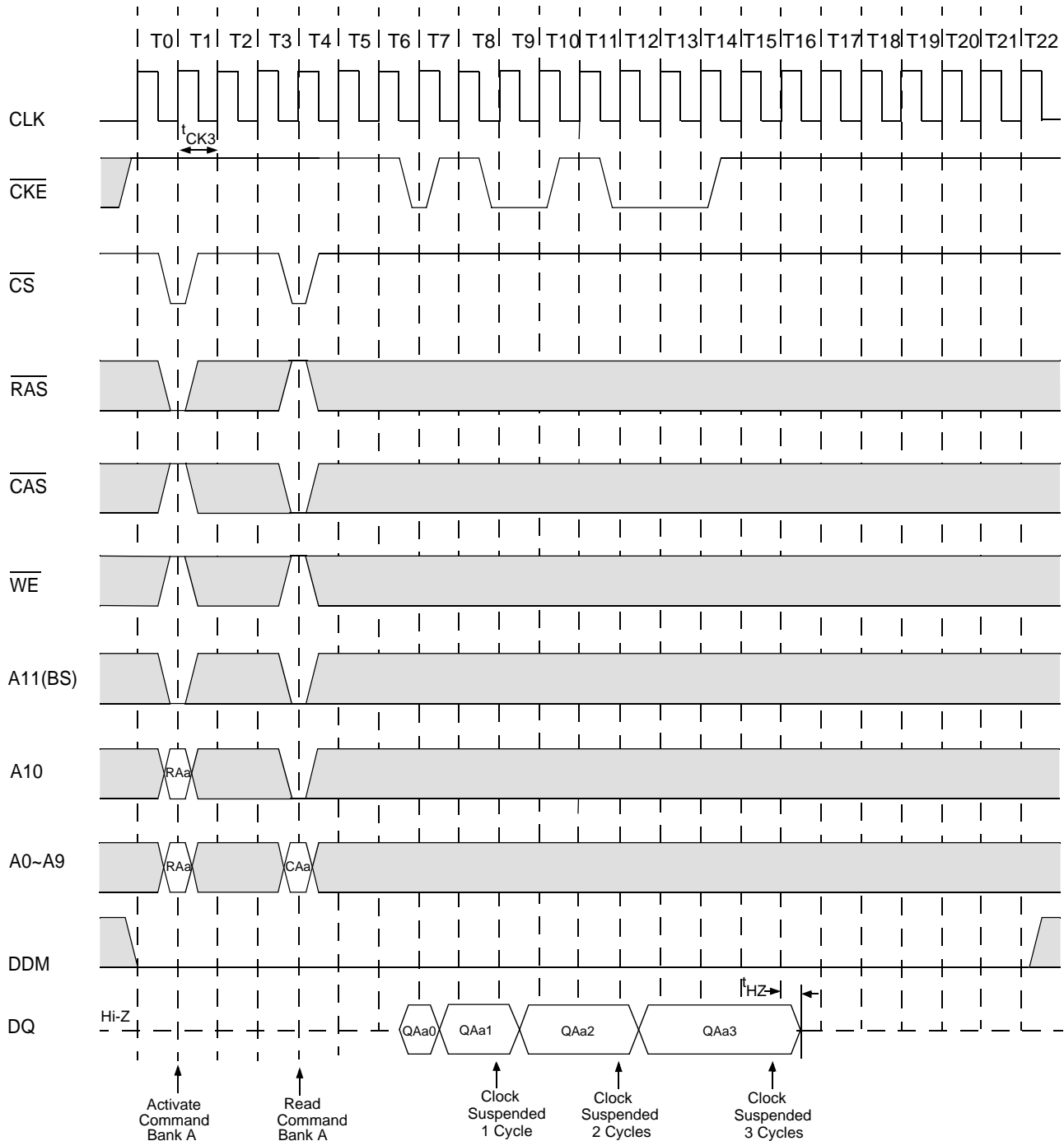
Clock Suspension During Burst Read (Using CKE) (1 of 2)

Burst Length=4, $\overline{\text{CAS}}$ Latency=2



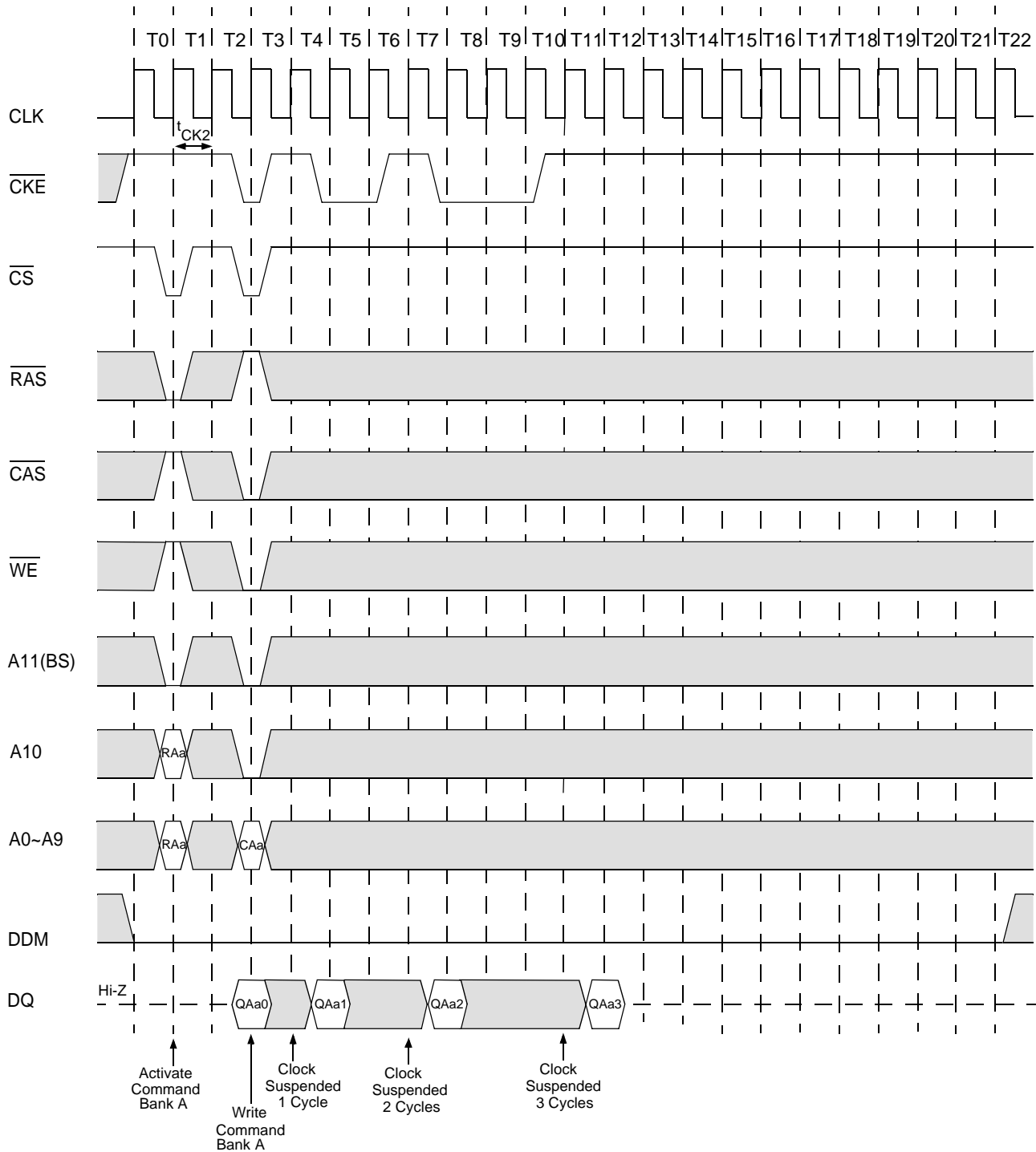
Clock Suspension During Burst Read (Using CKE) (2 of 2)

Burst Length=4, $\overline{\text{CAS}}$ Latency=3



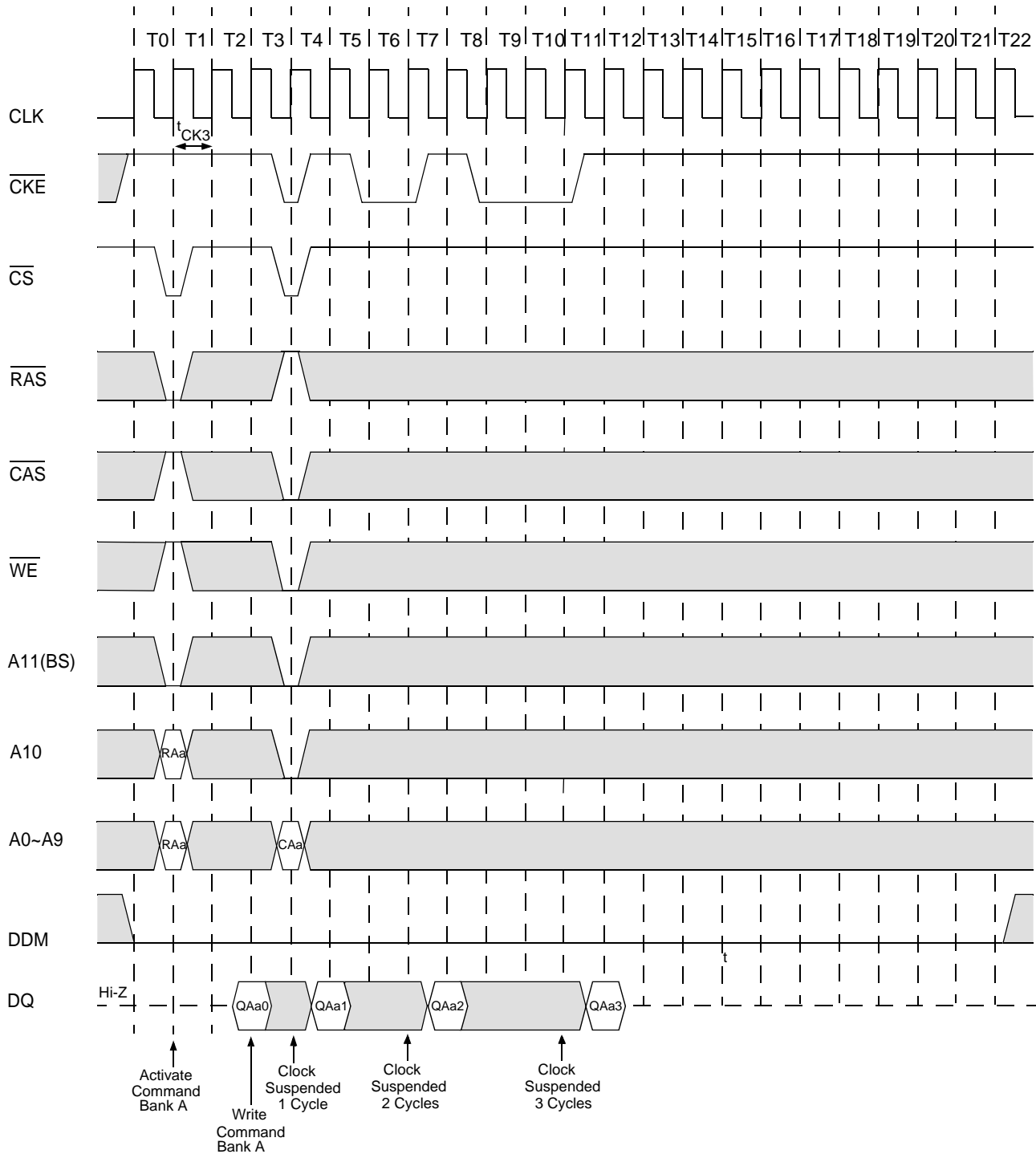
Clock Suspension During burst Write (Using CKE) (1 of 2)

Burst Length=4, $\overline{\text{CAS}}$ Latency=2



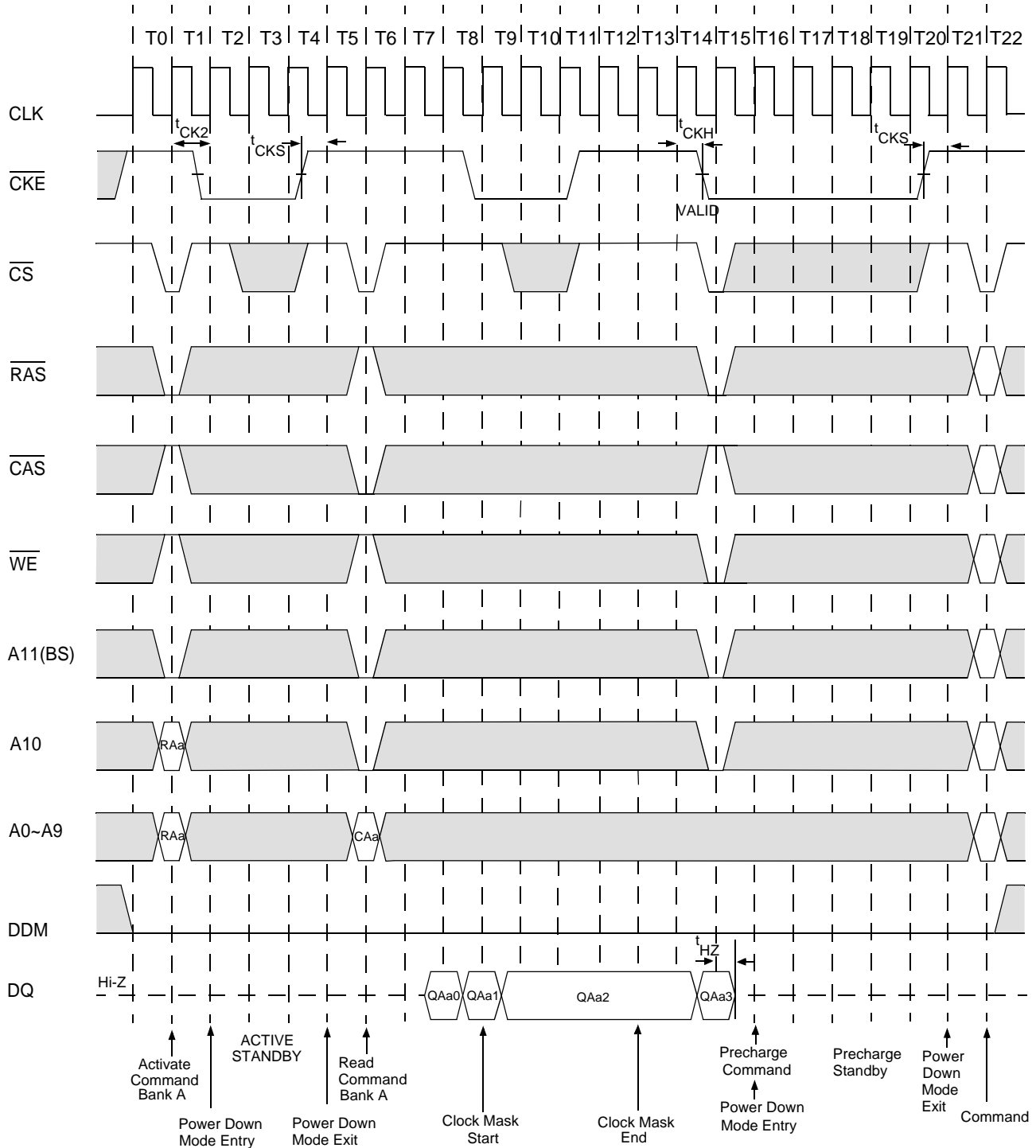
Clock suspension during Burst write (Using CKE) (2 of 2)

Burst Length=4, $\overline{\text{CAS}}$ Latency=3



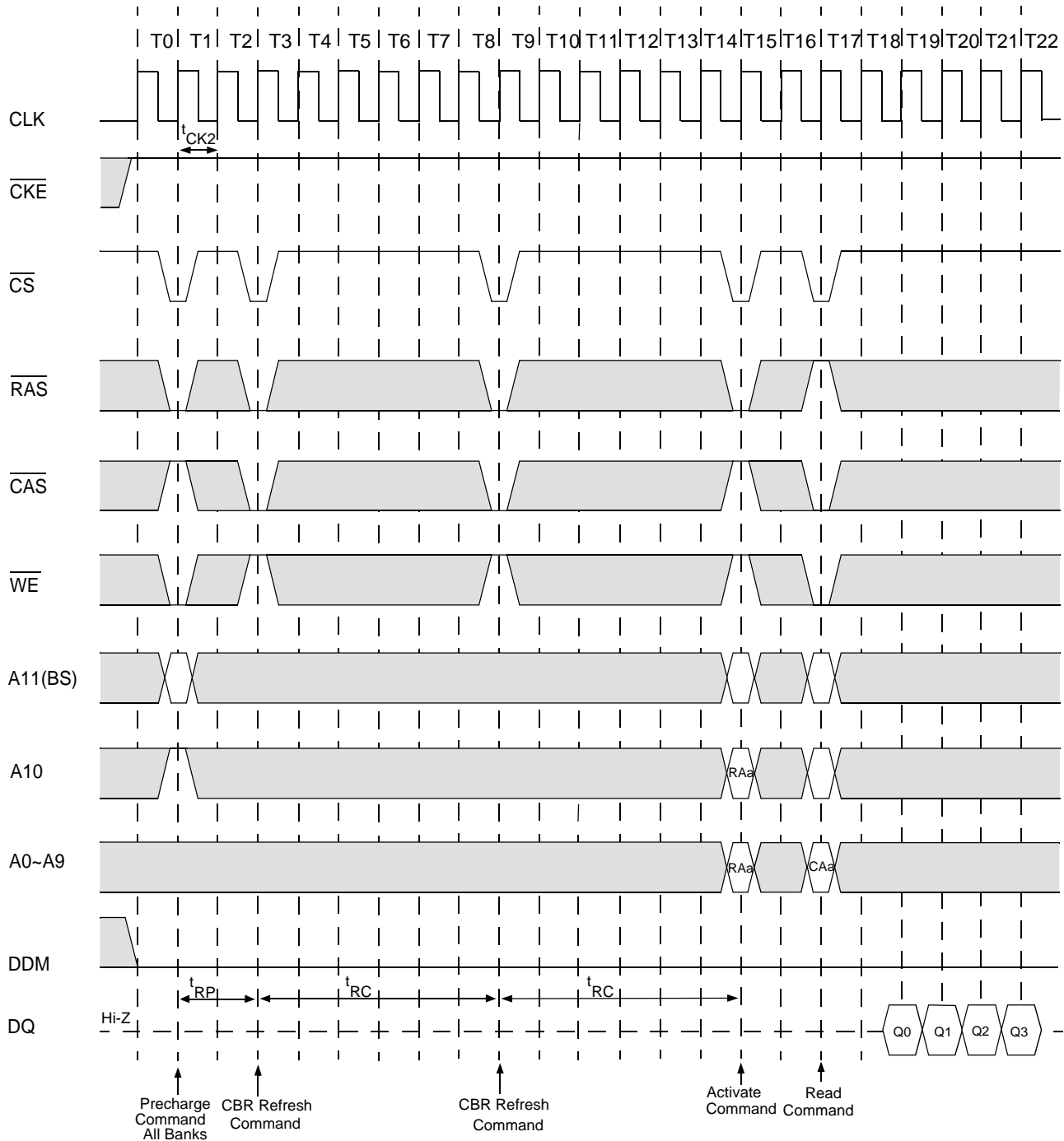
Power Down Mode and Clock Mask

Burst Length=4, $\overline{\text{CAS}}$ Latency=2

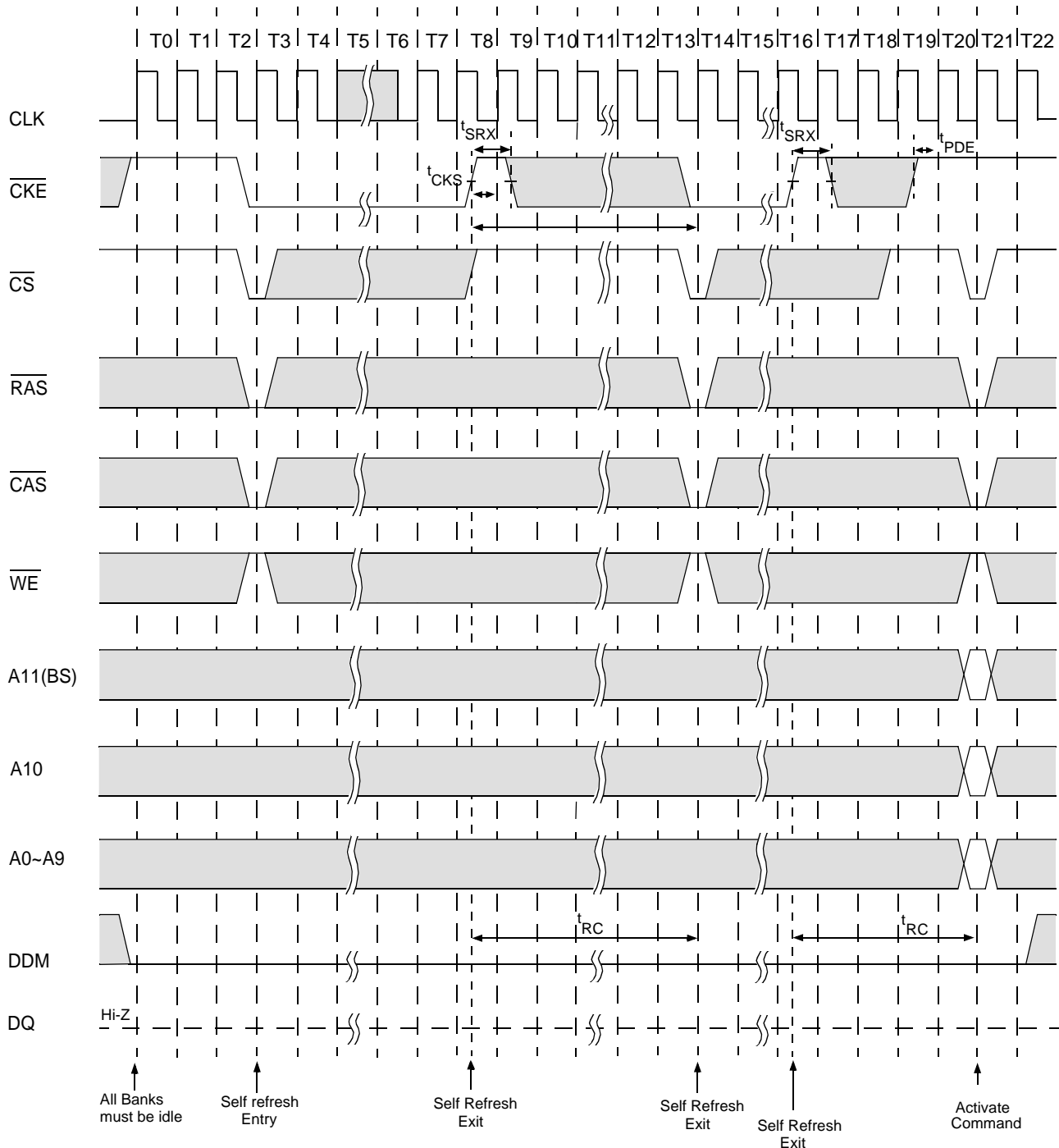


Auto Refresh (CBR)

Burst Length=4, $\overline{\text{CAS}}$ Latency=2

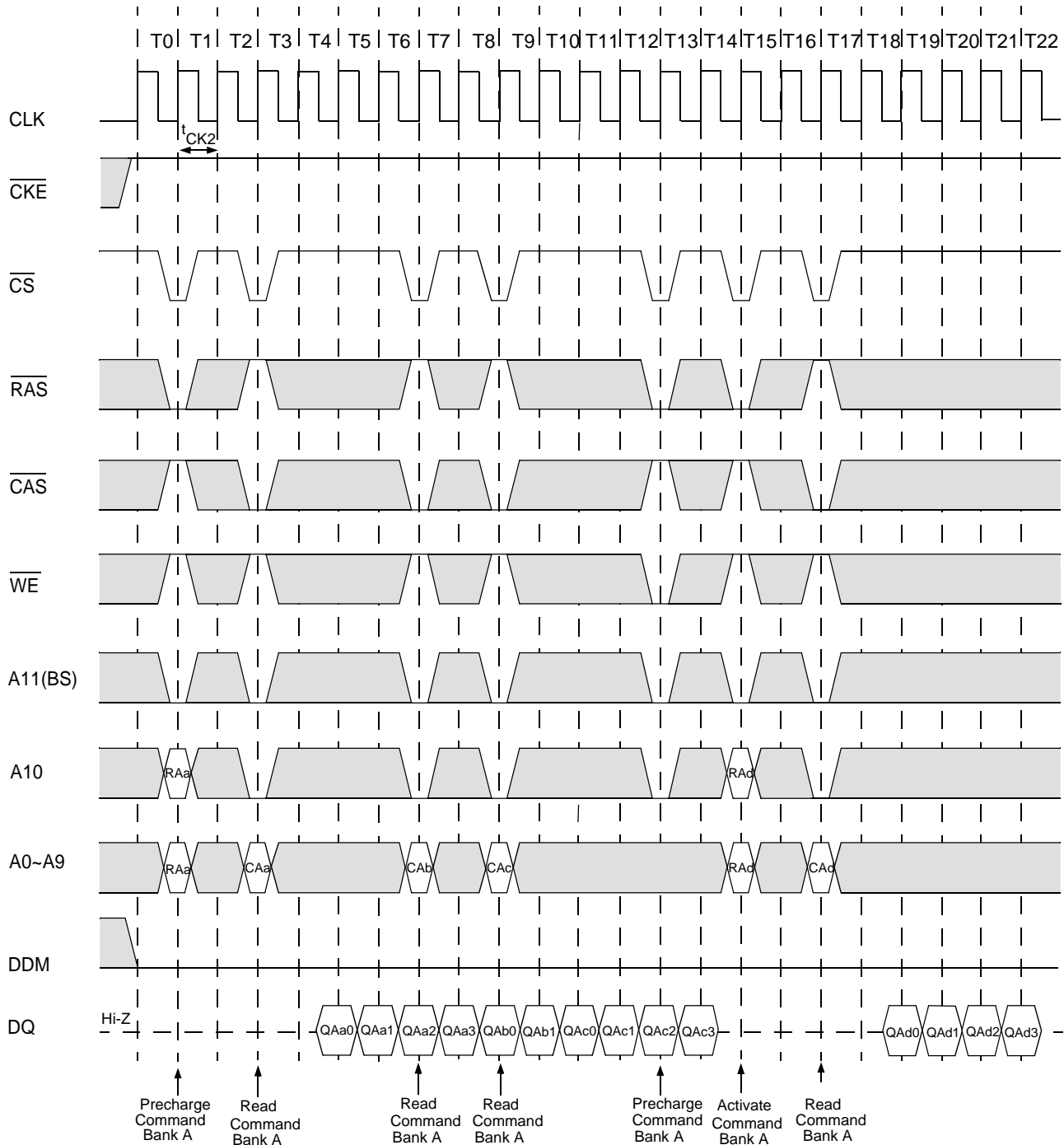


Self Refresh (Entry and Exit)



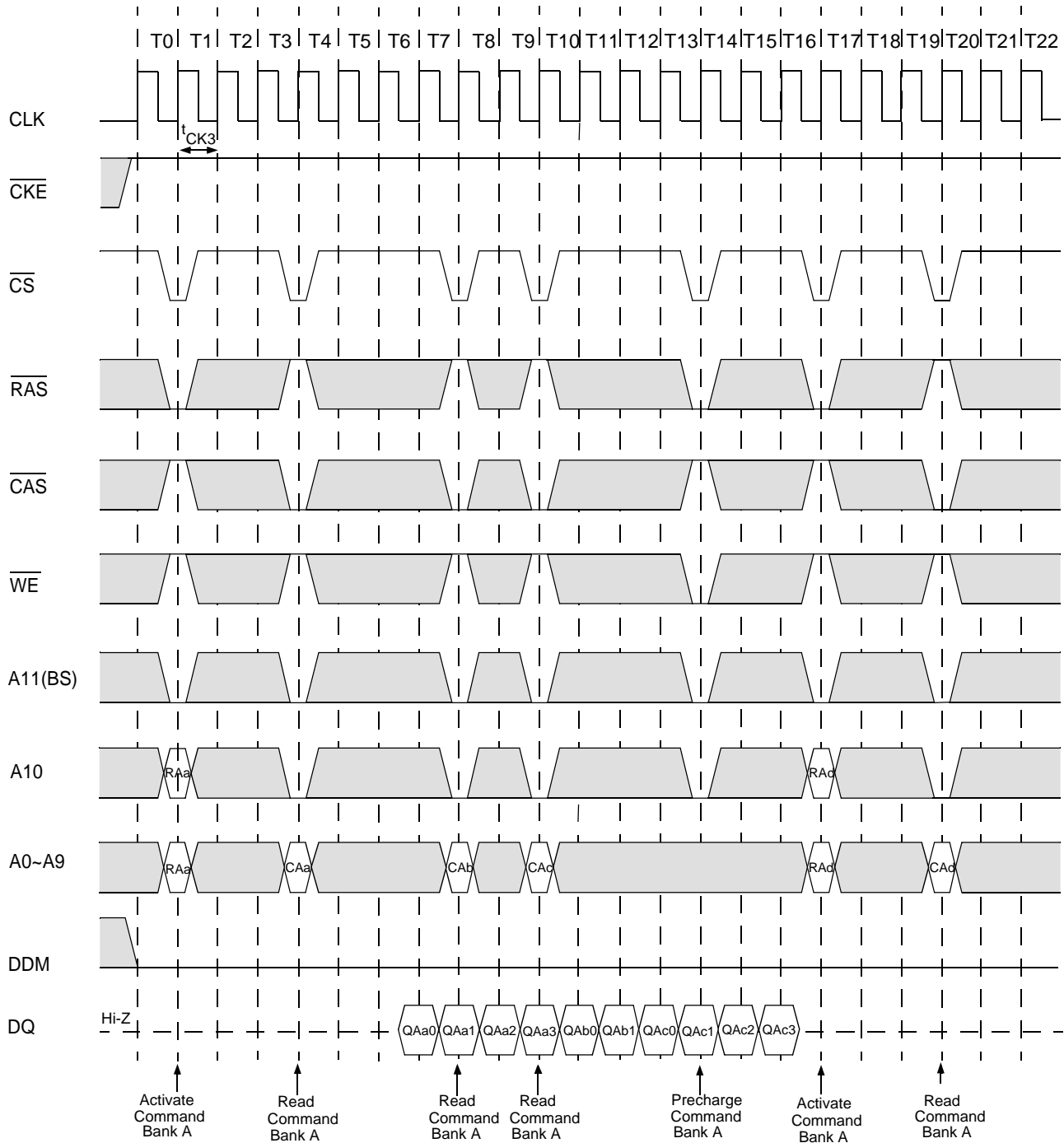
Random Column Read (Page Within same Bank)(1 of 2)

Burst Length=4, $\overline{\text{CAS}}$ Latency=2



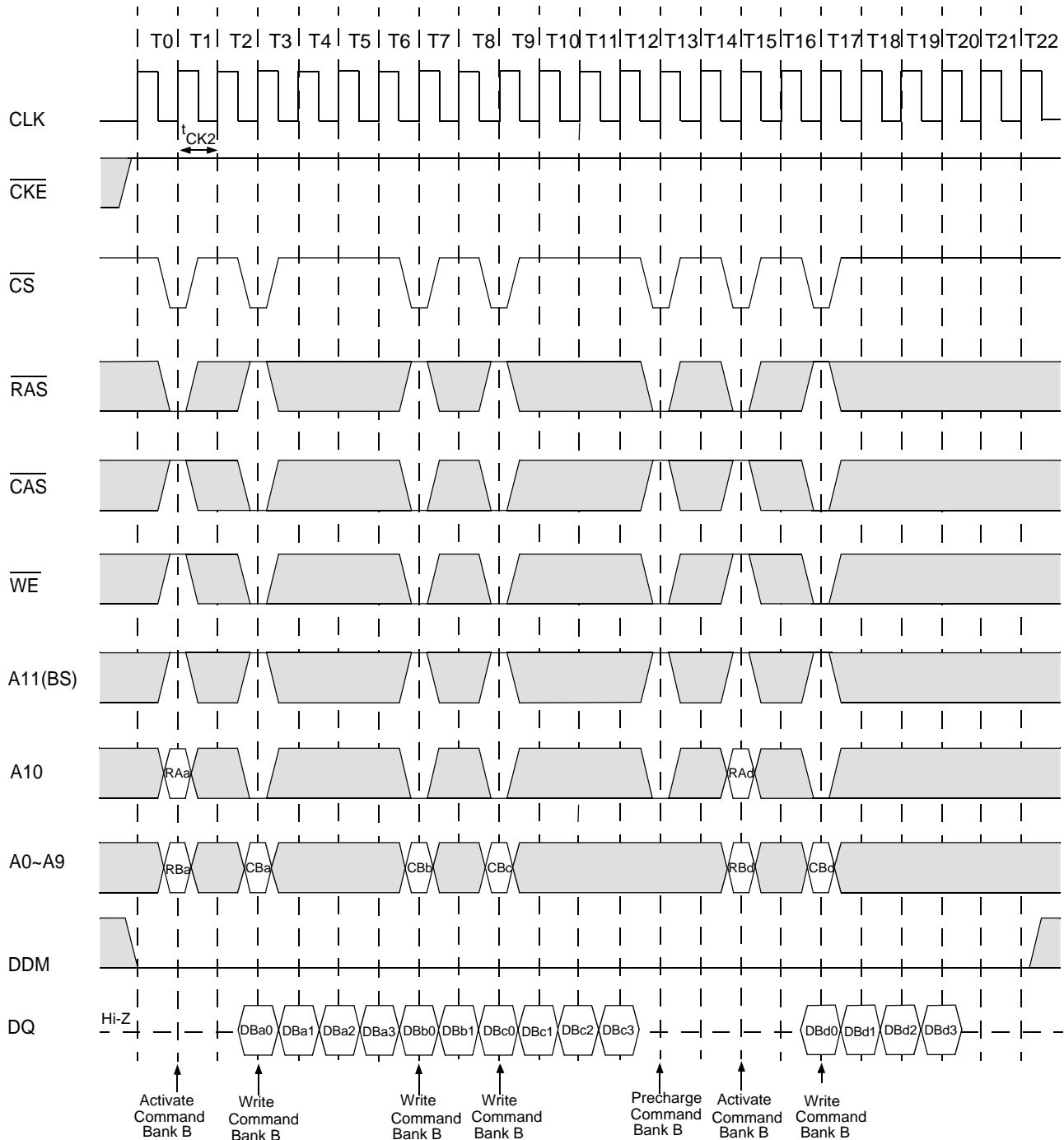
Random Column Read (Page Within same Bank)(2 of 2)

Burst Length=4, $\overline{\text{CAS}}$ Latency=3



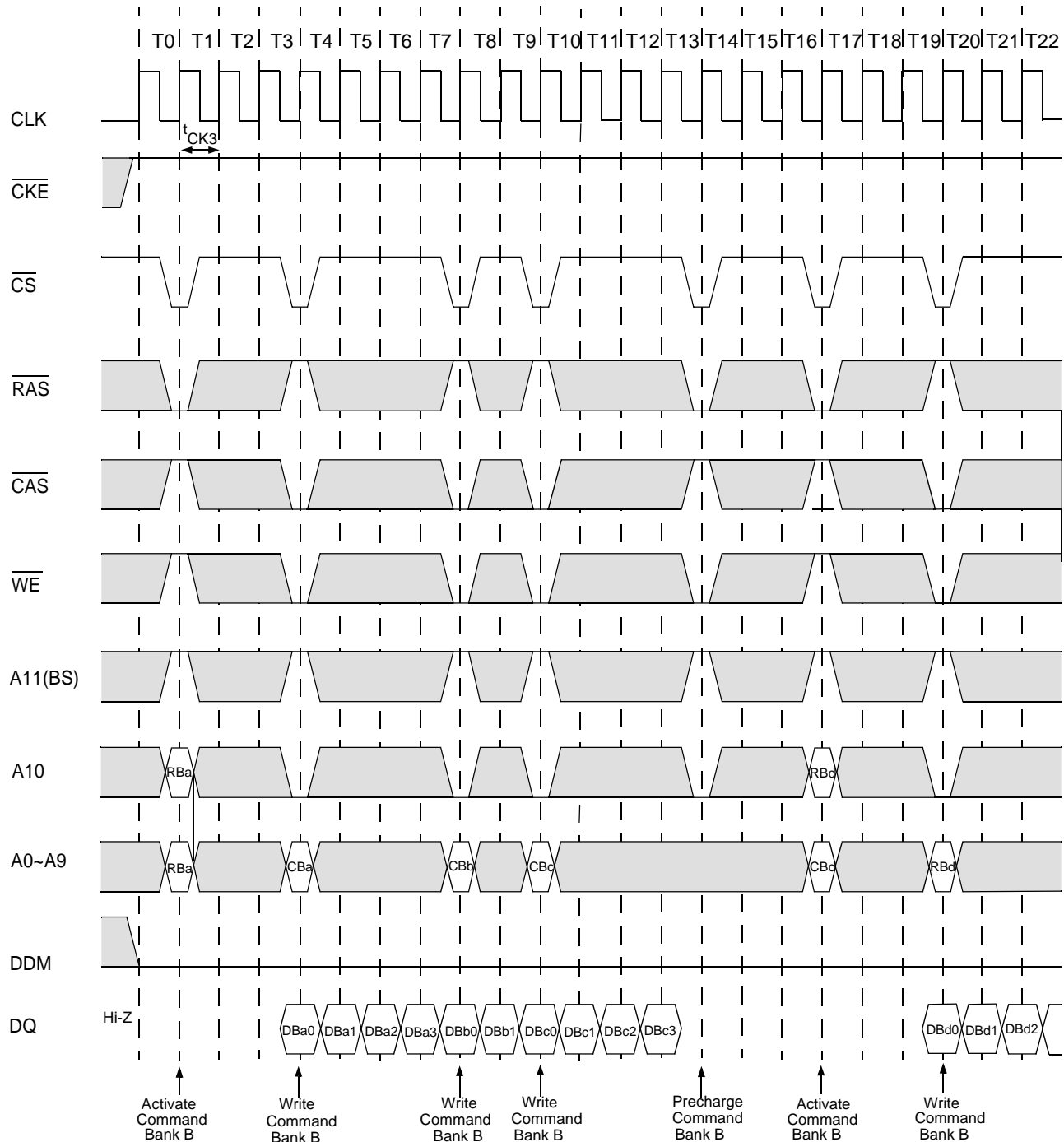
Random Column Write (Page Within same Bank) (1 of 2)

Burst Length=4, $\overline{\text{CAS}}$ Latency=2



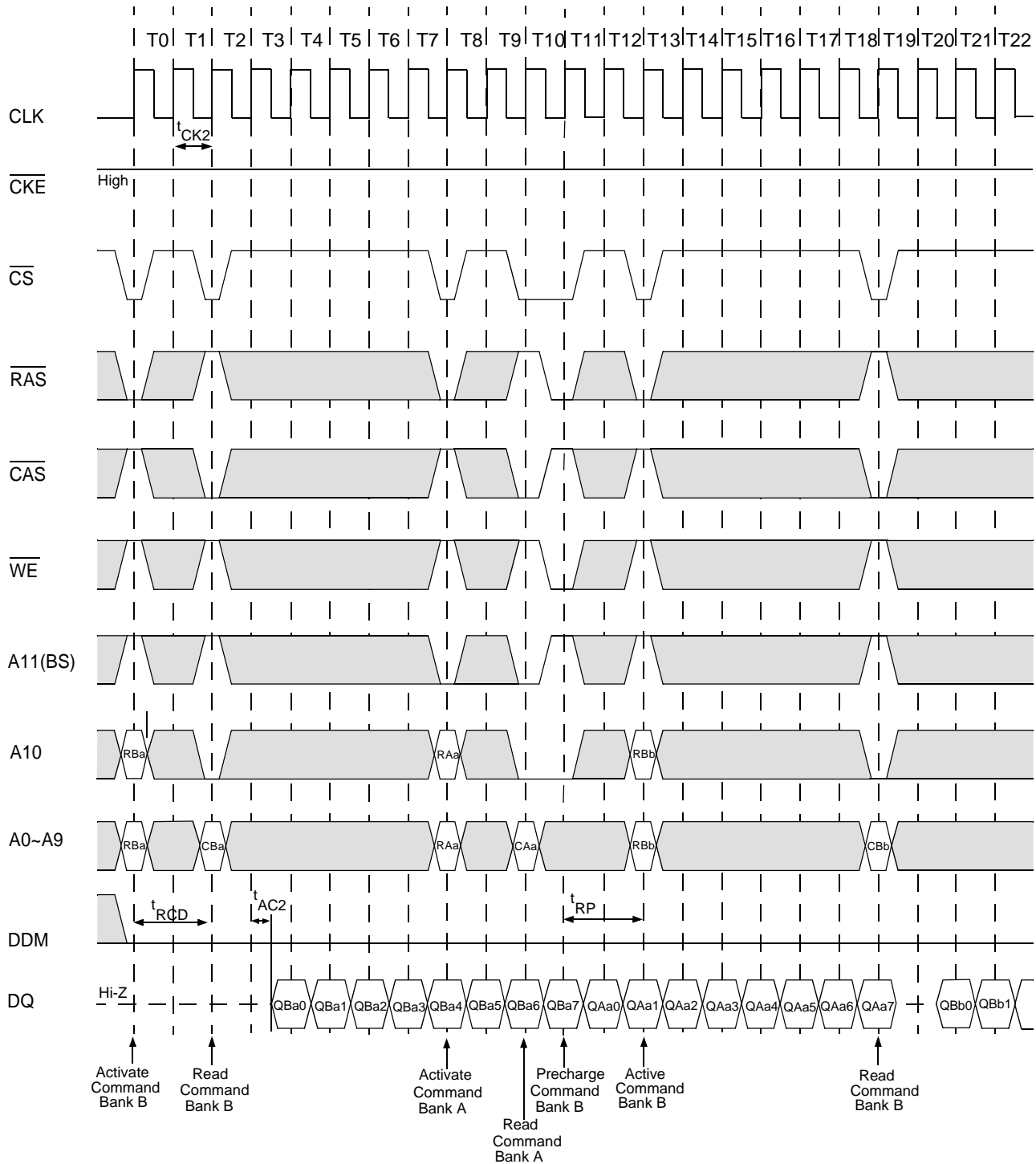
Random Column Write (Page Within same Bank) (2 of 2)

Burst Length=4, $\overline{\text{CAS}}$ Latency=3



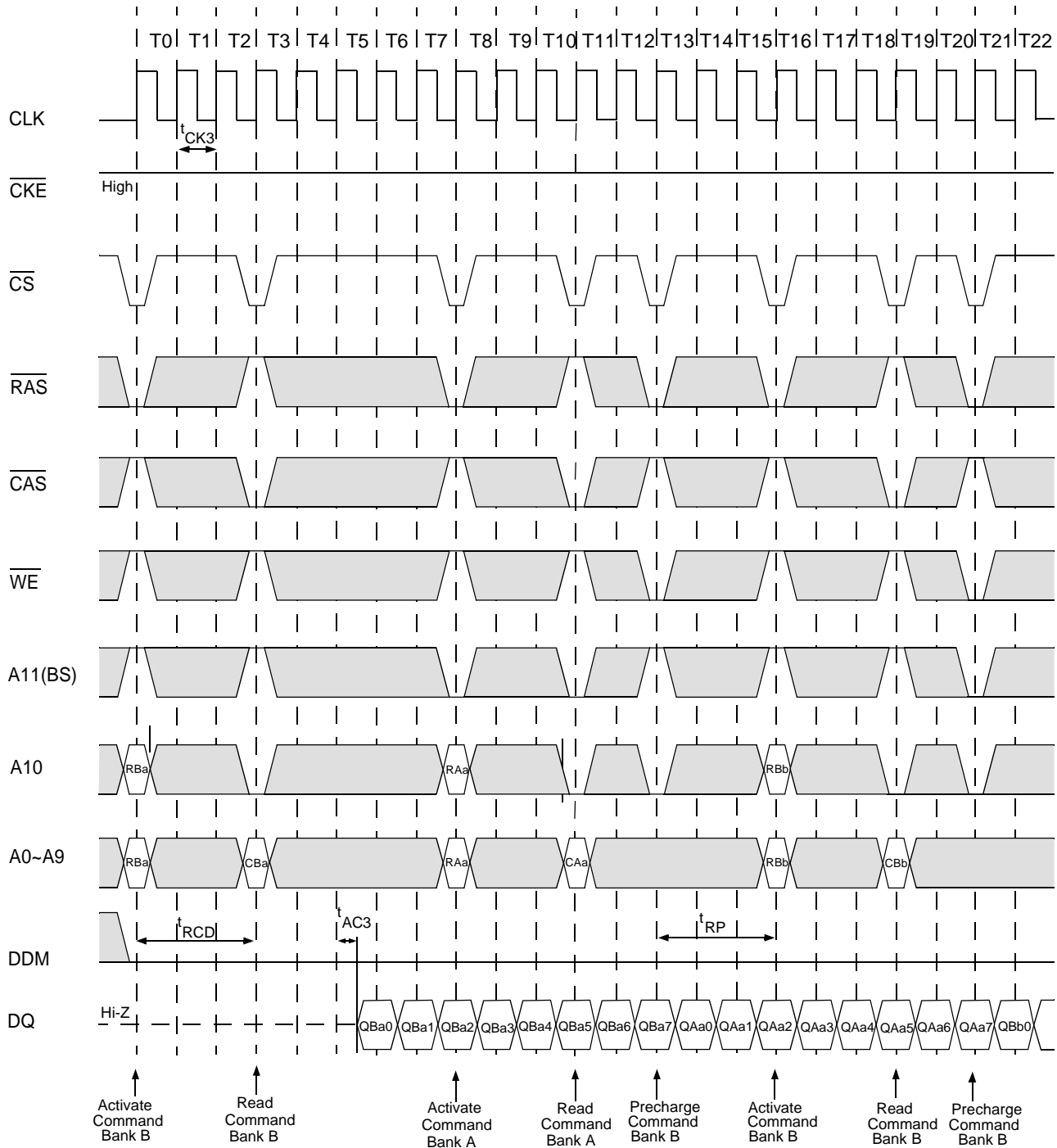
Random Row Read (Interleaving Banks) (1 of 2)

Burst Length=8, $\overline{\text{CAS}}$ Latency=2



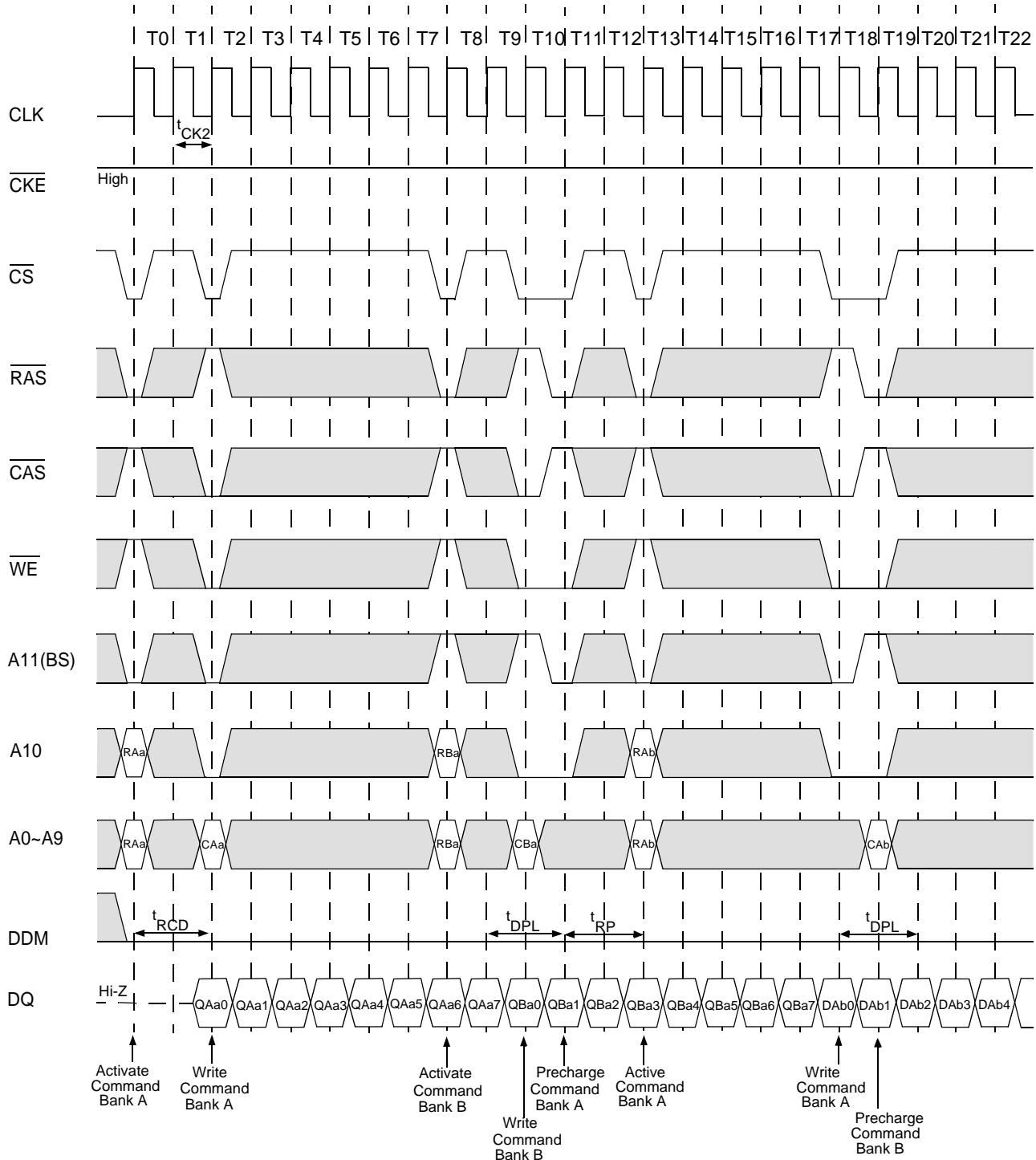
Random Row Read (Interleaving Banks) (2 of 2)

Burst Length=8, $\overline{\text{CAS}}$ Latency=3



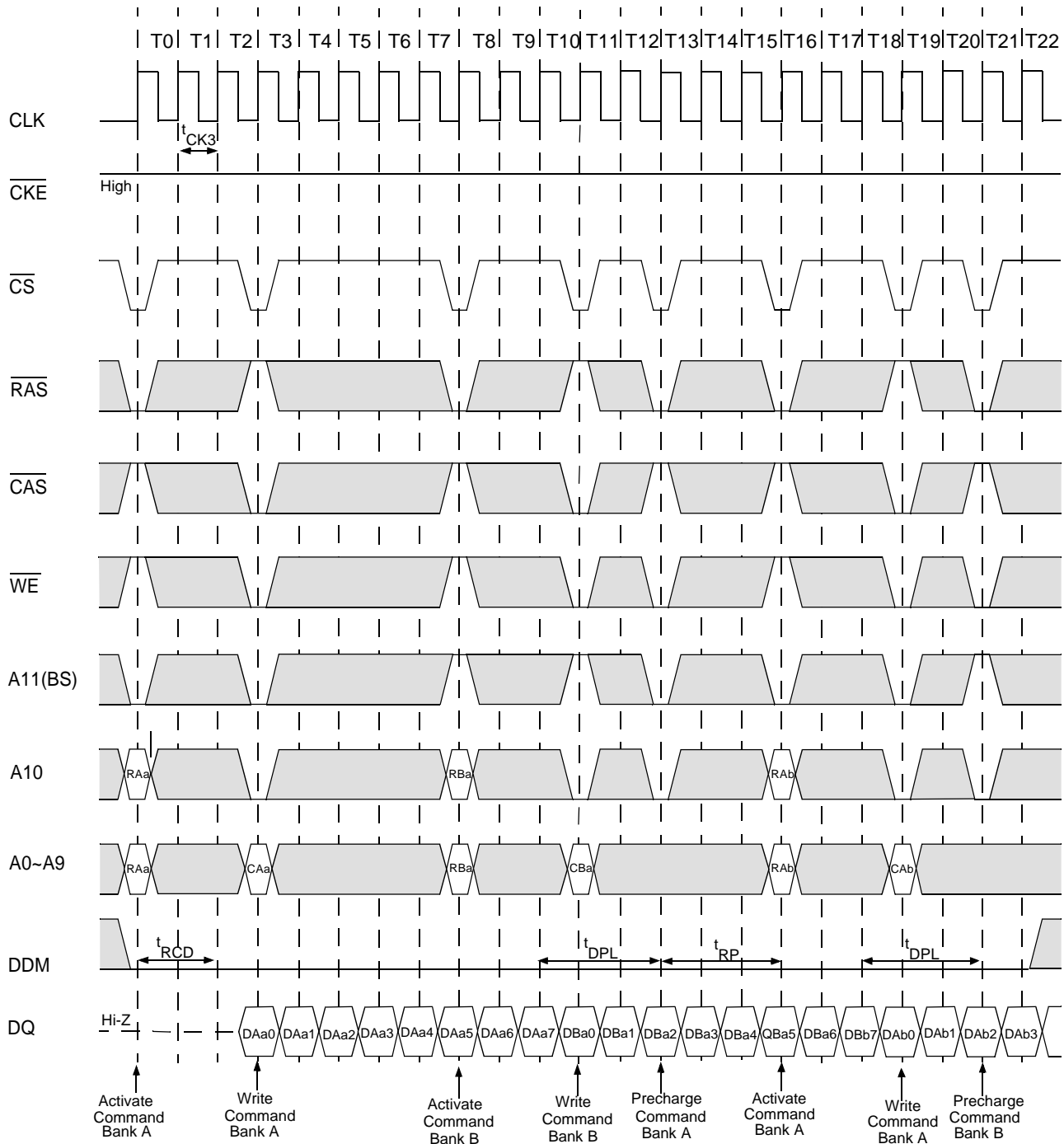
Random Row Write (Interleaving Banks) (1 of 2)

Burst Length=8, $\overline{\text{CAS}}$ Latency=2



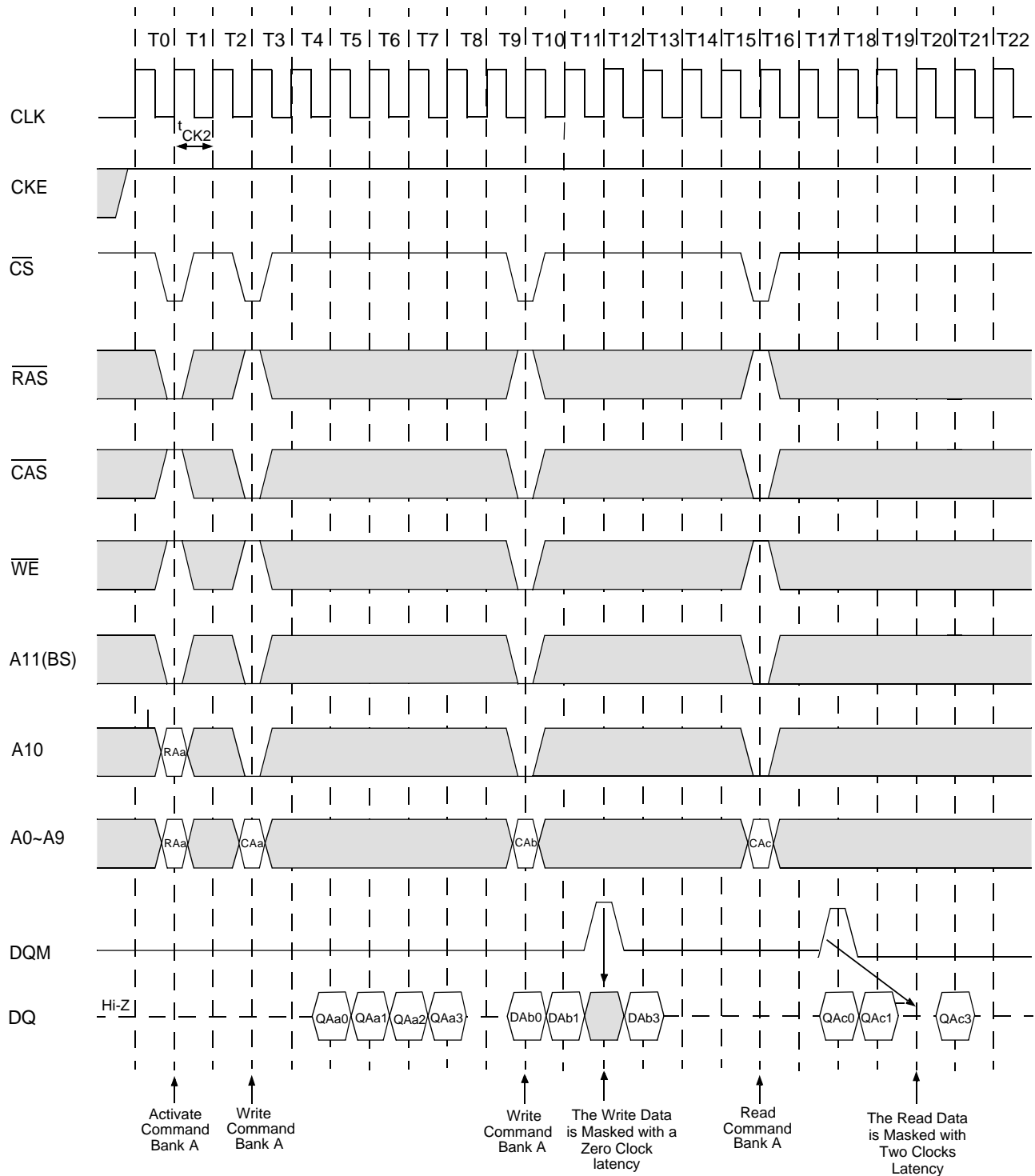
Random Row Write (Interleaving Banks) (2 of 2)

Burst Length=8, $\overline{\text{CAS}}$ Latency=3



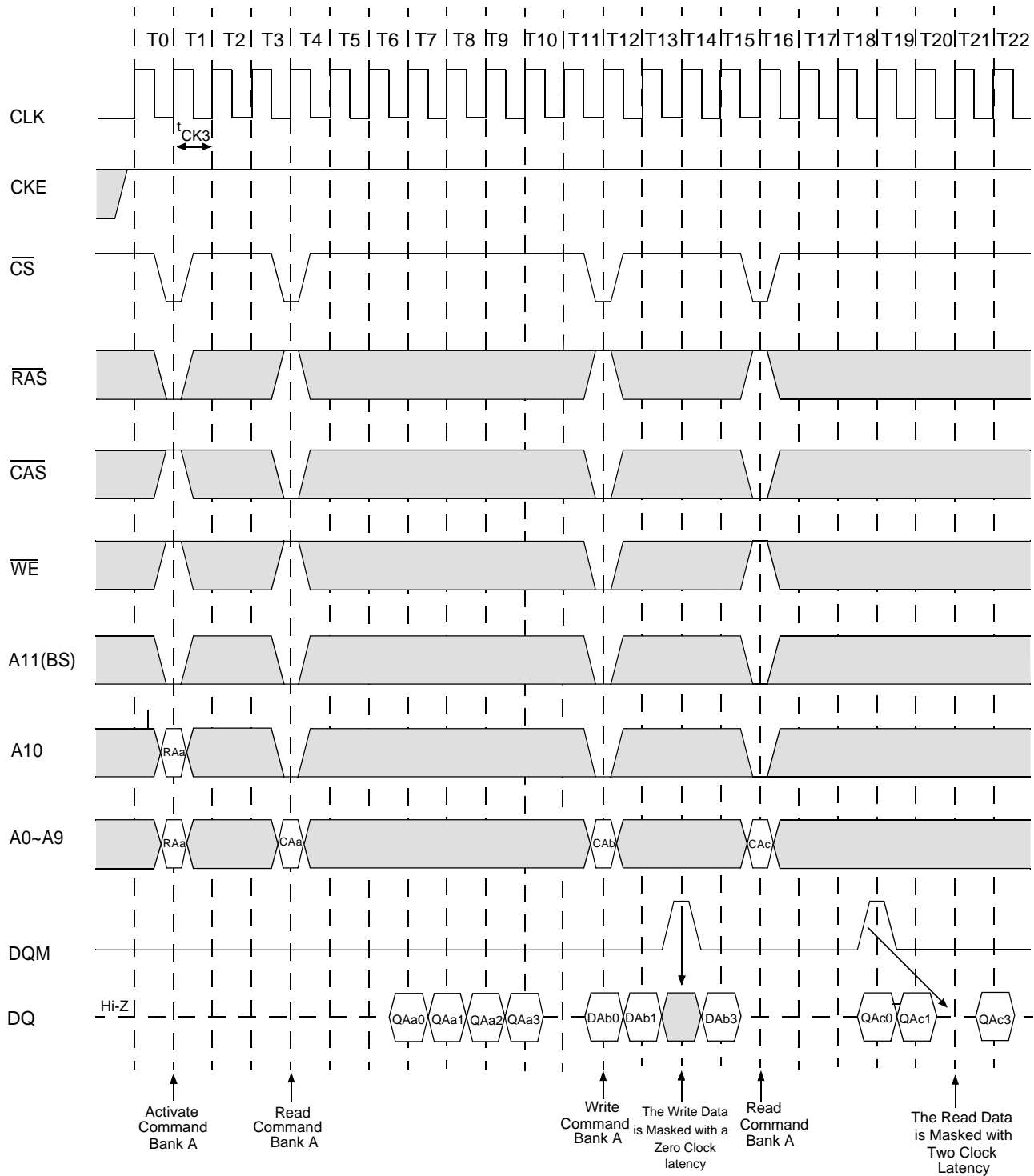
Read and Write Cycle (1 of 2)

Burst Length=4, $\overline{\text{CAS}}$ Latency=2



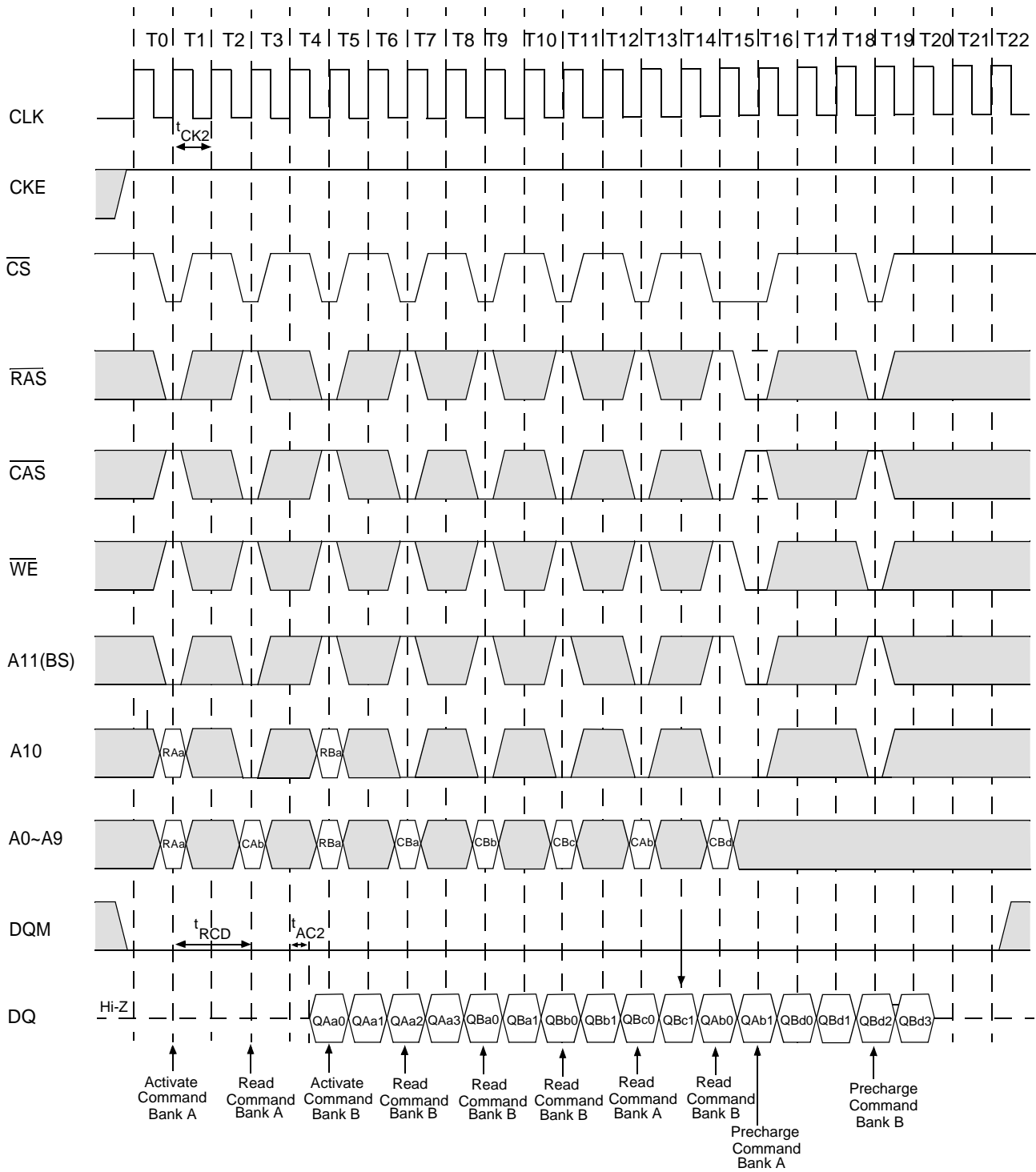
Read and Write Cycle (2 of 2)

Burst Length=4, $\overline{\text{CAS}}$ Latency=3



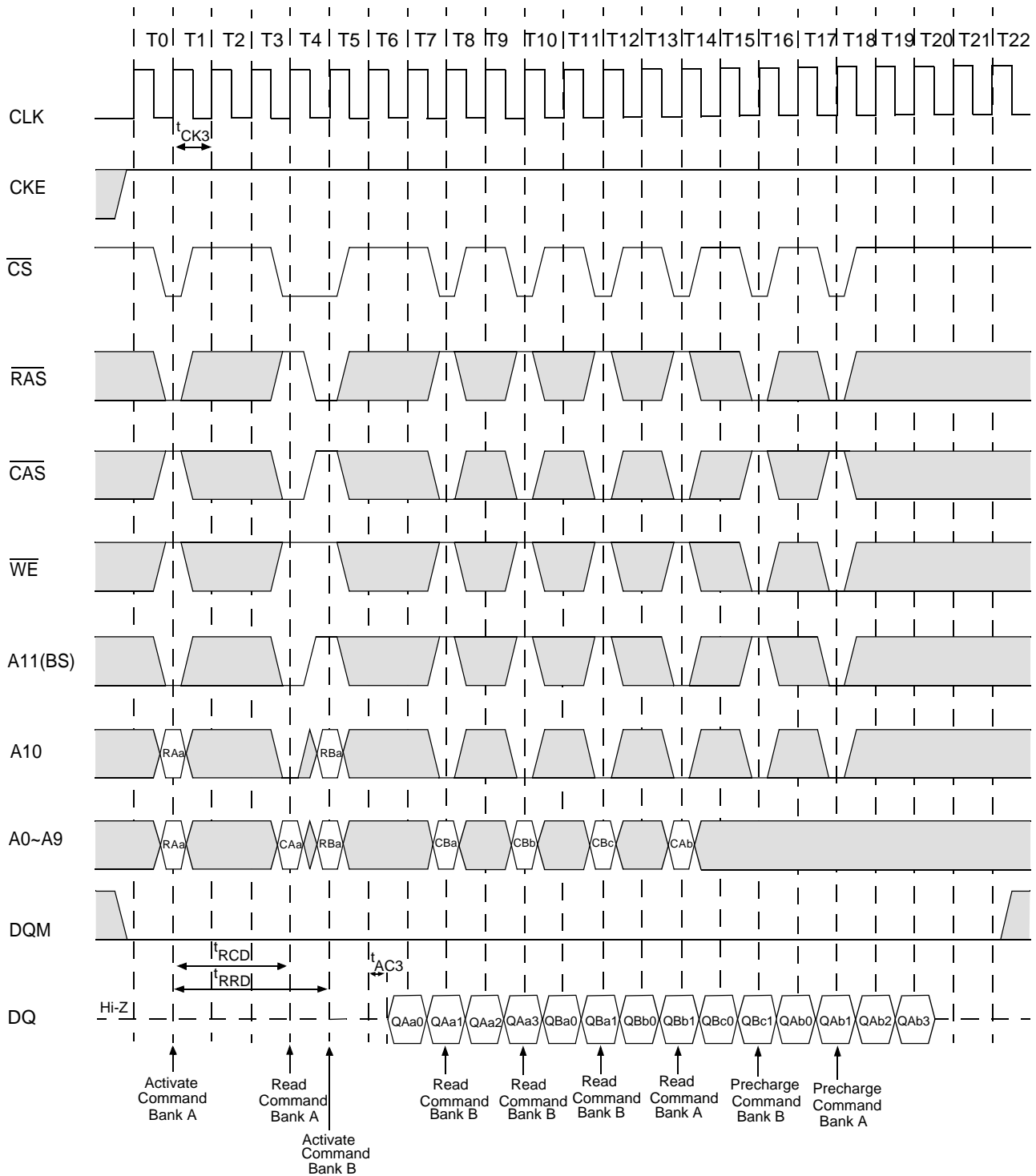
Interleaved Column Read Cycle (1 of 2)

Burst Length=4, $\overline{\text{CAS}}$ Latency=2



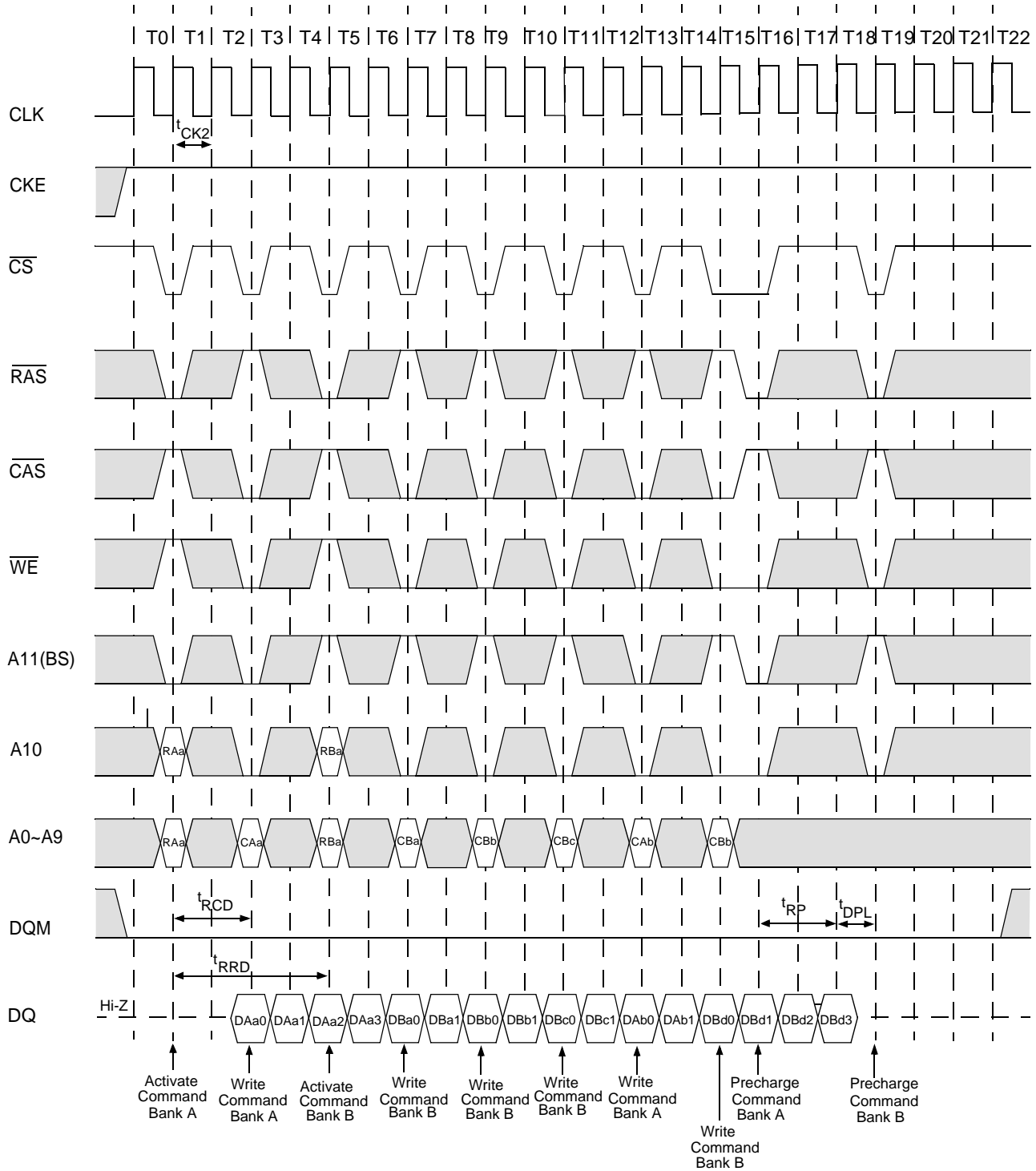
Interleaved Column Read Cycle (2 of 2)

Burst Length=4, $\overline{\text{CAS}}$ Latency=3



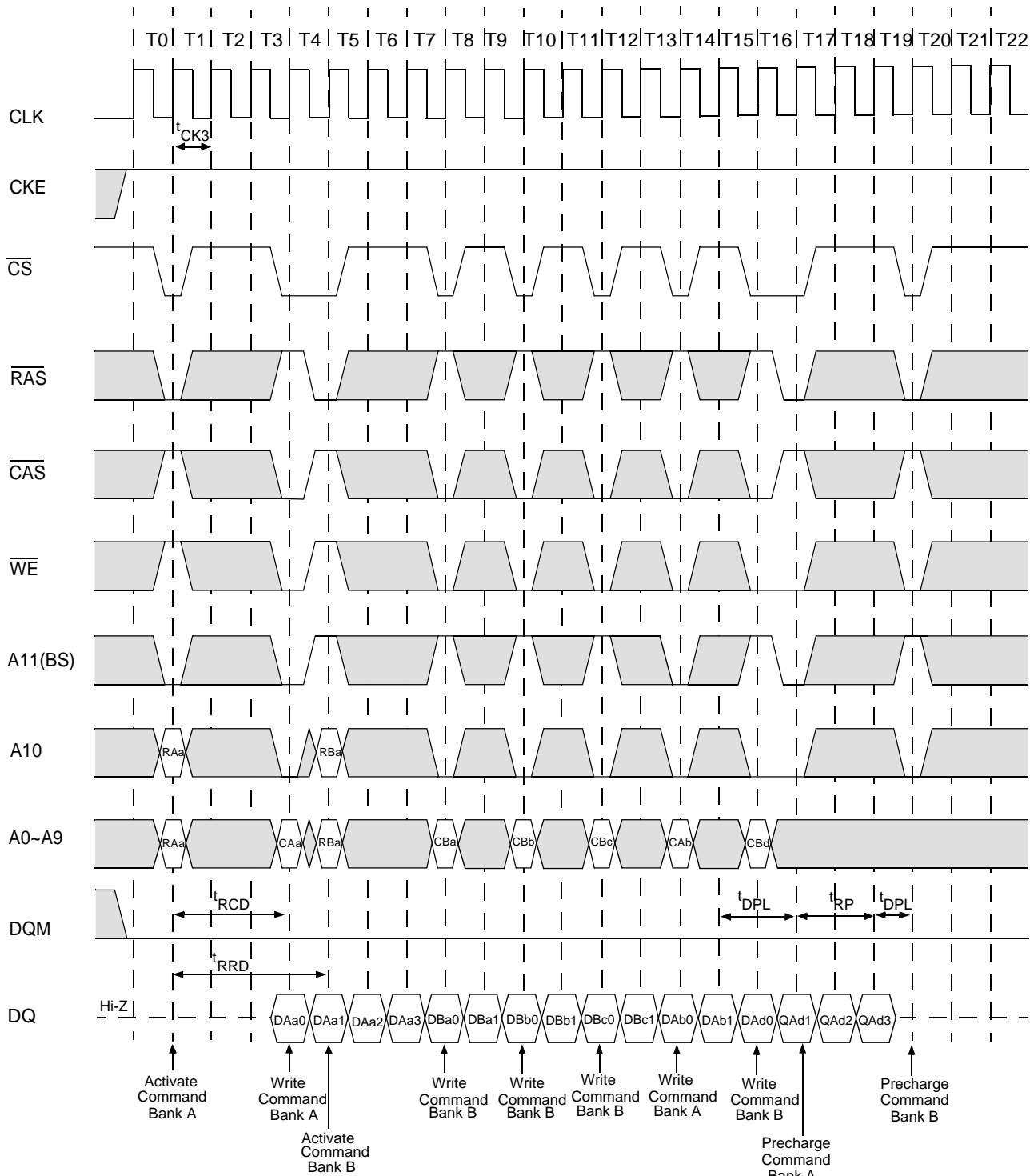
Interleaved Column Write Cycle (1 of 2)

Burst Length=4, $\overline{\text{CAS}}$ Latency=2



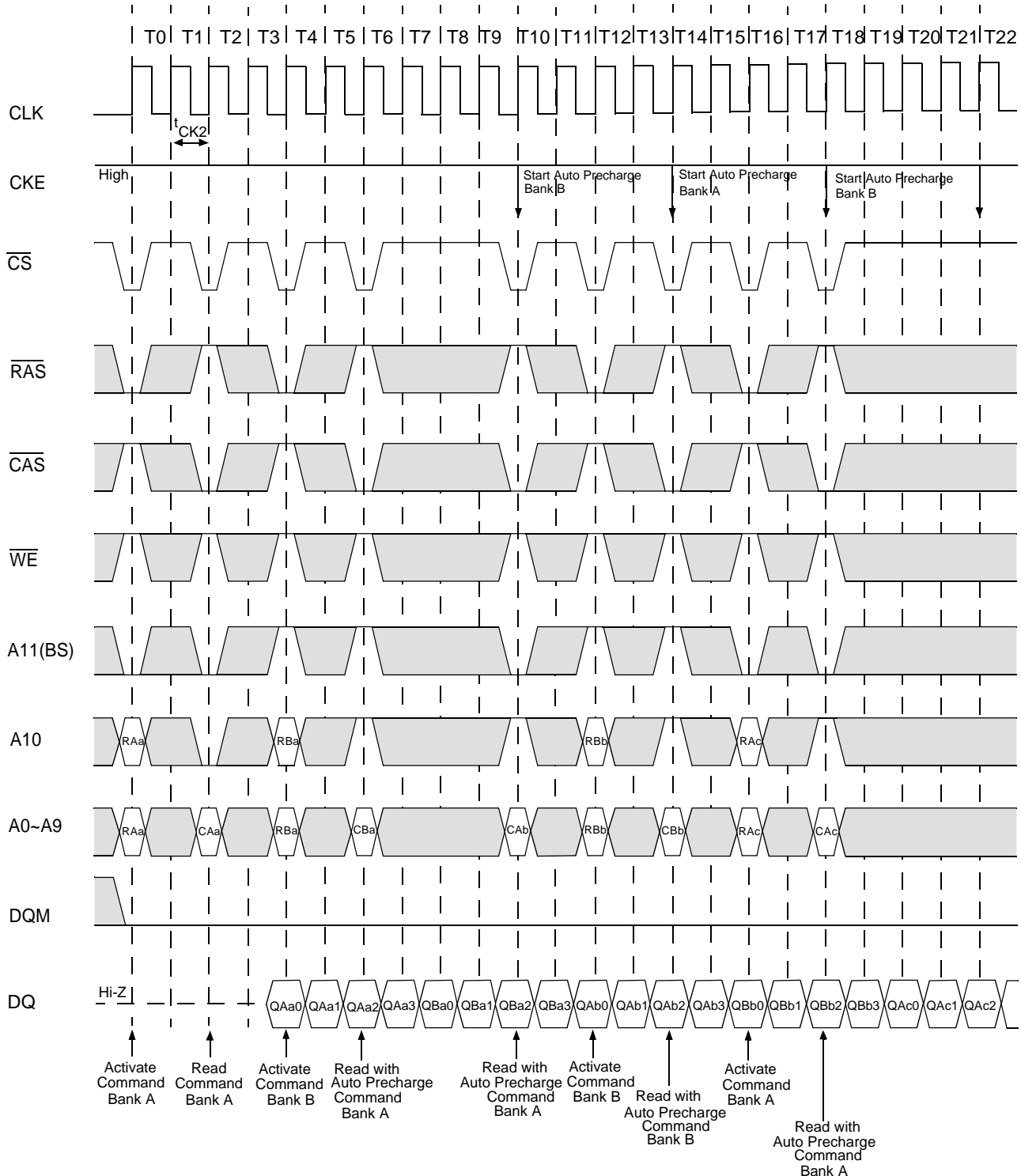
Interleaved Column Write Cycle (2 of 2)

Burst Length=4, $\overline{\text{CAS}}$ Latency=3



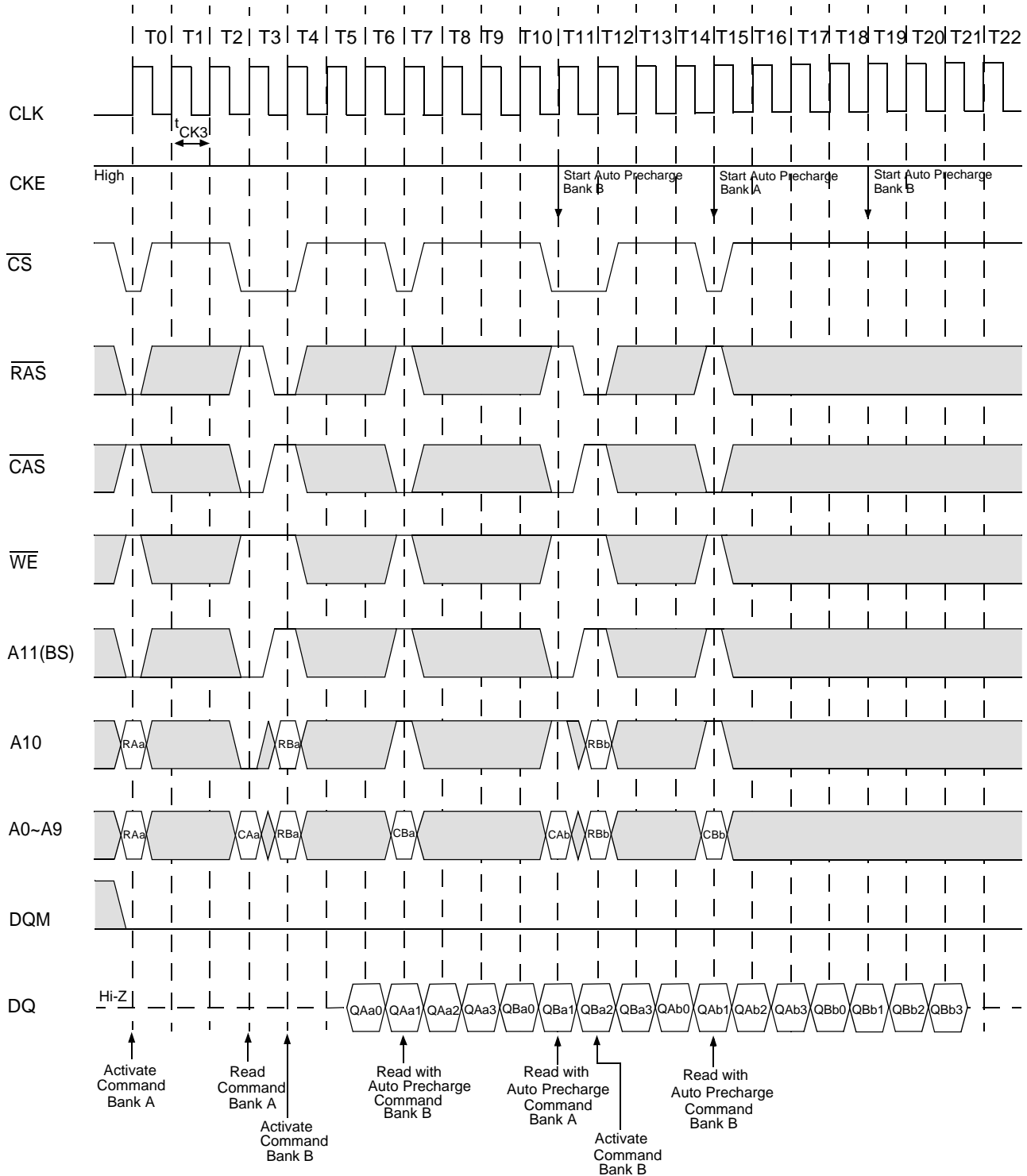
Auto Precharge after Read Burst (1 of 2)

Burst Length=4, $\overline{\text{CAS}}$ Latency=2



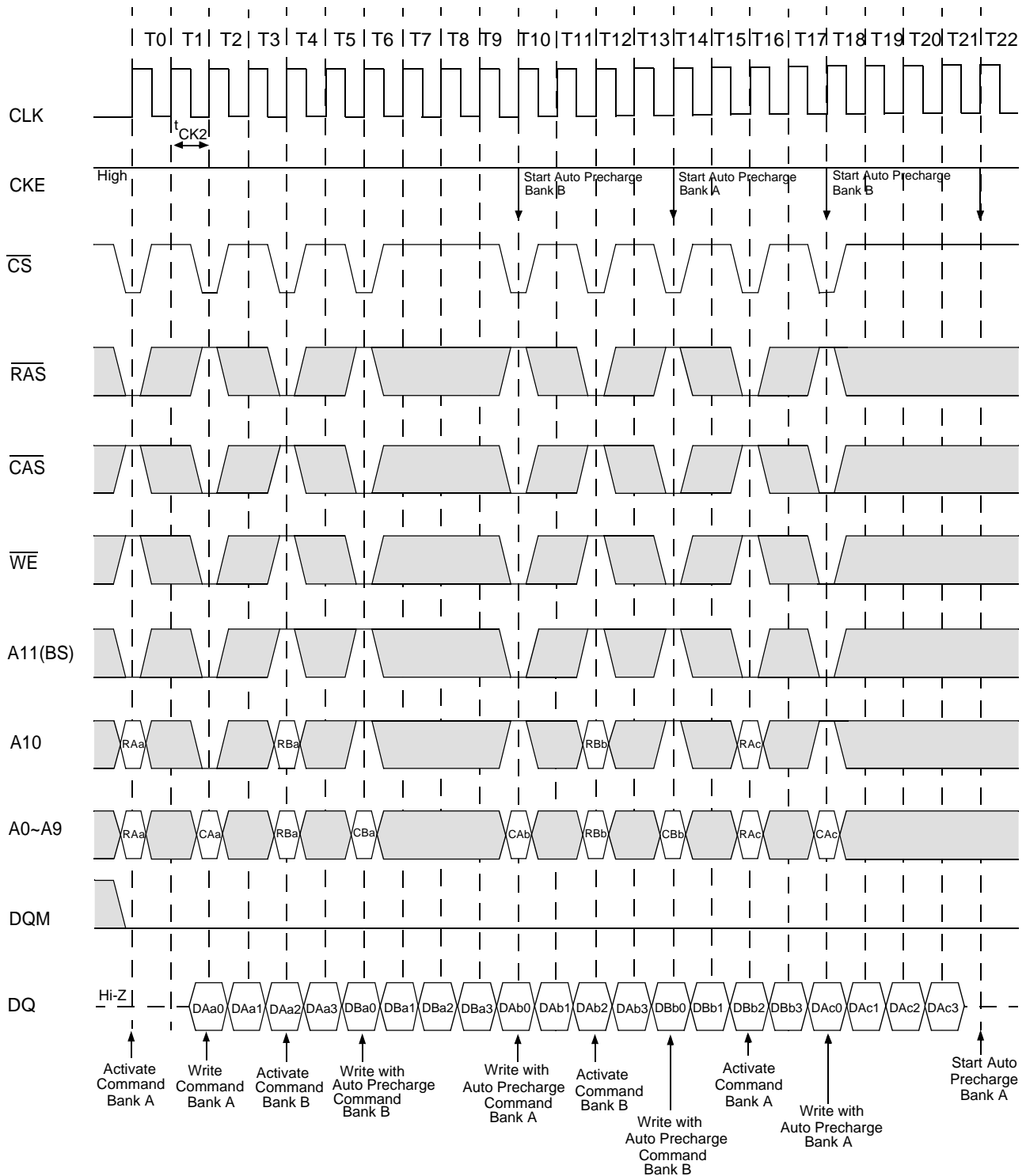
Auto Precharge after Read Burst (2 of 2)

Burst Length=4, $\overline{\text{CAS}}$ Latency=3



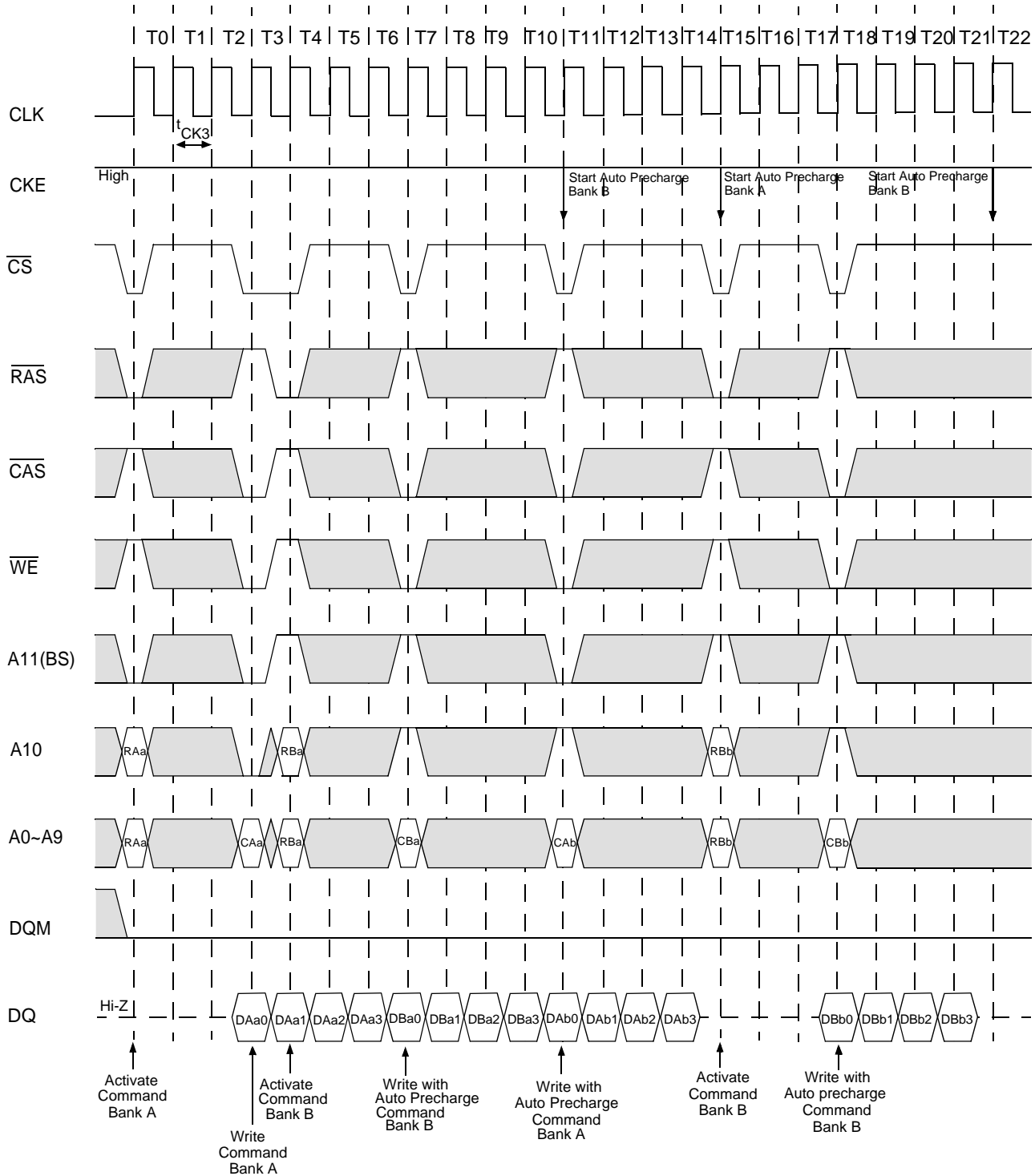
Auto Precharge after Write Burst (1 of 2)

Burst Length=4, $\overline{\text{CAS}}$ Latency=2



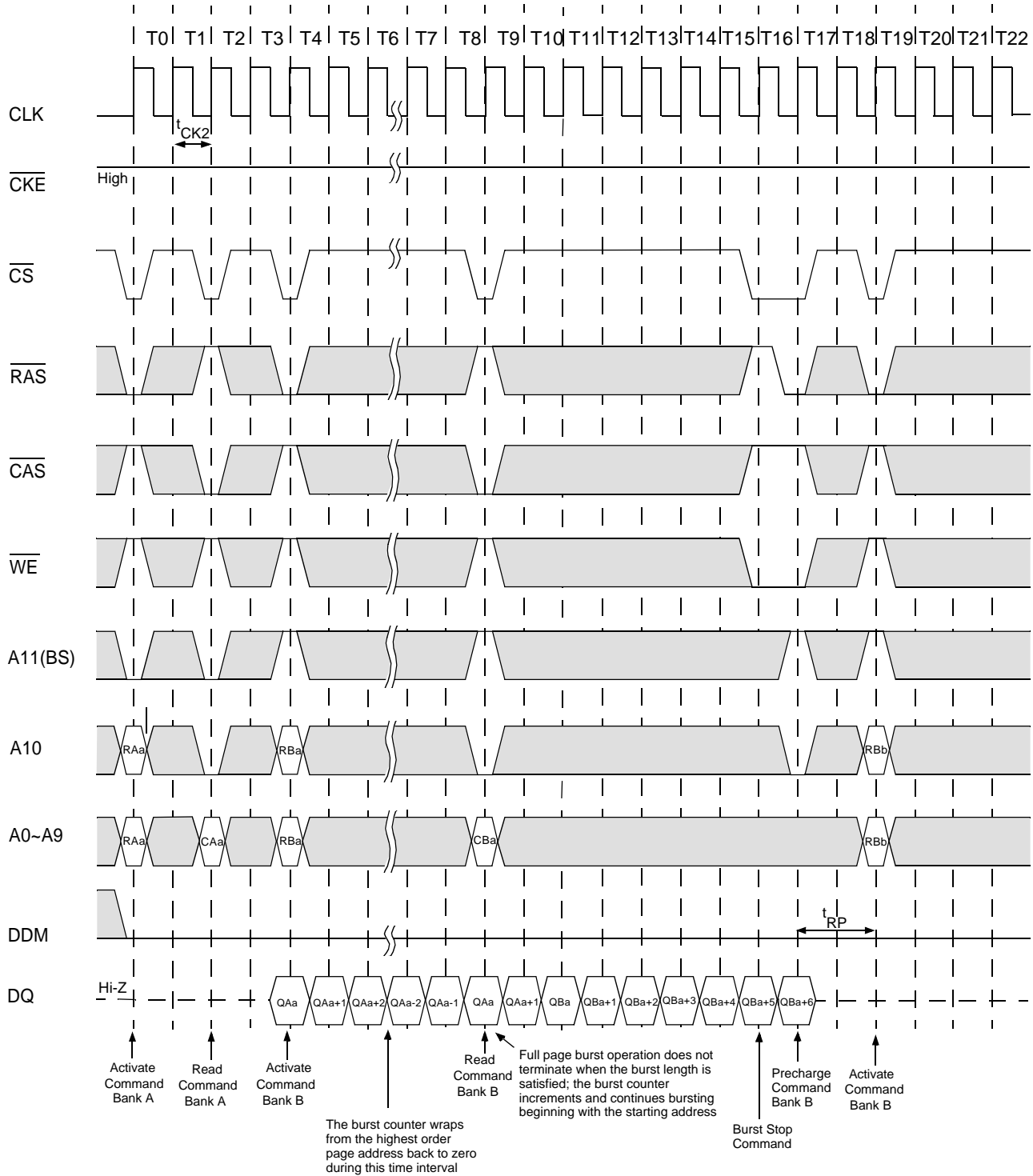
Auto Precharge after Write Burst (2 of 2)

Burst Length=4, $\overline{\text{CAS}}$ Latency=3



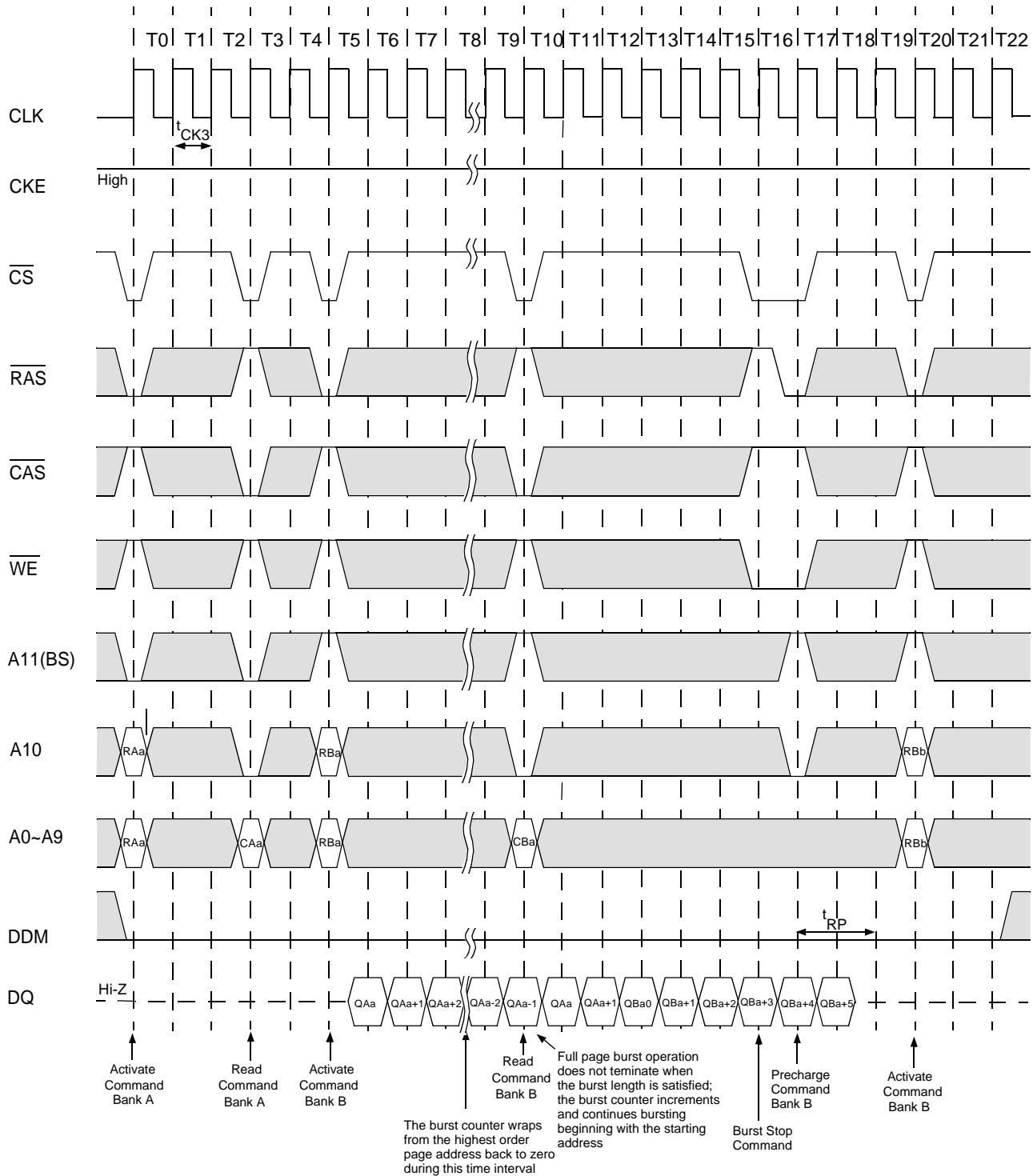
Full Page Read Cycle (1 of 2)

Burst Length=Full Page, $\overline{\text{CAS}}$ Latency=2



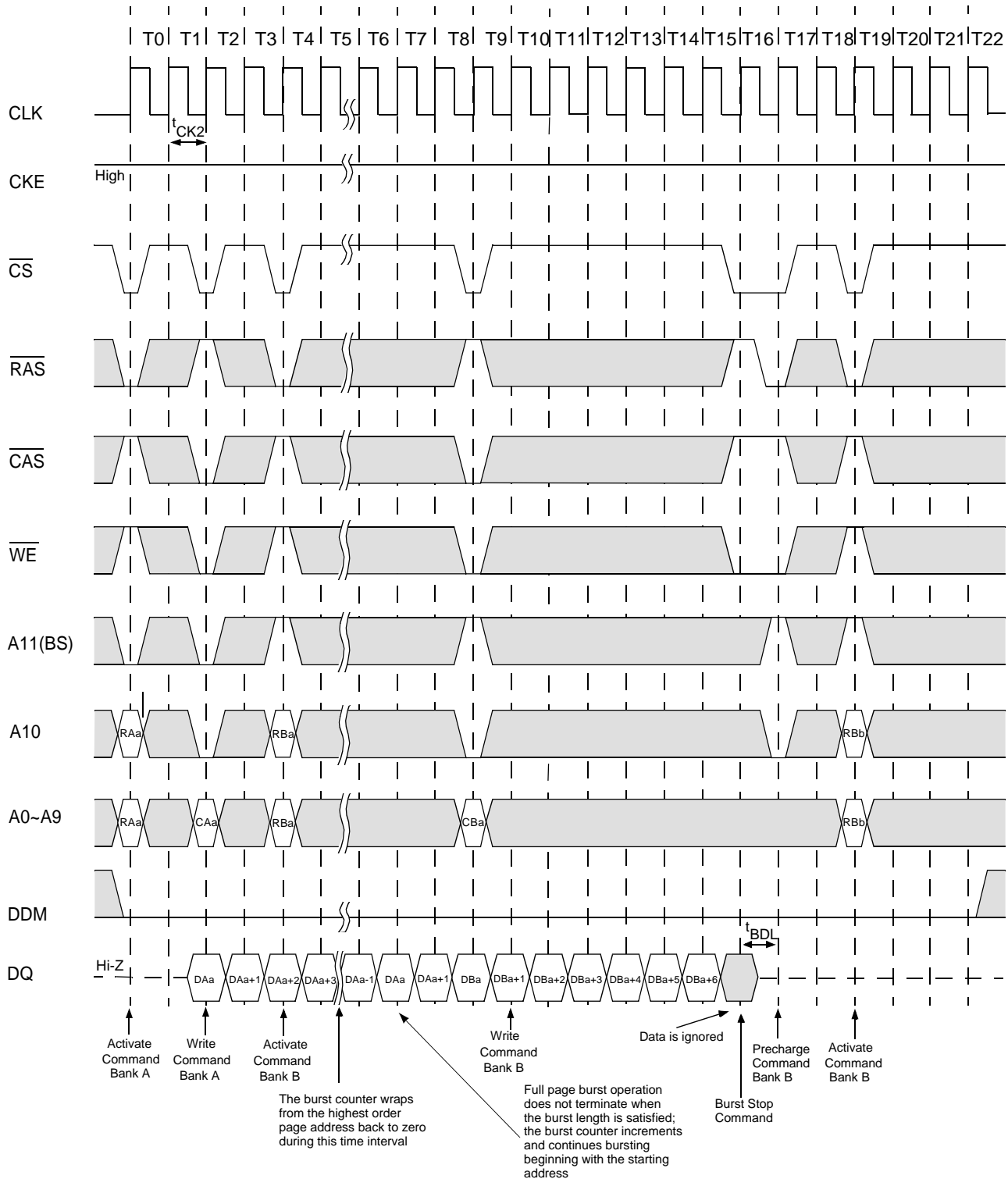
Full Page Read Cycle (2 of 2)

Burst Length=Full Page, $\overline{\text{CAS}}$ Latency=3



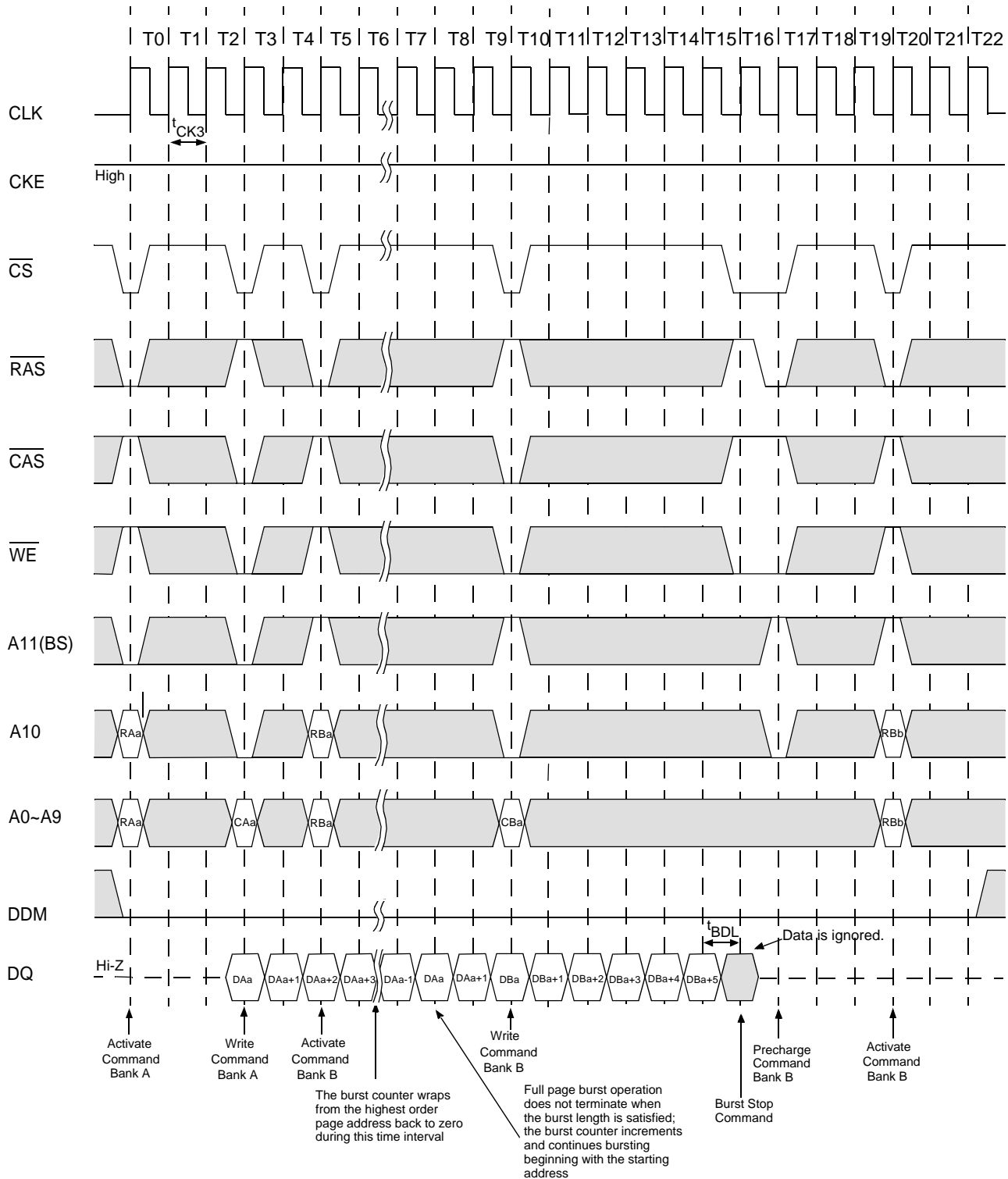
Full Page Write Cycle (1 of 2)

Burst Length=Full Page, $\overline{\text{CAS}}$ Latency=2



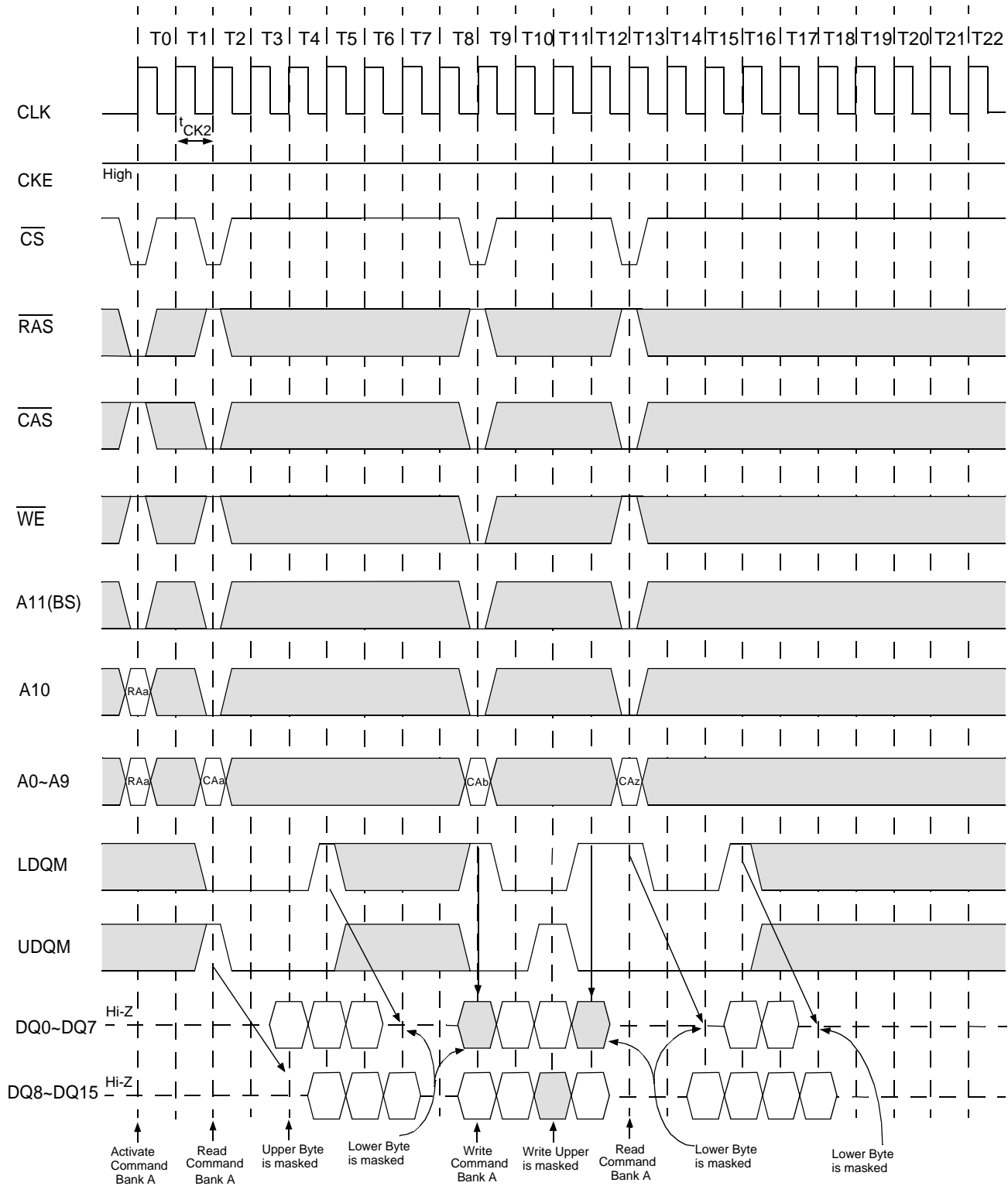
Full Page Write Cycle (2 of 2)

Burst Length=Full Page, $\overline{\text{CAS}}$ Latency=3



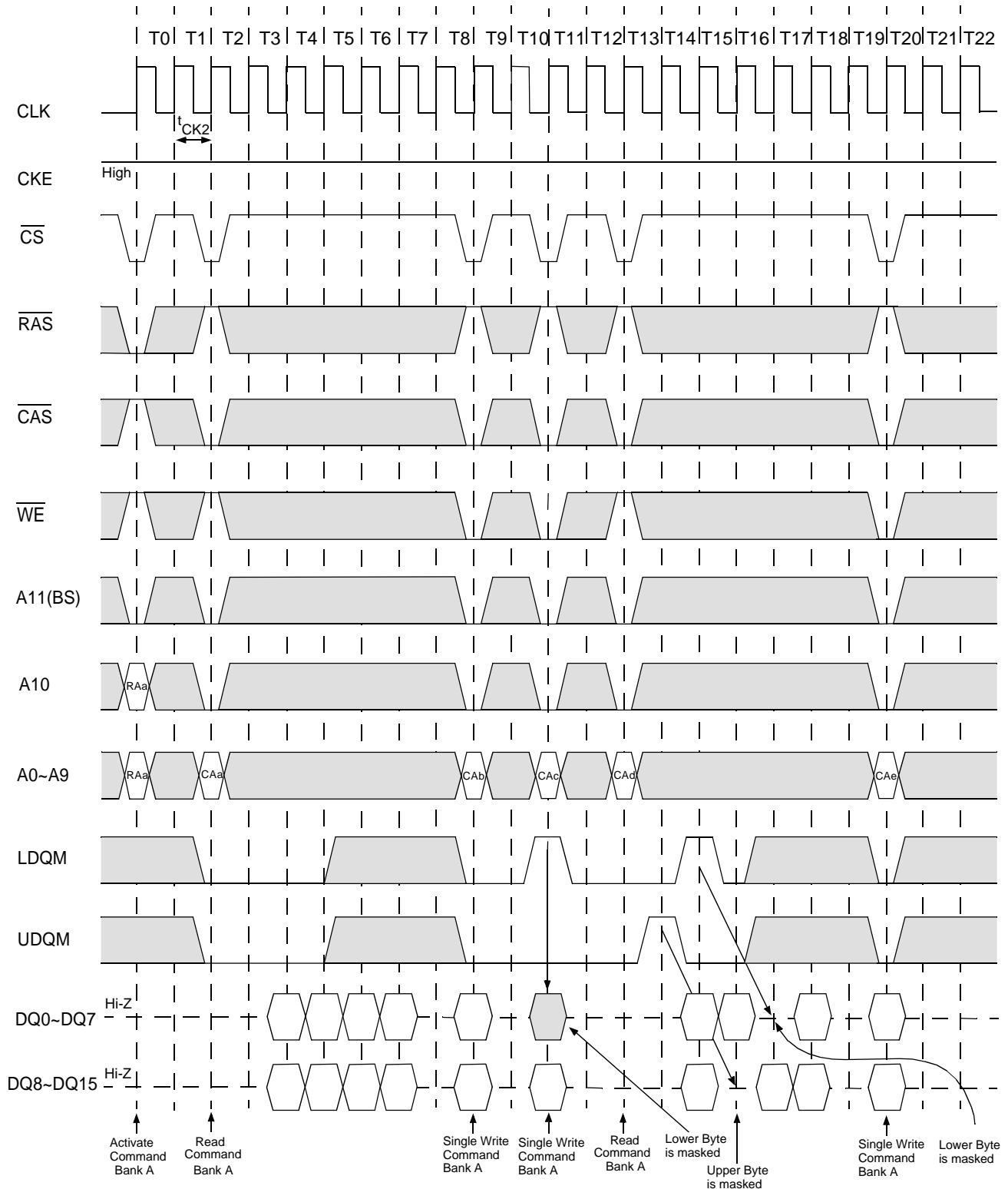
Byte Write Operation

Burst Length=4, $\overline{\text{CAS}}$ Latency=2



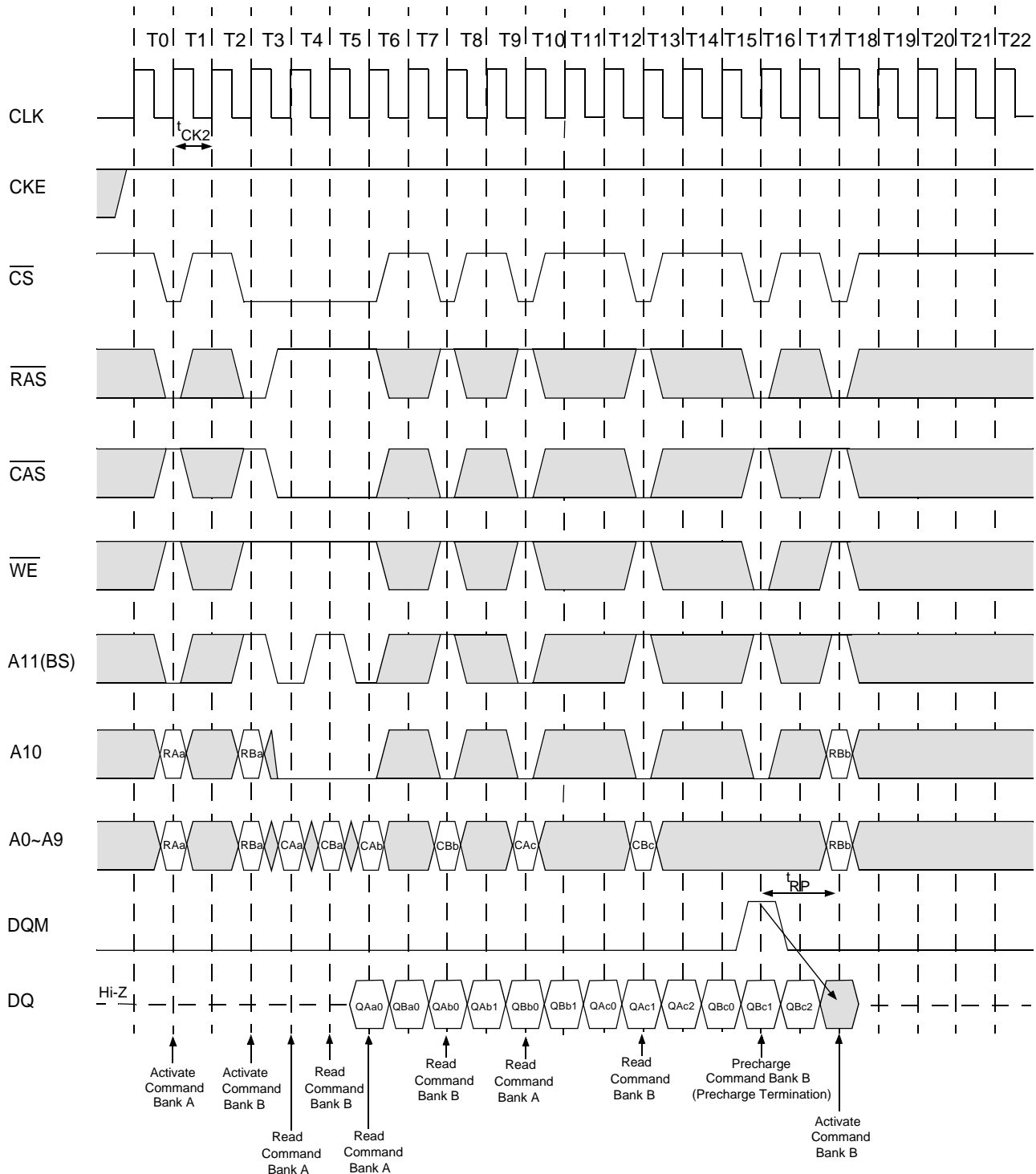
Burst Read and Single Write Operation

Burst Length=4, $\overline{\text{CAS}}$ Latency=2



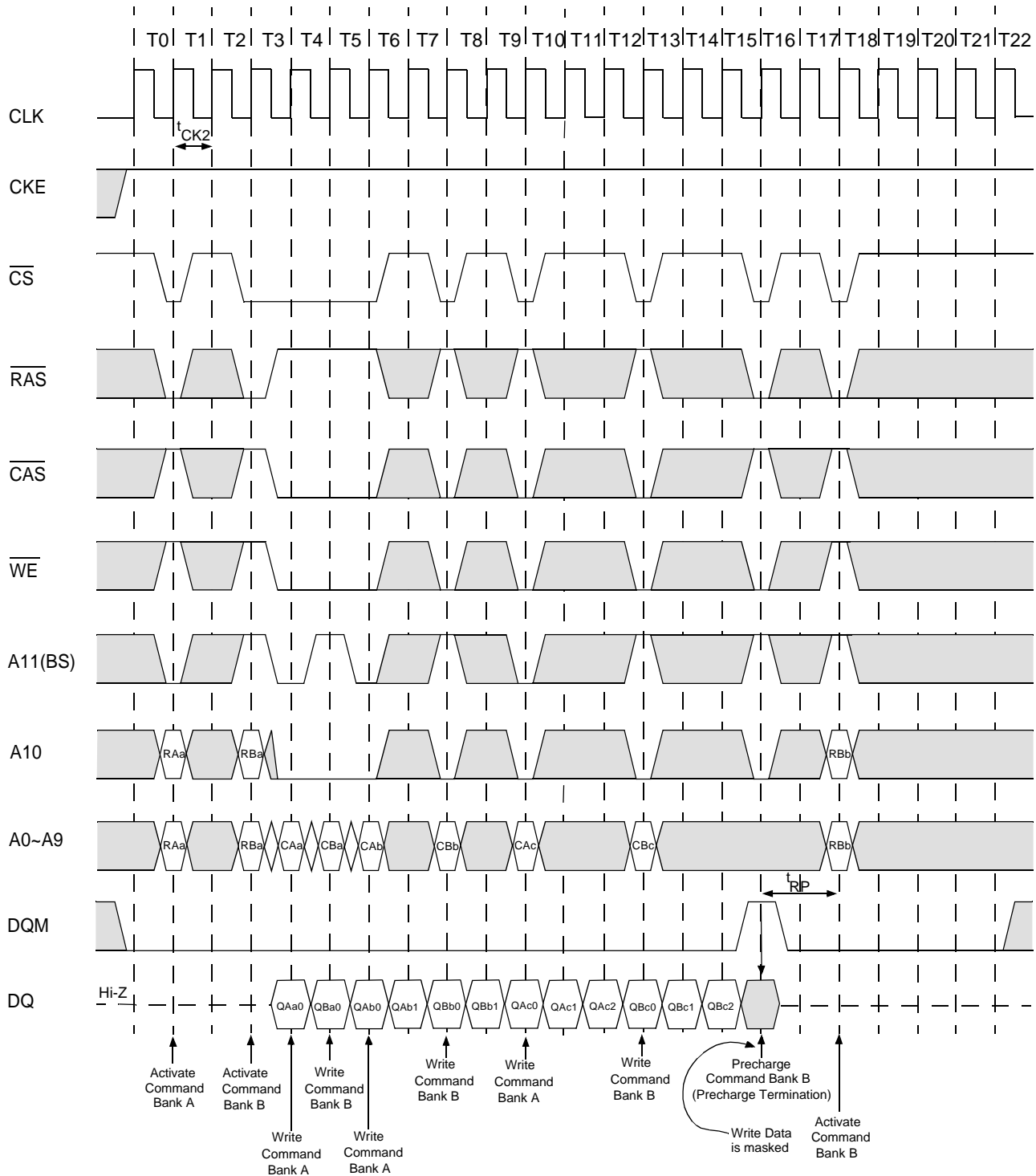
Full Page Random Column Read

Burst Length=Full Page, $\overline{\text{CAS}}$ Latency=2



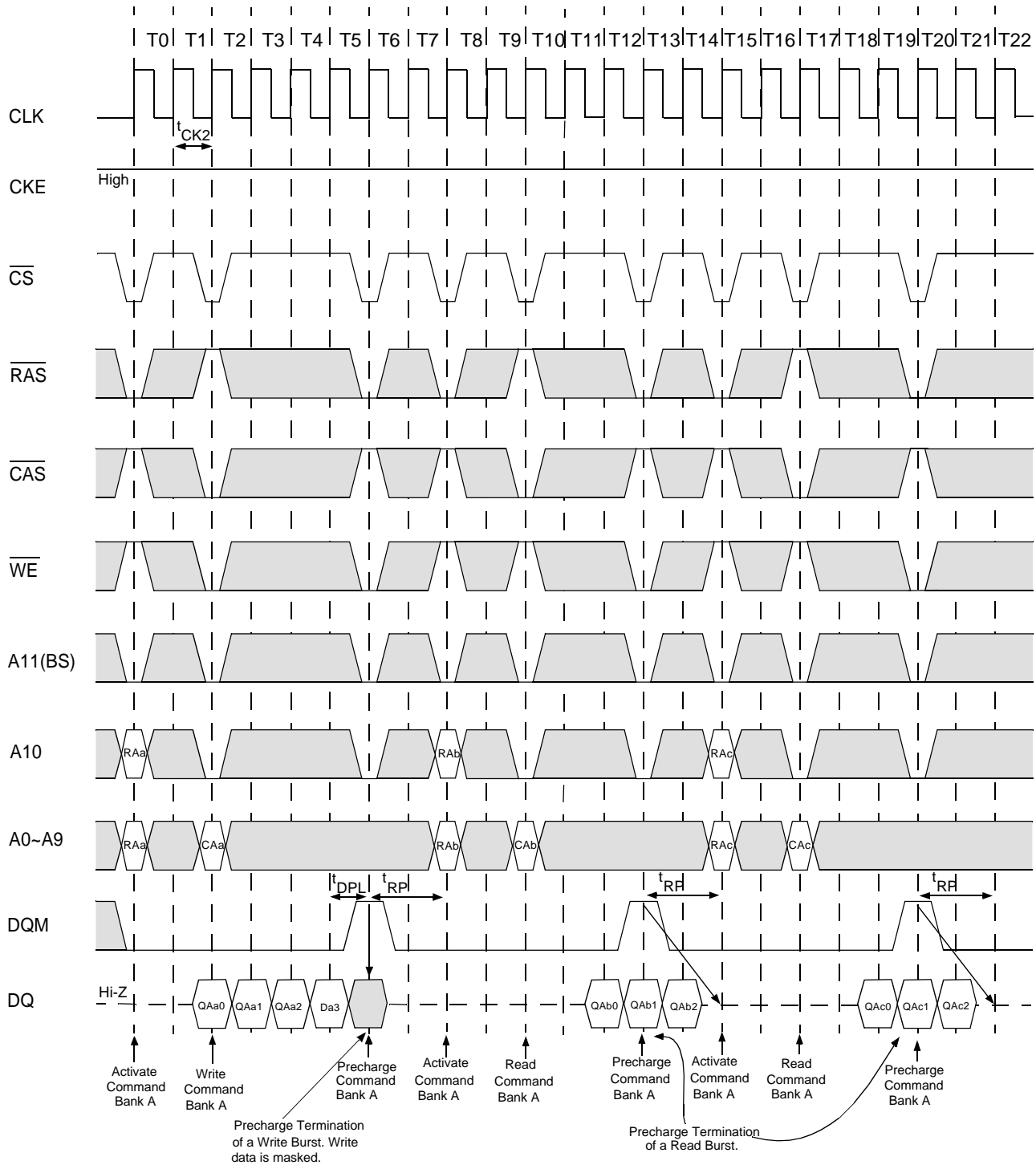
Full Page Random Column Write

Burst Length=Full Page, $\overline{\text{CAS}}$ Latency=2



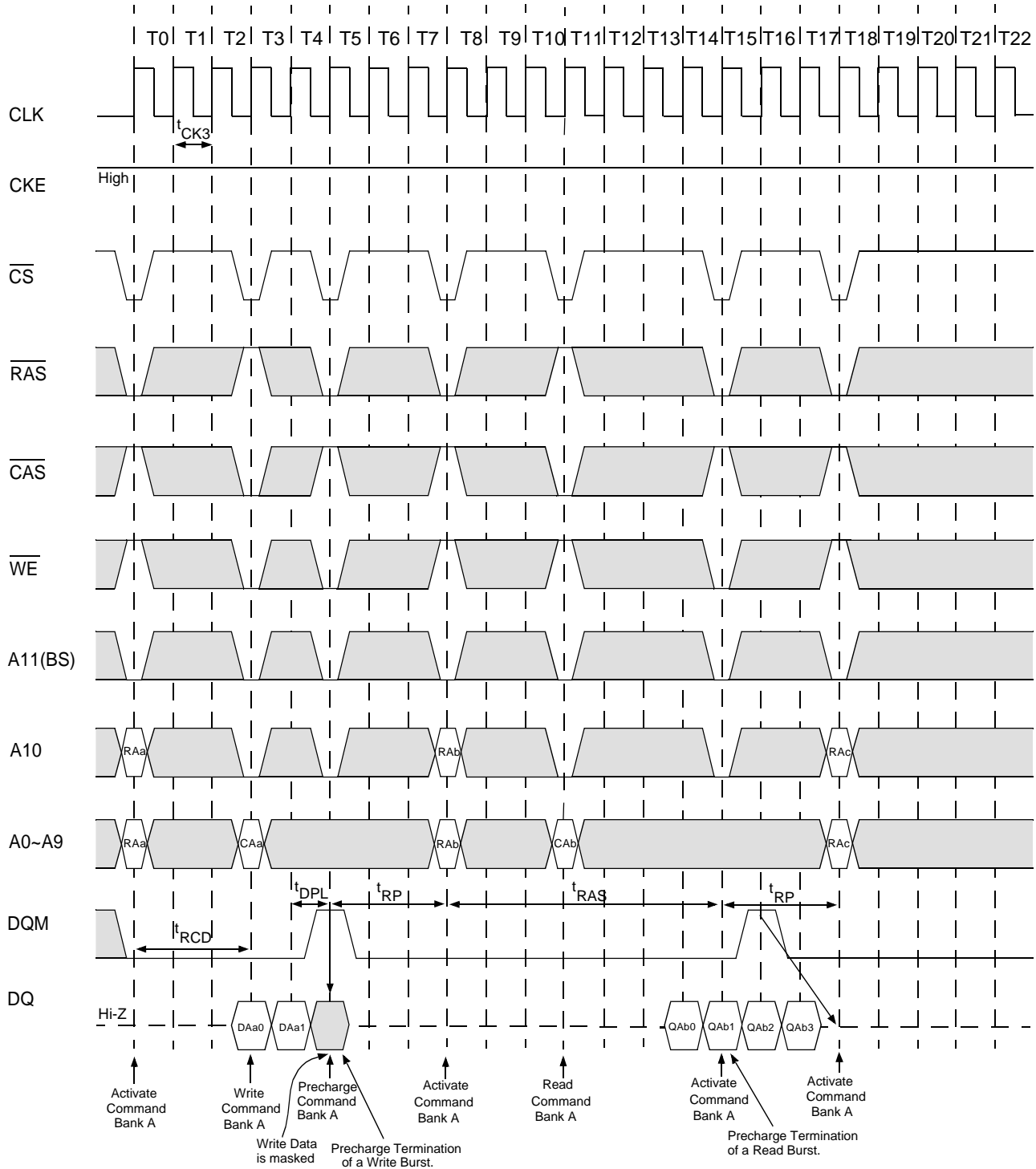
Precharge Termination of a Burst (1 of 2)

Burst Length=4,8 or Full Page, $\overline{\text{CAS}}$ Latency=2



Precharge Termination of a Burst (2 of 2)

Burst Length=4,8 or Full Page, $\overline{\text{CAS}}$ Latency=3



Ordering information

| Part Number | Cycle time | Package |
|----------------|------------|--------------|
| VG3617801BT-8H | 10ns | 400mil |
| VG3617801BT-8L | 10ns | 44-Pin |
| VG3617801BT-10 | 10ns | Plastic TSOP |

VG3617801BT-10

- VG → • VIS Memory Product
- 36 → • Technology/Design Rule
- 17801 → • Device Type/Configuration
- B → • Mask/Design Version
- T → • Package Type, T: TSOP
- 10 → • Cycle time, 10: 10ns, CL=2, tRP=2, tRCD=2 for PC 66
8L: 10ns, CL=3, tRP=2, tRCD=2 for PC 100
8H: 10ns, CL=2, tRP=2, tRCD=2 for PC 100

Packaging Information

- 400mil, 44-Pin Plastic TSOP

