



4 Megabyte Sync/Sync Burst, Dual Key DIMM

FEATURES

- 4x128Kx72 Synchronous, Synchronous Burst
- Flow-Through Architecture
- Linear and Sequential Burst Support via MODE pin
- Clock Controlled Registered Module Enable (EM#)
- Clock Controlled Registered Bank Enables (E1#, E2#, E3#, E4#)
- Clock Controlled Byte Write Mode Enable (BWE#)
- Clock Controlled Byte Write Enables (BW1# - BW8#)
- Clock Controlled Registered Address
- Clock Controlled Registered Global Write (GW#)
- Asynchronous Output Enable (G#)
- Internally Self-timed Write
- Individual Bank Sleep Mode enables (ZZ₁, ZZ₂, ZZ₃, ZZ₄)
- Gold Lead Finish
- 3.3V \pm 10% Operation
- Access Speed(s): TKHQV=8.5, 10, 12, 15ns
- Common Data I/O
- High Capacitance (30pf) drive, at rated Access Speed
- Single Total Array Clock
- Multiple Vcc and Gnd

DESCRIPTION

The EDI2CG472128VxxD2 is a Synchronous/Synchronous Burst SRAM, 84 position Dual Key; Double High DIMM (168 contacts) Module, organized as 4x128Kx72. The Module contains eight (8) Synchronous Burst Ram Devices, packaged in the industry standard JEDEC 14mmx20mm TQFP placed on a Multilayer FR4 Substrate. The module architecture is defined as a Sync/Sync Burst, Flow-Through, with support for either linear or sequential burst. This module provides High Performance, 2-1-1-1 accesses when used in Burst Mode, and used as a Synchronous Only Mode, provides a high performance cost advantage over BiCMOS asynchronous device architectures.

Synchronous Only operations are performed via strapping ADSC# Low, and ADSP# / ADV# High, which provides for Ultra Fast Accesses in Read Mode while providing for internally self-timed Early Writes.

Synchronous/Synchronous Burst operations are in relation to an externally supplied clock, Registered Address, Registered Global Write, Registered Enables as well as an Asynchronous Output enable. This Module has been defined with full flexibility, which allows individual control of each of the eight bytes, as well as Quad Words in both Read and Write Operations.

*This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.

**PIN CONFIGURATION**

PIN	FRONT	PIN	BACK
1	V _{SS}	85	V _{SS}
2	A0	86	A ₁₇
3	A ₁₆	87	A ₁
4	A ₂	88	A ₁₅
5	A ₁₄	89	A ₃
6	V _{CC}	90	V _{CC}
7	A ₄	91	A ₁₃
8	A ₁₂	92	A ₅
9	A ₆	93	A ₁₁
10	A ₁₀	94	A ₇
11	V _{SS}	95	V _{SS}
12	A ₈	96	A ₉
13	NC	97	NC ₃
14	E ₄ #	98	E ₁ #
15	E ₂ #	99	E ₃ #
16	V _{SS}	100	V _{SS}
17	MODE	101	CK
18	EM#	102	V _{SS}
19	GW#	103	G#
20	NC ₁	104	BWE#
21	V _{CC}	105	V _{CC}
22	BW ₄ #	106	BW ₂ #
23	BW ₃ #	107	BW ₁ #
24	BW ₆ #	108	BW ₆ #
25	BW ₇ #	109	BW ₅ #
26	ADSC#	110	V _{SS}
27	ADSP#	111	ADV#
28	V _{SS}	112	V _{SS}
29	NC	113	DQP ₀
30	V _{CC}	114	V _{CC}
31	DQ ₀	115	DQ ₇
32	DQ ₁	116	DQ ₆
33	DQ ₂	117	DQ ₅
34	DQ ₃	118	DQ ₄
35	V _{SS}	119	V _{SS}
36	ZZ ₁	120	DQP ₁
37	V _{CC}	121	V _{CC}
38	DQ ₈	122	DQ ₁₅
39	DQ ₉	123	DQ ₁₄
40	DQ ₁₀	124	DQ ₁₃
41	DQ ₁₁	125	DQ ₁₂
42	V _{SS}	126	V _{SS}

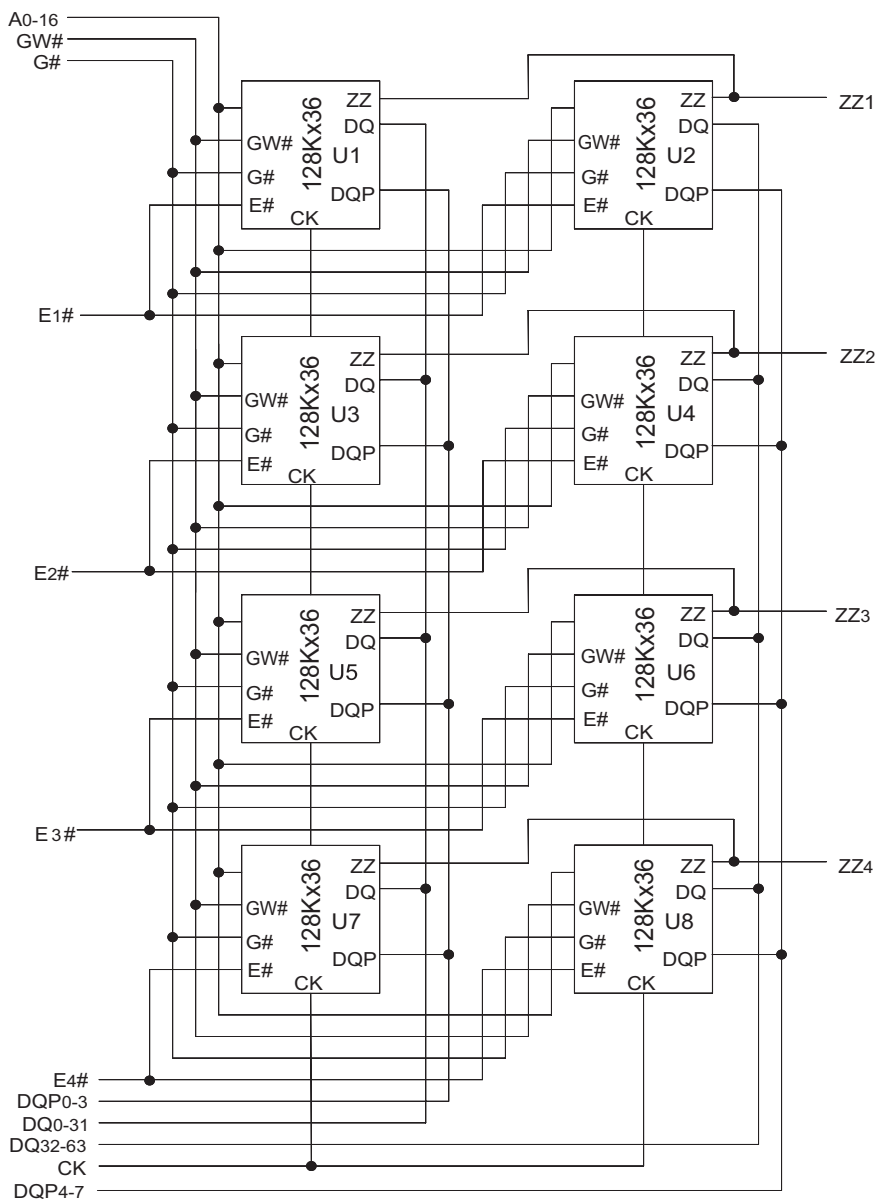
PIN	FRONT	PIN	BACK
43	NC	127	CRFU
44	V _{CC}	128	V _{CC}
45	DQ ₁₆	129	DQ ₂₃
46	DQ ₁₇	130	DQ ₂₂
47	DQ ₁₈	131	DQ ₂₁
48	DQ ₁₉	132	DQ ₂₀
49	V _{SS}	133	V _{SS}
50	ZZ ₂	134	DQP ₃
51	V _{CC}	135	V _{CC}
52	DQ ₂₄	136	DQ ₃₁
53	DQ ₂₅	137	DQ ₃₀
54	DQ ₂₆	138	DQ ₂₉
55	DQ ₂₇	139	DQ ₂₈
56	V _{SS}	140	V _{SS}
57	NC ₅	141	DQP ₄
58	V _{CC}	142	V _{CC}
59	DQ ₃₂	143	DQ ₃₉
60	DQ ₃₃	144	DQ ₃₈
61	DQ ₃₄	145	DQ ₃₇
62	DQ ₃₅	146	DQ ₃₆
63	V _{SS}	147	V _{SS}
64	ZZ ₃	148	DQP ₅
65	V _{CC}	149	V _{CC}
66	DQ ₄₀	150	DQ ₄₇
67	DQ ₄₁	151	DQ ₄₆
68	DQ ₄₂	152	DQ ₄₅
69	DQ ₄₃	153	DQ ₄₄
70	V _{SS}	154	V _{SS}
71	NC	155	DQP ₆
72	V _{CC}	156	V _{CC}
73	DQ ₄₈	157	DQ ₅₅
74	DQ ₄₉	158	DQ ₅₄
75	DQ ₅₀	159	DQ ₅₃
76	DQ ₅₁	160	DQ ₅₂
77	V _{SS}	161	V _{SS}
78	ZZ ₄	162	DQP ₇
79	V _{CC}	163	V _{CC}
80	DQ ₅₆	164	DQ ₆₃
81	DQ ₅₇	165	DQ ₆₂
82	DQ ₅₈	166	DQ ₆₁
83	DQ ₅₉	167	DQ ₆₀
84	V _{SS}	168	V _{SS}

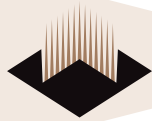
PIN NAMES

DQ0-DQ63	Input/Output Bus
DQP0-DQP7	Parity Bits
A0-A6	Address Bus
EM#	Module Enable
E1#, E2#, E3#, E4#	Synchronous Bank Enables
BWE#	Byte Write Mode Enable
BWE1#-BW8#	Byte Write Enables
CK	Array Clock
GW#	Synchronous Global Write Enable
G#	Asynchronous Output Enable
ZZ1, ZZ2, ZZ3, ZZ4	Blank Sleep Mode Enables
V _{CC}	3.3V Power Supply
V _{SS}	Ground



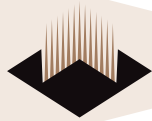
FUNCTIONAL BLOCK DIAGRAM





PIN DESCRIPTIONS

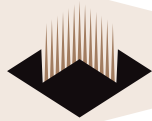
DIMM Pins	Symbol	Type	Description
2, 87, 4, 89, 7, 92, 9, 94, 12, 96, 10, 93, 8, 91, 5, 88, 3	A0-A16	Input Synchronous	Addresses: These inputs are registered and must meet the setup and hold times around the rising edge of CK. The burst counter generates internal addresses associated with A0 and A1, during burst and wait cycle.
107, 106, 23, 22, 109, 108, 25, 24	BW1#, BW2#, BW3#, BW4#, BW5#, BW6#, BW7#, BW8#	Input Synchronous	Byte Write: A byte write is LOW for a WRITE cycle and HIGH for a READ cycle. BW0/ controls DQ0-7 and DQP0, BW1# controls DQ8-15 and DQP1. BW2# controls DQ16-23 and DQP2. BW3# controls DQ24-31 and DQP3. BW4# controls DQ32-39 and DQP4. BW5# controls DQ40-47 and DQP5. BW6# controls DQ48-55 and DQP6. BW7# controls DQ56-64 and DQP7.
104	BWE#	Input Synchronous	Write Enable: This active LOW input gates byte write operations and must meet the setup and hold times around the rising edge of CK.
19	GW#	Input Synchronous	Global Write: This active LOW input allows a full 72-bit WRITE to occur independent of the BWE# and BWx# lines and must meet the setup and hold times around the rising edge of CK.
101	CK	Input Synchronous	Clock: This signal registers the addresses, data, chip enables, write control and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
98, 15, 99, 14	E1#, E2#, E3#, E4#	Input Synchronous	Bank Enables: These active LOW inputs are used to enable each individual bank and to gate ADSP#.
103	G#	Input	Output Enable: This active LOW asynchronous input enables the data output drivers.
111	ADV#	Input Synchronous	Address Status Processor: This active LOW input is used to control the internal burst counter. A HIGH on this pin generates wait cycle (no address advance).
27	ADSP#	Input Synchronous	Address Status Processor: This active LOW input, along with EL# and EH# being LOW, causes a new external address to be registered and a READ cycle is initiated using the new address.
26	ADSC#	Input Synchronous	Address Status Controller: This active LOW input causes device to be de-selected or selected along with new external address to be registered. A READ or WRITE cycle is initiated depending upon write control inputs.
17	MODE	Input Static	Mode: This input selects the burst sequence. A LOW on this pin selects LINEAR BURST. A NC or HIGH on this pin selects INTERLEAVED BURST.
36, 50, 64, 78	ZZ1, ZZ2, ZZ3, ZZ4	Input Asynchronous	Snooze: These active HIGH inputs put the individual banks in low power consumption standby mode. For normal operation, this input has to be either LOW or NC (no connect).
Various	DQ0-63	Input/Output	Data Inputs/Outputs: First byte is DQ0-7, second byte is DQ8-15, third byte is DQ16-23, fourth byte is DQ24-31, fifth byte is DQ32-39, sixth byte is DQ40-47, seventh byte is DQ48-55 and the eight byte is DQ56-64.
113, 120, 127, 134, 141, 148, 155, 162	DQP0-7	Input/Output	Parity Inputs/Outputs: DQP0 is parity bit for DQ0-7. DQP1 is parity bit for DQ8-15. DQP2 is parity bit for DQ16-23. DQP3 is parity bit for DQ24-31. DQP4# is parity bit for DQ-32-39. DQP5 is parity bit for DQ40-47. DQP6# is parity bit for DQ48-55. DQP7 is parity bit for DQ56-64 and DQP7. In order to use the device configured as a 128K x 64, the parity bits need to be tied to Vss through a 10K ohm resistor.
Various	Vcc	Supply	Core Power supply: +3.3V -5%/+10%
Various	Vss	Ground	Ground



SYNCHRONOUS BURST - TRUTH TABLE

Operation	E1#	E2#	E3#	E4#	ADSP#	ADSC#	ADV#	GW#	G#	CK	DQ	Addr. Used
Deselected Cycle, Power Down; Bank 1	H	X	*	*	X	L	X	X	X	L-H	High-Z	None
Deselected Cycle, Power Down; Bank 2	X	H	*	*	X	L	X	X	X	L-H	High-Z	None
Read Cycle, Begin Burst; Bank 1	L	H	*	*	L	X	X	X	L	L-H	Q	External
Read Cycle, Begin Burst; Bank 1	L	H	*	*	L	X	X	X	H	L-H	High-Z	External
Read Cycle, Begin Burst; Bank 2	H	L	*	*	L	X	X	X	L	L-H	Q	External
Read Cycle, Begin Burst; Bank 2	H	L	*	*	L	X	X	X	H	L-H	High-Z	External
Write Cycle, Begin Burst; Bank 1	L	H	*	*	H	L	X	L	X	L-H	D	External
Write Cycle, Begin Burst; Bank 2	H	L	*	*	H	L	X	L	X	L-H	D	External
Read Cycle, Begin Burst; Bank 1	L	H	*	*	H	L	X	H	L	L-H	Q	External
Read Cycle, Begin Burst; Bank 1	L	H	*	*	H	L	X	H	H	L-H	High-Z	External
Read Cycle, Begin Burst; Bank 2	H	L	*	*	H	L	X	H	L	L-H	Q	External
Read Cycle, Begin Burst; Bank 2	H	L	*	*	H	L	X	H	H	L-H	High-Z	External
Read Cycle, Continue Burst; Bank 1	X	H	*	*	X	H	L	H	L	L-H	Q	Next
Read Cycle, Continue Burst; Bank 1	X	H	*	*	X	H	L	H	H	L-H	High-Z	Next
Read Cycle, Continue Burst; Bank 2	H	X	*	*	X	H	L	H	L	L-H	Q	Next
Read Cycle, Continue Burst; Bank 2	H	X	*	*	X	H	L	H	H	L-H	High-Z	Next
Read Cycle, Continue Burst; Bank 1	H	H	*	*	X	H	L	H	L	L-H	Q	Next
Read Cycle, Continue Burst; Bank 1	H	H	*	*	X	H	L	H	H	L-H	High-Z	Next
Read Cycle, Continue Burst; Bank 2	H	H	*	*	X	H	L	H	L	L-H	Q	Next
Read Cycle, Continue Burst; Bank 2	H	H	*	*	X	H	L	H	H	L-H	High-Z	Next
Write Cycle, Continue Burst; Bank 1	X	H	*	*	H	H	L	L	X	L-H	D	Next
Write Cycle, Continue Burst; Bank 1	H	H	*	*	X	H	L	L	X	L-H	D	Next
Write Cycle, Continue Burst; Bank 2	H	X	*	*	H	H	L	L	X	L-H	D	Next
Write Cycle, Continue Burst; Bank 2	H	H	*	*	X	H	L	L	X	L-H	D	Next
Read Cycle, Suspend Burst; Bank 1	X	H	*	*	H	H	H	H	L	L-H	Q	Current
Read Cycle, Suspend Burst; Bank 1	X	H	*	*	H	H	H	H	H	L-H	High-Z	Current
Read Cycle, Suspend Burst; Bank 2	H	X	*	*	H	H	H	H	L	L-H	Q	Current
Read Cycle, Suspend Burst; Bank 2	H	X	*	*	H	H	H	H	H	L-H	High-Z	Current
Read Cycle, Suspend Burst; Bank 1	H	H	*	*	X	H	H	H	L	L-H	Q	Current
Read Cycle, Suspend Burst; Bank 1	H	H	*	*	X	H	H	H	H	L-H	High-Z	Current
Read Cycle, Suspend Burst; Bank 2	H	H	*	*	X	H	H	H	L	L-H	Q	Current
Read Cycle, Suspend Burst; Bank 2	H	H	*	*	X	H	H	H	H	L-H	High-Z	Current
Write Cycle, Suspend Burst; Bank 1	X	H	*	*	H	H	H	L	X	L-H	D	Current
Write Cycle, Suspend Burst; Bank 1	H	H	*	*	X	H	H	L	X	L-H	D	Current
Write Cycle, Suspend Burst; Bank 2	H	X	*	*	H	H	H	L	X	L-H	D	Current
Write Cycle, Suspend Burst; Bank 2	H	H	*	*	X	H	H	L	X	L-H	D	Current

*All Truth Table Functions Repeat for Bank 3 (E3#) and Bank 4 (E4#)



SYNCHRONOUS ONLY - TRUTH TABLE

Operation	E1#	E2#	E3#	E4#	GW#	G#	ZZ	CK	DQ
Synchronous Write-Bank 1	L	H	H	H	L	H	L	↑	High-Z
Synchronous Read-Bank 1	L	H	H	H	H	L	L	↑	
Synchronous Write-Bank 2	H	L	H	H	L	H	L	↑	High-Z
Synchronous Read-Bank 2	H	L	H	H	H	L	L	↑	
Synchronous Write-Bank 3	H	H	L	H	L	H	L	↑	High-Z
Synchronous Read-Bank 3	H	H	L	H	H	L	L	↑	
Synchronous Write-Bank 4	H	H	H	L	L	H	L	↑	High-Z
Synchronous Read-Bank 4	H	H	H	L	H	L	L	↑	
Snooze Mode	X	X	X	X	X	X	H	X	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Relative to Vss	-0.5V to +4.6V
V _{IN}	-0.5V to V _{CC} +0.5V
Storage Temperature	-55°C to +125°C
Operating Temperature (Commercial)	0°C to +70°C
Operating Temperature (Industrial)	-40°C to +85°C
Short Circuit Output Current	10 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in operational sections of this specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	V _{CC}	3.14	3.3	3.6	V
Supply Voltage	V _{SS}	0.0	0.0	0.0	V
Input High	V _{IH}	1.1	3.0	V _{CC} +0.3	V
Input Low	V _{IL}	-0.3	0.0	0.3	V
Input Leakage	I _{LI}	-2	1	2	μA
Output Leakage	I _{LO}	-2	1	2	μA

DC ELECTRICAL CHARACTERISTICS - READ CYCLE

Description	SYM	Typ	8.5	10	12	15	Units
Power Supply Current	I _{CC1}	2.0	2.9	2.7	2.7	2.5	A
Power Supply Current Device Selected, No Operation	I _{CC}	875	1.8	1.8	1.3	1.3	A
Snooze Mode	I _{CCZZ}	500	700	700	700	700	mA
CMOS Standby	I _{CC3}	270	350	350	350	350	mA
Clock Running-Deselect	I _{CCK}	900	1.1	1.1	1.0	1.0	A

AC TEST CONDITIONS

Input Pulse Levels	V _{SS} to 3.0V
Input and Output Timing Ref.	1.25V
Output Test equivalencies	

AC TEST LOAD

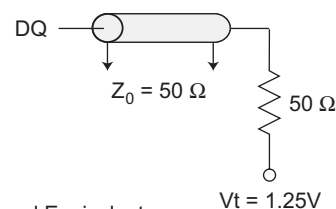


Fig. 1 Output Load Equivalent



BURST ADDRESS TABLE (MODE=NC/V_{CC})

First Address (external)	Second Address (internal)	Third Address (internal)	Fourth Address (internal)
A-A00	A-A01	A-A10	A-A11
A-A01	A-A00	A-A11	A-A10
A-A10	A-A11	A-A00	A-A01
A-A11	A-A10	A-A01	A-A00

BURST ADDRESS TABLE (MODE=GND)

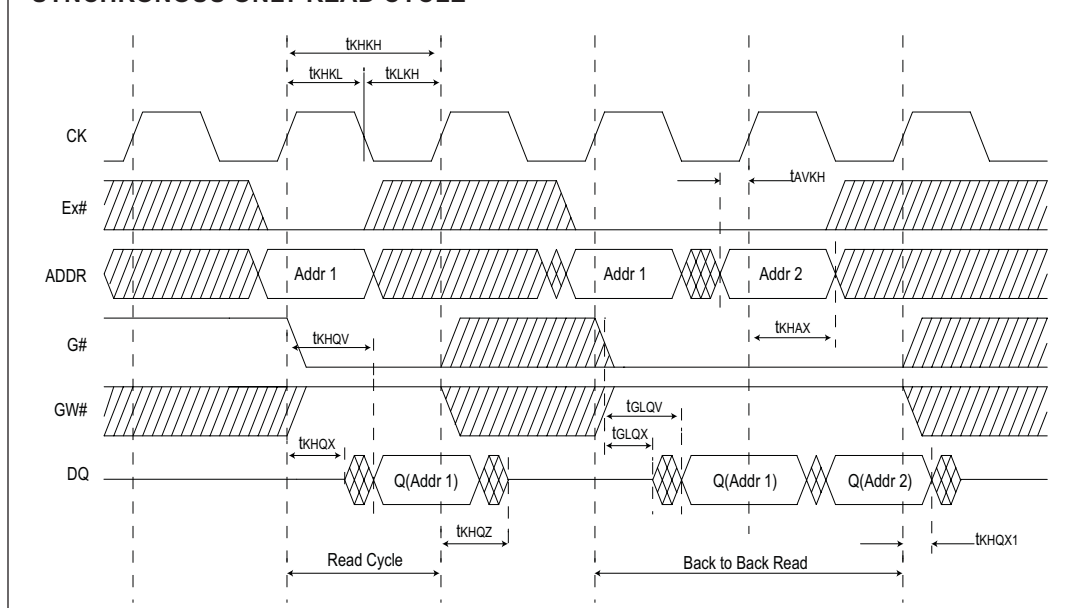
First Address (external)	Second Address (internal)	Third Address (internal)	Fourth Address (internal)
A-A00	A-A01	A-A10	A-A11
A-A01	A-A10	A-A11	A-A00
A-A10	A-A11	A-A00	A-A01
A-A11	A-A00	A-A01	A-A10

READ CYCLE TIMING PARAMETERS

Description	Sym	8.5ns		10ns		12ns		15ns		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Clock Cycle Time	t _{KHKH}	*	*	15		15		20		ns
Clock High Time	t _{KHKL}	*	*	5		5		6		ns
Clock Low Time	t _{KLKH}	*	*	5		5		6		ns
Clock to Output Valid	t _{KHQP}	*	*		10		12		15	ns
Clock to Output Invalid	t _{KHQX1}	*	*	3		3		3		ns
Clock to Output Low-Z	t _{KHQX}	*	*	4		4		4		ns
Output Enable to Output Valid	t _{GLQP}	*	*		5		5		6	ns
Output Enable to Output Low-Z	t _{GLQX}	*	*	0		0		0		ns
Output Enable to Output High-Z	t _{GHQZ}	*	*		5		5		5	ns
Address Setup	t _{AVKH}	*	*	2.5		2.5		2.5		ns
Bank Enable Setup	t _{EVKH}	*	*	2.5		2.5		2.5		ns
Address Hold	t _{KHAX}	*	*	1.0		1.0		1.0		ns
Bank Enable Hold	t _{KHEX}	*	*	1.0		1.0		1.0		ns

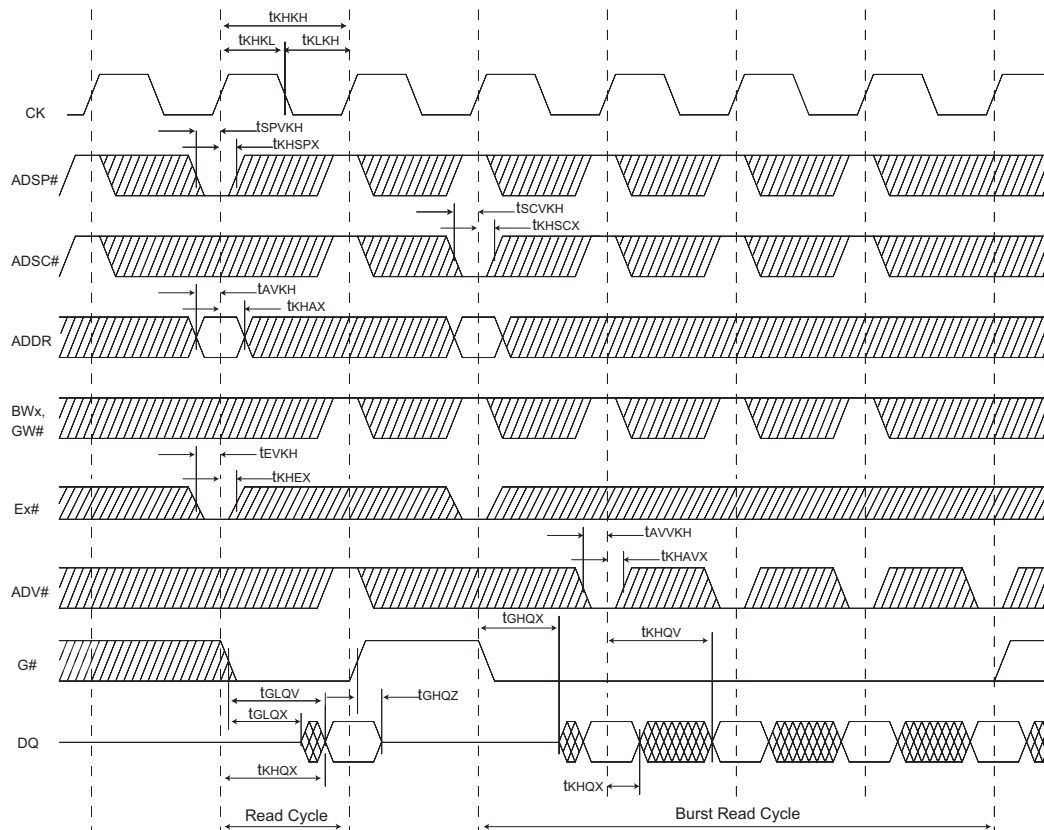
*TBD

SYNCHRONOUS ONLY READ CYCLE





SYNC-BURST READ CYCLE



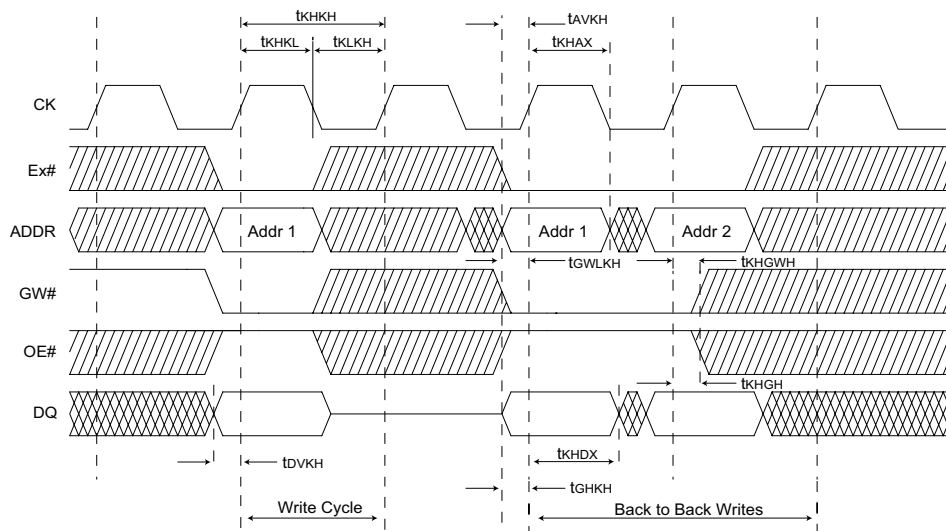
WRITE CYCLE TIMING PARAMETERS

Description	Sym	8.5ns		10ns		12ns		15ns		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Clock Cycle Time	tKHKH	*	*	15		15		20		ns
Clock High Time	tKHKL	*	*	5		5		6		ns
Clock Low Time	tKCLKH	*	*	5		5		6		ns
Address Setup	tAVKH	*	*	2.5		2.5		2.5		ns
Address Hold	tKHAX	*	*	1.0		1.0		1.0		ns
Bank Enable Setup	tEVKH	*	*	2.5		2.5		2.5		ns
Bank Enable Hold	tKHEX	*	*	1.0		1.0		1.0		ns
Global Write Enable Setup	tWVKH	*	*	2.5		2.5		2.5		ns
Global Write Enable Hold	tKHGX	*	*	1.0		1.0		1.0		ns
Data Setup	tDVKH	*	*	2.5		2.5		2.5		ns
Data Hold	tKHDX	*	*	1.0		1.0		1.0		ns

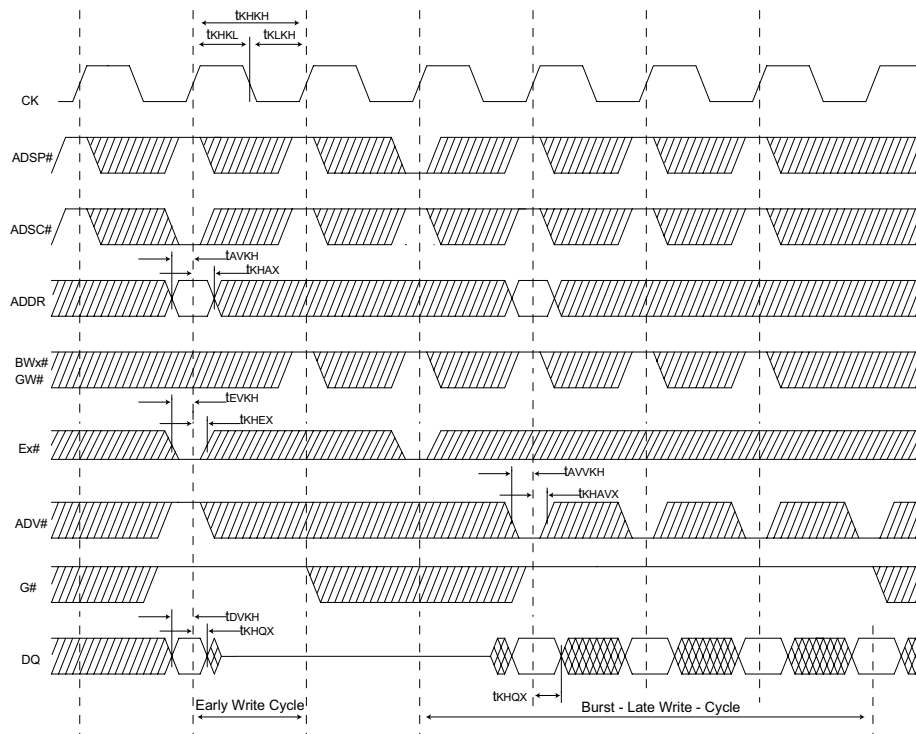
*TBD



SYNC (NON-BURST) WRITE CYCLE

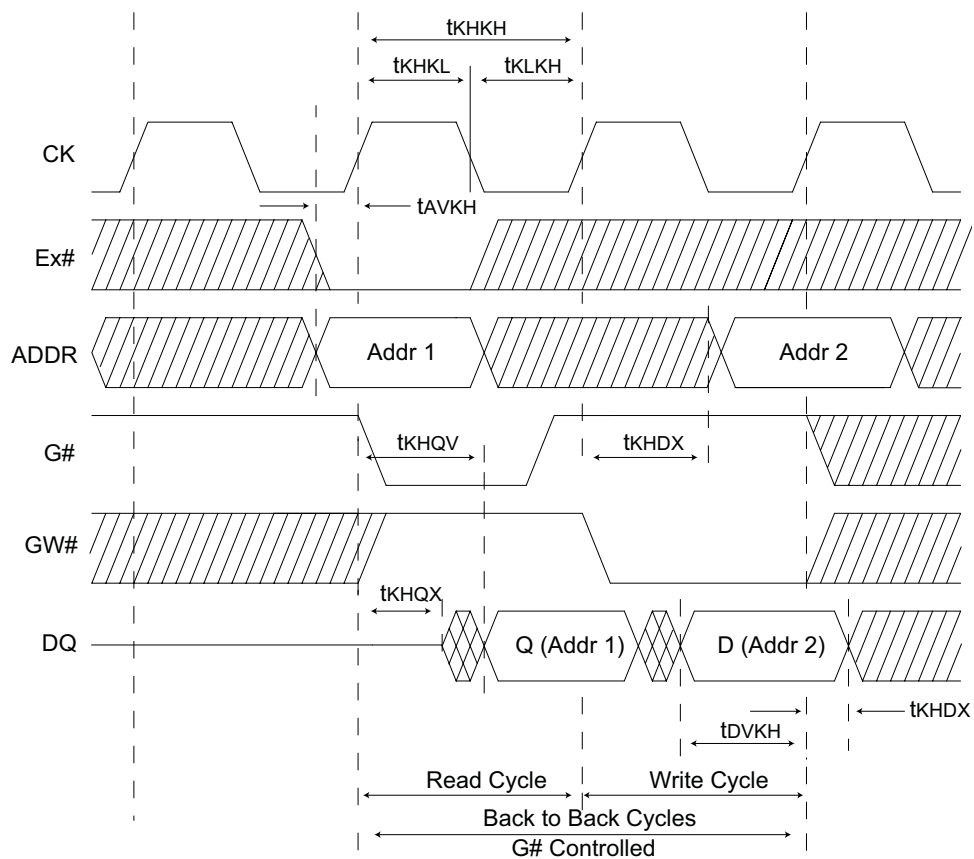


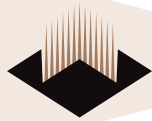
SYNCBURST WRITE CYCLE





SYNC (NON-BURST) READ/WRITE CYCLE



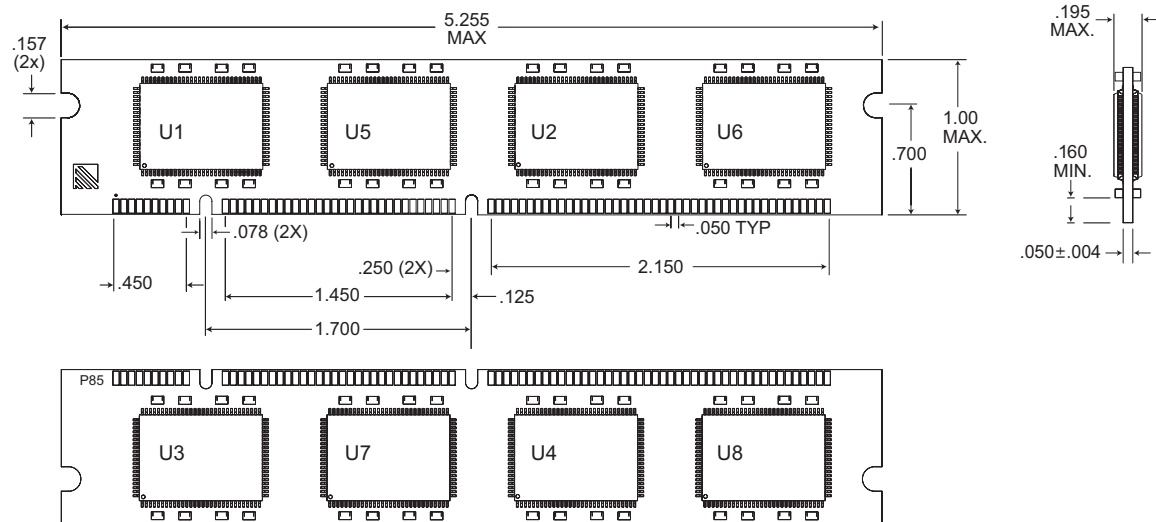


PACKAGE DESCRIPTION

Package No. 410

168 Lead

Dual Key DIMM



ORDERING INFORMATION

Part Number	Organization	Voltage	Speed (ns)	Package
EDI2CG472128V85D2*	4x128Kx72	3.3	8.5	168 Gold Lead DIMM
EDI2CG472128V10D2*	4x128Kx72	3.3	10	168 Gold Lead DIMM
EDI2CG472128V12D2	4x128Kx72	3.3	12	168 Gold Lead DIMM
EDI2CG472128V15D2	4x128Kx72	3.3	15	168 Gold Lead DIMM

*Consult Factory for Availability