



128KX8 MONOLITHIC SRAM, SMD 5962-89598

FEATURES

- Access Times of 70, 85, 100ns
- Available with Single Chip Selects (EDI88128) or Dual Chip Selects (EDI88130)
- 2V Data Retention (LP Versions)
- \overline{CS} and \overline{OE} Functions for Bus Control
- TTL Compatible Inputs and Outputs
- Fully Static, No Clocks
- Organized as 128Kx8
- Industrial, Military and Commercial Temperature Ranges
- Thru-hole and Surface Mount Packages JEDEC Pinout
 - 32 pin Ceramic DIP, 0.6 mils wide (Package 9)
 - 32 lead Ceramic SOJ (Package 140)
- Single +5V ($\pm 10\%$) Supply Operation

The EDI88128C is a high speed, high performance, Monolithic CMOS Static RAM organized as 128Kx8.

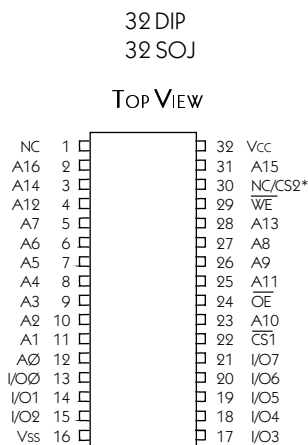
The device is also available as EDI88130C with an additional chip select line (CS₂) which will automatically power down the device when proper logic levels are applied.

The second chip select line (CS₂) can be used to provide system memory security during power down in non-battery backed up systems and simplify decoding schemes in memory banking where large multiple pages of memory are required.

The EDI88128C and the EDI88130C have eight bi-directional input-output lines to provide simultaneous access to all bits in a word. An automatic power down feature permits the on-chip circuitry to enter a very low standby mode and be brought back into operation at a speed equal to the address access time.

Low power versions, EDI88128LP and EDI88130LP, offer a 2V data retention function for battery back-up operation. Military product is available compliant to Appendix A of MIL-PRF-38535.

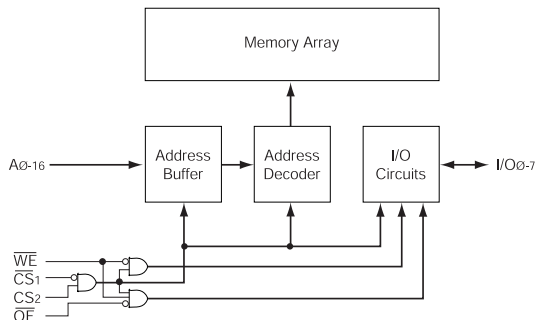
FIG. 1 PIN CONFIGURATION



PIN DESCRIPTION

I/O0-7	Data Inputs/Outputs
A0-16	Address Inputs
\overline{WE}	Write Enable
$\overline{CS}_1, \overline{CS}_2$	Chip Selects
\overline{OE}	Output Enable
Vcc	Power (+5V $\pm 10\%$)
Vss	Ground
NC	Not Connected

BLOCK DIAGRAM



* Pin 30 is NC for 88128 or CS2 for 88130.



ABSOLUTE MAXIMUM RATINGS

Parameter		Unit
Voltage on any pin relative to Vss	-0.5 to 7.0	V
<u>Operating Temperature T_A (Ambient)</u>		
Commercial	0 to +70	°C
Industrial	-40 to +85	°C
Military	-55 to +125	°C
Storage Temperature, Plastic	-65 to +150	°C
Power Dissipation	1	W
Output Current	20	mA
Junction Temperature, T _J	175	°C

NOTE:

Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C)

Parameter	Symbol	Condition	Max	Unit
Address Lines	C _I	V _{IN} = V _{CC} or V _{SS} , f = 1.0MHz	12	pF
Input/Output Lines	C _O	V _{OUT} = V _{CC} or V _{SS} , f = 1.0MHz	14	pF

These parameters are sampled, not 100% tested.

DC CHARACTERISTICS (V_{CC} = 5V, T_A = -55°C TO +125°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Leakage Current	I _I	V _{IN} = 0V to V _{CC}	-5	—	+5	μA
Output Leakage Current	I _{LO}	V _{IO} = 0V to V _{CC} , $\overline{CS}_1 \geq V_{IH}$ and/or $\overline{CS}_2 \leq V_{IL}$	-10	—	+10	μA
Operating Power Supply Current	I _{CC1}	\overline{WE} , $\overline{CS}_1 = V_{IL}$, I _{IO} = 0mA, Min Cycle (70-85ns) $\overline{CS}_2 = V_{IH}$ (100ns)	—	—	120	mA
Standby (TTL) Power Supply Current	I _{CC2}	$\overline{CS}_1 \geq V_{IH}$ and/or $\overline{CS}_2 \leq V_{IL}$, V _{IN} ≥ V _{IH} or ≤ V _{IL}	—	—	110	mA
Full Standby Power Supply Current	I _{CC3}	$\overline{CS}_1 \geq V_{CC} - 0.2V$ and/or $\overline{CS}_2 \leq V_{CC} + 0.2V$	—	1	5	mA
		V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V	—	—	1	mA
Output Low Voltage	V _{OL}	I _{OL} = 2.1mA	—	—	0.4	V
Output High Voltage	V _{OH}	I _{OH} = -1.0mA	2.4	—	—	V

NOTE: DC test conditions : V_{IL} = 0.3V, V_{IH} = V_{CC} - 0.3V

TRUTH TABLE

\overline{OE}	\overline{CS}_1	\overline{CS}_2	\overline{WE}	Mode	Output	Power
X	H	X	X	Standby	High Z	I _{CC2} , I _{CC3}
X	X	L	X	Standby	High Z	I _{CC2} , I _{CC3}
X	X	L	X	Output Deselect	High Z	I _{CC1}
H	L	H	H	Output Deselect	High Z	I _{CC1}
L	L	H	H	Read	Data Out	I _{CC1}
X	L	H	L	Write	Data In	I _{CC1}

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Supply Voltage	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.2	—	V _{CC} + 0.5	V
Input Low Voltage	V _{IL}	-0.3	—	+0.8	V



AC CHARACTERISTICS – READ CYCLE ($V_{CC} = 5.0V$, $V_{SS} = 0V$, $T_A = -55^{\circ}C$ TO $+125^{\circ}C$)

Parameter	Symbol		70ns		85ns		100ns		Units
	JEDEC	Alt	Min	Max	Min	Max	Min	Max	
Read Cycle Time	tAVAV	tRC	70		85		100		ns
Address Access Time	tAVQV	tAA		70		85		100	ns
Chip Select Access Time	tELQV	tACS		70		85		100	ns
	tSHQV	tACS		70		85		100	ns
Chip Select to Output in Low Z (1)	tELQX	tCLZ	3		3		3		ns
	tSHQX	tCLZ	3		3		3		ns
Chip Disable to Output in High Z (1)	tEHQZ	tCHZ	0	30	0	30	0	30	ns
	tSLQZ	tCHZ	0	30	0	30	0	30	ns
Output Hold from Address Change	tAVQX	tOH	3		3		3		ns
Output Enable to Output Valid	tGLQV	tOE		25		30		50	ns
Output Enable to Output in Low Z (1)	tGLQX	tOLZ	0		0		0		ns
Output Disable to Output in High Z (1)	tGHQZ	tCHZ	0	30	0	30	0	30	ns

1. This parameter is guaranteed by design but not tested.

AC TEST CONDITIONS

Figure 1

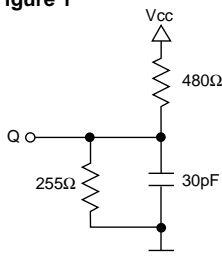
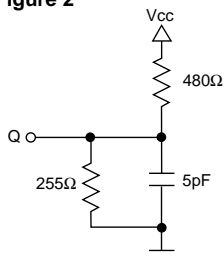


Figure 2



Input Pulse Levels	V_{SS} to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	Figure 1

NOTE: For tEHQZ, tGHQZ and tWLQZ, $C_L = 5pF$ Figure 2)



AC CHARACTERISTICS – WRITE CYCLE (V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C TO +125°C)

Parameter	Symbol		70ns		85ns		100ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	
Write Cycle Time	tAVAV	tWC	70		85		100		ns
Chip Select to End of Write	tELWH	tCW	60		75		85		ns
	tELEH	tCW	60		75		85		ns
	tSHWH	tCW	60		75		85		ns
	tSHSL	tCW	60		75		85		ns
Address Setup Time	tAVWL	tAS	0		0		0		ns
	tAVEL	tAS	0		0		0		ns
	tAVSH	tAS	0		0		0		ns
Address Valid to End of Write	tAVWH	tAW	60		75		85		ns
Write Pulse Width	tWLWH	tWP	35		70		80		ns
	tWLEH	tWP	35		70		80		ns
	tWLSL	tWP	35		70		80		ns
Write Recovery Time	tWHAX	tWR	5		5		5		ns
	tEHAX	tWR	5		5		5		ns
	tSLAX	tWR	5		5		5		ns
Data Hold Time	tWHDX	tDH	0		0		0		ns
	tEHDX	tDH	0		0		0		ns
	tSLDX	tDH	0		0		0		ns
Write to Output in High Z (1)	tWLQZ	tWHZ	0	30	0	35	0	40	ns
Data to Write Time	tDVWH	tDW	35		40		40		ns
	tDVEH	tDW	35		40		40		ns
	tDVSL	tDW	35		40		40		ns
Output Active from End of Write (1)	tWHQX	tWLZ	5		5		5		ns

1. This parameter is guaranteed by design but not tested.



FIG. 2 TIMING WAVEFORM - READ CYCLE

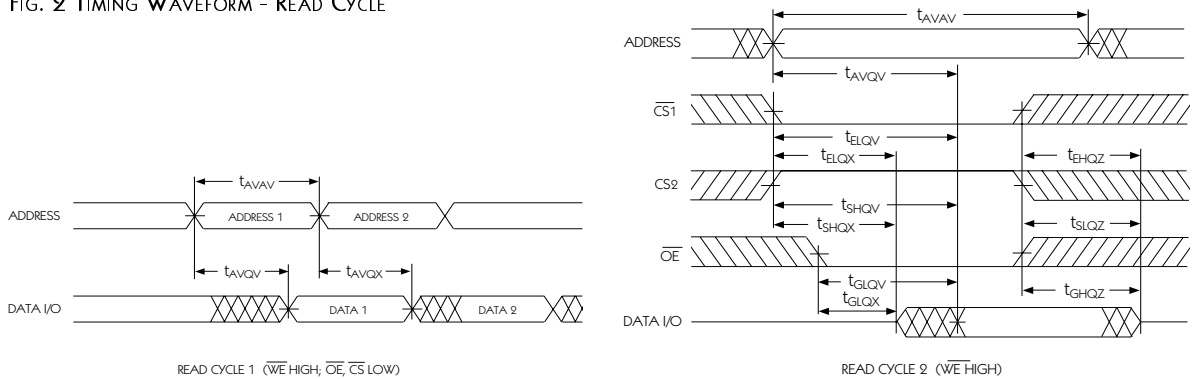


FIG. 3 WRITE CYCLE 1

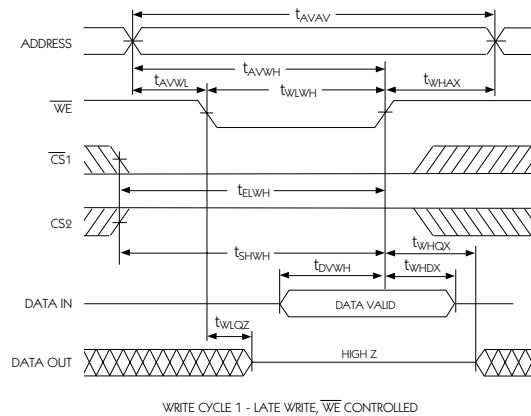
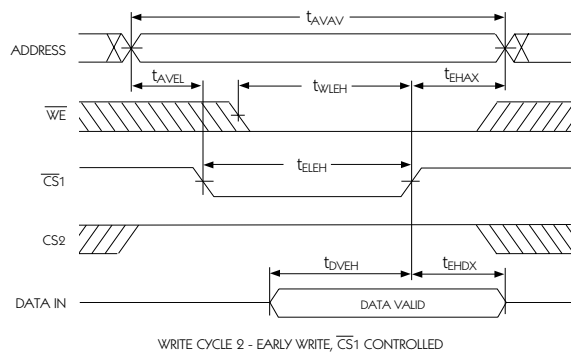
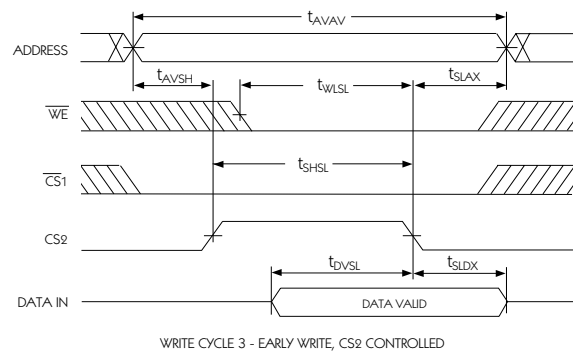


FIG. 4 WRITE CYCLE 2



WRITE CYCLE 3





DATA RETENTION CHARACTERISTICS (EDI88128LP & EDI88130LP ONLY) ($T_A = -55^{\circ}\text{C}$ TO $+125^{\circ}\text{C}$)

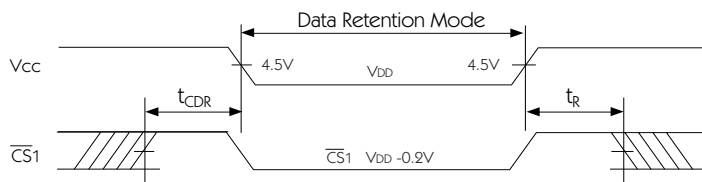
Characteristic	Sym	Conditions	Min	Typ	Max	Units
Low Power Version only						
Data Retention Voltage	V_{DD}	$V_{DD} = 2.0\text{V}$	2	—	—	V
Data Retention Quiescent Current	I_{CCDR}	$\overline{CS}1 \geq V_{DD} - 0.2\text{V}$	—	—	400	μA
Chip Disable to Data Retention Time (1)	T_{CDR}	$V_{IN} \geq V_{DD} - 0.2\text{V}$	0	—	—	ns
Operation Recovery Time (1)	T_R	or $V_{IN} \leq 0.2\text{V}$	T_{AVAV}^*	—	—	ns

NOTE:

1. Parameter guaranteed by design, but not tested.

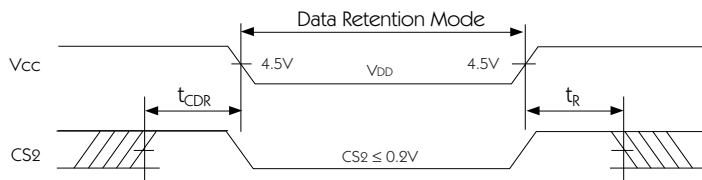
* Read Cycle Time

FIG. 5 DATA RETENTION - $\overline{CS}1$ CONTROLLED

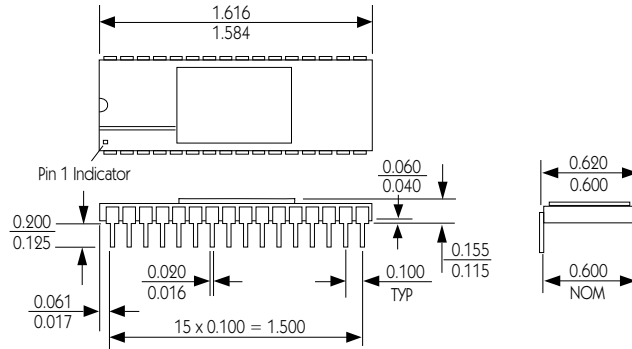


DATA RETENTION, $\overline{CS}1$ CONTROLLED

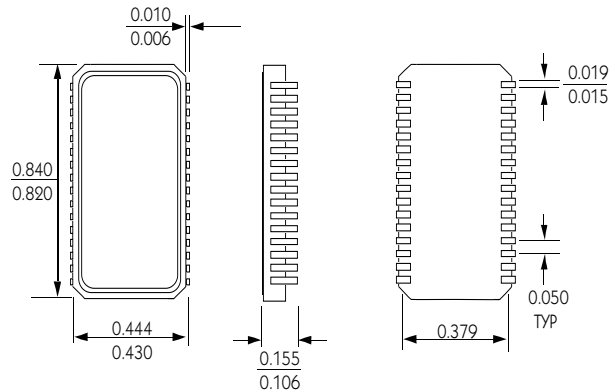
FIG. 6 DATA RETENTION - $CS2$ CONTROLLED



DATA RETENTION, $CS2$ CONTROLLED

**PACKAGE 9: 32 PIN SIDEBRAZED CERAMIC DIP (600MILS WIDE)**

ALL Dimensions ARE in inches

PACKAGE 140: 32 LEAD CERAMIC SOJ

ALL Dimensions ARE in inches



EDI 8 8 128 C X X X