



## 512MB- 64Mx72 SDRAM UNBUFFERED

### FEATURES

- PC100 and PC133 Compatible
- Burst Mode Operation
- Auto and Self Refresh capability
- LVTTTL compatible inputs and outputs
- Serial Presence Detect with EEPROM
- Fully synchronous: All signals are registered on the positive edge of the system clock
- Programmable Burst Lengths: 1, 2, 4, 8 or Full Page
- 3.3V  $\pm$  0.3V Power Supply
- 144 Pin SO-DIMM
  - Package height option:  
AD1: 27.94 (1.10")

### DESCRIPTION

The W3DG7268V is a 64Mx72 synchronous DRAM module which consists of nine 64Mx8 SDRAM components in TSOP II package, and one 2K EEPROM in an 8 pin TSSOP package for Serial Presence Detect which are mounted on a 144 Pin SO-DIMM multilayer FR4 Substrate.

\* This product is under development, is not qualified or characterized and is subject to change without notice.

### PIN CONFIGURATIONS (FRONT SIDE/BACK SIDE)

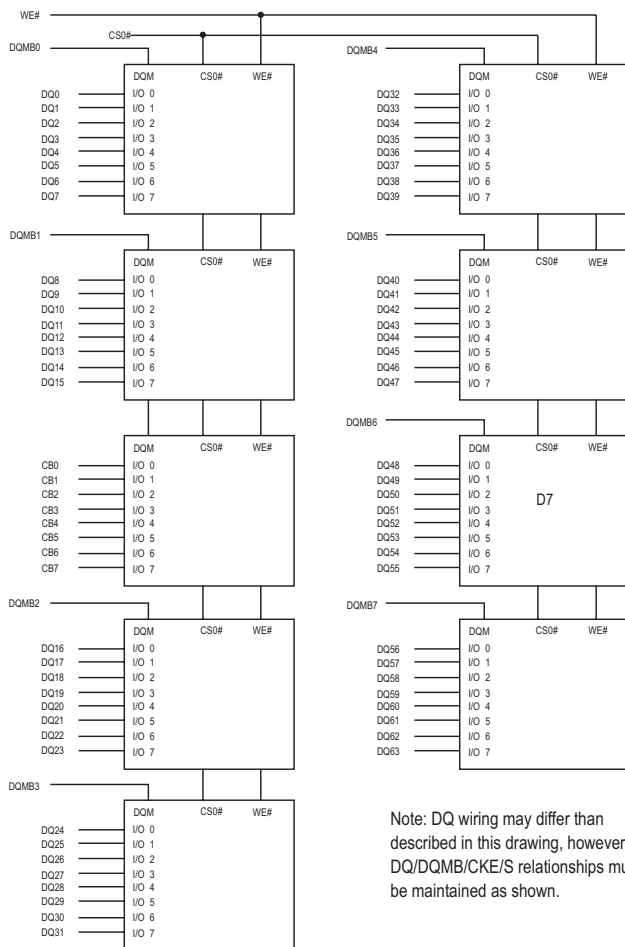
PIN	FRONT	PIN	BACK	PIN	FRONT	PIN	BACK	PIN	FRONT	PIN	BACK
1	V <sub>SS</sub>	2	V <sub>SS</sub>	49	DQ13	50	DQ45	97	DQ22	98	DQ54
3	DQ0	4	DQ32	51	DQ14	52	DQ46	99	DQ23	100	DQ55
5	DQ1	6	DQ33	53	DQ15	54	DQ47	101	V <sub>CC</sub>	102	V <sub>CC</sub>
7	DQ2	8	DQ34	55	V <sub>SS</sub>	56	V <sub>SS</sub>	103	A6	104	A7
9	DQ3	10	DQ35	57	CB0	58	CB4	105	A8	106	BA0
11	V <sub>CC</sub>	12	V <sub>CC</sub>	59	CB1	60	CB5	107	V <sub>SS</sub>	108	V <sub>SS</sub>
13	DQ4	14	DQ36	61	CLK0	62	CKE0	109	A9	110	BA1
15	DQ5	16	DQ37	63	V <sub>CC</sub>	64	V <sub>CC</sub>	111	A10	112	A11
17	DQ6	18	DQ38	65	RAS#	66	CAS#	113	V <sub>CC</sub>	114	V <sub>CC</sub>
19	DQ7	20	DQ39	67	WE#	68	NC	115	DQMB2	116	DQMB6
21	V <sub>SS</sub>	22	V <sub>SS</sub>	69	CS0#	70	A12	117	DQMB3	118	DQMB7
23	DQMB0	24	DQB4	71	NC	72	NC	119	V <sub>SS</sub>	120	V <sub>SS</sub>
25	DQMB1	26	DQB5	73	NC	74	CLK1	121	DQ24	122	DQ56
27	V <sub>CC</sub>	28	V <sub>CC</sub>	75	V <sub>SS</sub>	76	V <sub>SS</sub>	123	DQ25	124	DQ57
29	A0	30	A3	77	CB2	78	CB6	125	DQ26	126	DQ58
31	A1	32	A4	79	CB3	80	CB7	127	DQ27	128	DQ59
33	A2	34	A5	81	V <sub>CC</sub>	82	V <sub>CC</sub>	129	V <sub>CC</sub>	130	V <sub>CC</sub>
35	V <sub>SS</sub>	36	V <sub>SS</sub>	83	DQ16	84	DQ48	131	DQ28	132	DQ60
37	DQ8	38	DQ40	85	DQ17	86	DQ49	133	DQ29	134	DQ61
39	DQ9	40	DQ41	87	DQ18	88	DQ50	135	DQ30	136	DQ62
41	DQ10	42	DQ42	89	DQ19	90	DQ51	137	DQ31	138	DQ63
43	DQ11	44	DQ43	91	V <sub>SS</sub>	92	V <sub>SS</sub>	139	V <sub>SS</sub>	140	V <sub>SS</sub>
45	V <sub>CC</sub>	46	V <sub>CC</sub>	93	DQ20	94	DQ52	141	SDA	142	SCL
47	DQ12	48	DQ44	95	DQ21	96	DQ53	143	V <sub>CC</sub>	144	V <sub>CC</sub>

### PIN NAMES

A0 – A12	Address input (Multiplexed)
BA0-1	Select Bank
DQ0-63	Data Input/Output
CB0-7	Check bit (Data-in/data-out)
CLK0,CK1	Clock input
CKE0	Clock Enable input
CS0#	Chip select Input
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
DQMB0-7	DQM
V <sub>CC</sub>	Power Supply (3.3V)
V <sub>SS</sub>	Ground
SDA	Serial data I/O
SCL	Serial clock
DNU	Do not use
NC	No Connect

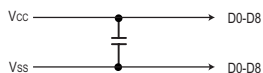


### FUNCTIONAL BLOCK DIAGRAM



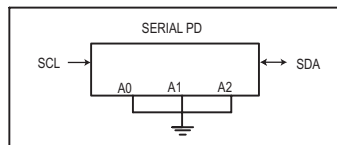
Note: DQ wiring may differ than described in this drawing, however DQ/DQMB/CKE/S relationships must be maintained as shown.

RAS# → RAS#: SDRAM D0-D8  
CAS# → CAS#: SDRAM D0-D8  
CKE0 → CKE: SDRAM D0-D8  
BA0-BA1 → BA0-BA1: SDRAM D0-D8  
A0-A12 → A0-A12: SDRAM D0-D8



*CLOCK WIRING	
CLOCK INPUT	SDRAMS
*CLK0	5 SDRAMS
*CLK1	4 SDRAMS

\*Wire per Clock Loading Table/Wiring Diagrams





## ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Units
Voltage on any pin relative to V <sub>SS</sub>	V <sub>IN</sub> , V <sub>OUT</sub>	-1.0 ~ 4.6	V
Voltage on V <sub>CC</sub> supply relative to V <sub>SS</sub>	V <sub>CC</sub> , V <sub>CCQ</sub>	-1.0 ~ 4.6	V
Storage Temperature	T <sub>STG</sub>	-55 ~ +150	°C
Power Dissipation	P <sub>D</sub>	9	W
Short Circuit Current	I <sub>OS</sub>	50	mA

Note: Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.

Functional operation should be restricted to recommended operating condition.

Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

## RECOMMENDED DC OPERATING CONDITIONS

Voltage Referenced to: V<sub>SS</sub> = 0V, 0°C ≤ T<sub>A</sub> ≤ +70°C

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V <sub>CC</sub>	3.0	3.3	3.6	V	
Input High Voltage	V <sub>IH</sub>	2.0	3.0	V <sub>CCQ</sub> +0.3	V	1
Input Low Voltage	V <sub>IL</sub>	-0.3	—	0.8	V	2
Output High Voltage	V <sub>OH</sub>	2.4	—	—	V	I <sub>OH</sub> = -2mA
Output Low Voltage	V <sub>OL</sub>	—	—	0.4	V	I <sub>OL</sub> = +2mA
Input Leakage Current	I <sub>LI</sub>	-10	—	10	μA	3

Note:

1. V<sub>IH</sub> (max)= 5.6V AC. The overshoot voltage duration is ≤ 3ns.

2. V<sub>IL</sub> (min)= -2.0V AC. The undershoot voltage duration is ≤ 3ns.

3. Any input 0V ≤ V<sub>IN</sub> ≤ V<sub>CCQ</sub>

Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

## CAPACITANCE

T<sub>A</sub> = 25°C, f = 1MHz, V<sub>CC</sub> = 3.3V, V<sub>REF</sub> = 1.4V ± 200mV

Parameter	Symbol	Max	Unit
Input Capacitance (A0-A12)	C <sub>IN1</sub>	36	pF
Input Capacitance (RAS#,CAS#,WE#)	C <sub>IN2</sub>	36	pF
Input Capacitance (CKE0)	C <sub>IN3</sub>	36	pF
Input Capacitance (CK0)	C <sub>IN4</sub>	20	pF
Input Capacitance (CS0#)	C <sub>IN5</sub>	36	pF
Input Capacitance (DQM0-DQM7)	C <sub>IN6</sub>	7	pF
Input Capacitance (BA0-BA1)	C <sub>IN7</sub>	36	pF
Data Input/Output Capacitance (DQ0-DQ63)	C <sub>OUT</sub>	9	pF
Data input/output capacitance (CB0-CB7)	C <sub>OUT1</sub>	9	pF

**OPERATING CURRENT CHARACTERISTICS** $V_{CC} = 3.3V$ ,  $0^{\circ}C \leq T_A \leq +70^{\circ}C$ 

			Version		
Parameter	Symbol	Conditions	100/133	Units	Note
Operating Current (One bank active)	I <sub>CC1</sub>	Burst Length = 1 $t_{RC} \leq t_{RC(min)}$ $I_{OL} = 0mA$	1080	mA	1
Precharge Standby Current in Power Down Mode	I <sub>CC2</sub>	$CKE \leq V_{IL(max)}$ , $t_{CC} = 10ns$	35	mA	
Active Standby Current in Power-Down Mode	I <sub>CC3</sub>	$CKE \geq V_{IL(max)}$ , $t_{CC} = 10ns$	405	mA	
Operating Current (Burst mode)	I <sub>CC4</sub>	$I_O = mA$ Page burst 4 Banks activated $t_{CCD} = 2CK$	1125	mA	1
Refresh Current	I <sub>CC5</sub>	$t_{RC} \geq t_{RC(min)}$	2205	mA	2
Self Refresh Current	I <sub>CC6</sub>	$CKE \leq 0.2V$	54	mA	

## Notes:

1. Measured with outputs open.
2. Refresh period is 64ms.



### ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

AC CHARACTERISTICS			7		75/10			
PARAMETER		SYMBOL	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from CLK (pos. edge)	CL = 3	t <sub>AC(3)</sub>		5.4		5.4	ns	27
	CL = 2	t <sub>AC(2)</sub>		5.4		6	ns	
Address hold time		t <sub>AH</sub>	0.8		0.8		ns	
Address setup time		t <sub>AS</sub>	1.5		1.5		ns	
CLK high-level width		t <sub>CH</sub>	2.5		2.5		ns	
CLK low-level width		t <sub>CL</sub>	2.5		2.5		ns	
Clock cycle time	CL = 3	t <sub>CK(3)</sub>	7		7.5		ns	23
	CL = 2	t <sub>CK(2)</sub>	7.5		10		ns	23
CKE hold time		t <sub>CKH</sub>	0.8		0.8		ns	
CKE setup time		t <sub>CKS</sub>	1.5		1.5		ns	
CS#, RAS#, CAS#, WE#, DQM hold time		t <sub>CMH</sub>	0.8		0.8		ns	
CS#, RAS#, CAS#, WE#, DQM setup time		t <sub>CMS</sub>	1.5		1.5		ns	
Data-in hold time		t <sub>DH</sub>	0.8		0.8		ns	
Data-in setup time		t <sub>DS</sub>	1.5		1.5		ns	
Data-out high-impedance time	CL = 3	t <sub>HZ(3)</sub>		5.4		5.4	ns	10
	CL = 2	t <sub>HZ(2)</sub>		5.4		6	ns	10
Data-out low-impedance time		t <sub>LZ</sub>	1		1		ns	
Data-out hold time (load)		t <sub>OH</sub>	2.7		2.7		ns	
Data-out hold time (no load)		t <sub>OHN</sub>	1.8		1.8		ns	28
ACTIVE to PRECHARGE command		t <sub>RAS</sub>	37	120K	44	120K	ns	
ACTIVE to ACTIVE command period		t <sub>RC</sub>	60		66		ns	
ACTIVE to READ or WRITE delay		t <sub>RCD</sub>	15		20		ns	
Refresh period (8,192 rows)		t <sub>REF</sub>		64		64	ms	
AUTO REFRESH period		t <sub>RFC</sub>	66		66		ns	
PRECHARGE command period		t <sub>RP</sub>	15		20		ns	
ACTIVE bank a to ACTIVE bank b command		t <sub>R RD</sub>	14		15		ns	
Transition time		t <sub>T</sub>	0.3	1.2	0.3	1.2	ns	7
WRITE recovery time		t <sub>WR</sub>	1 CLK + 7ns		1 CLK + 7ns		-	24
			14		15		ns	14, 25
Exit SELF REFRESH to ACTIVE command		t <sub>XS R</sub>	67		75		ns	20

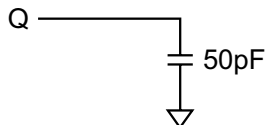
**AC FUNCTIONAL CHARACTERISTICS**

PARAMETER		SYMBOL	7	75/10	UNITS	NOTES
READ/WRITE command to READ/WRITE command		t <sub>CCD</sub>	1	1	t <sub>CK</sub>	17
CKE to clock disable or power-down entry mode		t <sub>CKED</sub>	1	1	t <sub>CK</sub>	14
CKE to clock enable or power-down exit setup mode		t <sub>PED</sub>	1	1	t <sub>CK</sub>	14
DQM to input data delay		t <sub>DQD</sub>	0	0	t <sub>CK</sub>	17
DQM to data mask during WRITES		t <sub>DQM</sub>	0	0	t <sub>CK</sub>	17
DQM to data high-impedance during READs		t <sub>DQZ</sub>	2	2	t <sub>CK</sub>	17
WRITE command to input data delay		t <sub>DWD</sub>	0	0	t <sub>CK</sub>	17
Data-in to ACTIVE command		t <sub>DAL</sub>	4	5	t <sub>CK</sub>	15, 21
Data-in to PRECHARGE command		t <sub>DPL</sub>	2	2	t <sub>CK</sub>	16, 21
Last data-in to burst STOP command		t <sub>BDL</sub>	1	1	t <sub>CK</sub>	17
Last data-in to new READ/WRITE command		t <sub>CDL</sub>	1	1	t <sub>CK</sub>	17
Last data-in to PRECHARGE command		t <sub>RDL</sub>	2	2	t <sub>CK</sub>	16, 21
LOAD MODE REGISTER command to ACTIVE or REFRESH command		t <sub>M RD</sub>	2	2	t <sub>CK</sub>	26
Data-out to high-impedance from PRECHARGE command	CL = 3	t <sub>ROH(3)</sub>	3	3	t <sub>CK</sub>	17
	CL = 2	t <sub>ROH(2)</sub>	2	2	t <sub>CK</sub>	17



## Notes

1. All voltages referenced to  $V_{SS}$ .
2. This parameter is sampled.  $V_{CC}$ ,  $V_{CCQ} = +3.3V$ ;  $= 25^{\circ}C$ ; pin under test biased at 1.4V.  $f = 1$  MHz,  $T_A$
3.  $I_{DD}$  is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ( $0^{\circ}C \leq \leq 70^{\circ}C$ ) is  $T_A$  ensured.
6. An initial pause of 100 $\mu s$  is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. ( $V_{CC}$  and  $V_{CCQ}$  must be powered up simultaneously.  $V_{SS}$  and  $V_{SSQ}$  must be at same potential.) The two AUTO REFRESH command wake-ups should be repeated any time the  $t_{REF}$  refresh requirement is exceeded.
7. AC characteristics assume  $t_r = 1ns$ .
8. In addition to meeting the transition rate specification, the clock and CKE must transit between  $V_{IH}$  and  $V_{IL}$  (or between  $V_{IL}$  and  $V_{IH}$ ) in a mono-tonic manner.
9. Outputs measured at 1.5V with equivalent load:



10.  $t_{HZ}$  defines the time at which the output achieves the open circuit condition; it is not a reference to  $V_{OH}$  or  $V_{OL}$ . The last valid data element will meet  $t_{OH}$  before going High-Z.
11. AC timing and  $I_{DD}$  tests have  $V_{IL} = 0V$  and  $V_{IH} = 3V$ , with timing referenced to 1.5V crossover point. If the input transition time is longer than 1ns, then the timing is referenced at  $V_{IL}$  (MAX) and  $V_{IH}$  (MIN) and no longer at the 1.5V crossover point.
12. Other input signals are allowed to transition no more than once every two clocks and are other-wise at valid  $V_{IH}$  or  $V_{IL}$  levels.
13.  $I_{DD}$  specifications are tested after the device is properly initialized.
14. Timing actually specified by  $t_{CKS}$ ; clock(s) specified as a reference only at minimum cycle rate.
15. Timing actually specified by  $t_{WR}$  plus  $t_{RP}$ ; clock(s) specified as a reference only at minimum cycle rate.
16. Timing actually specified by  $t_{WR}$ .
17. Required clocks are specified by JEDEC functionality and are not dependent on any timing parameter.
18. The  $I_{DD}$  current will increase or decrease in a proportional amount by the amount the frequency is altered for the test condition.
19. Address transitions average one transition every two clocks.
20. CLK must be toggled a minimum of two times during this period.
21. Based on  $t_{CK} = 7.5ns$  for 75/10 and 7.
22.  $V_{IH}$  overshoot:  $V_{IH}$  (MAX) =  $V_{CCQ} + 2V$  for a pulse width  $\leq 3ns$ , and the pulse width cannot be greater than one third of the cycle rate.  $V_{IL}$  under-shoot:  $V_{IL}$  (MIN) =  $-2V$  for a pulse width  $\leq 3ns$ .
23. The clock frequency must remain constant (stable clock is defined as a signal cycling within timing constraints specified for the clock pin) during access or precharge states (READ, WRITE, including  $t_{WR}$ , and PRECHARGE commands). CKE may be used to reduce the data rate.
24. Auto precharge mode only. The precharge timing budget ( $t_{RP}$ ) begins 7.5ns/7ns after the first clock delay, after the last WRITE is executed.
25. Precharge mode only.
26. JEDEC and PC100, PC133 specify three clocks.
27.  $t_{AC}$  for 75/10/7 at  $CL = 3$  with no load is 4.6ns and is guaranteed by design.
28. Parameter guaranteed by design.
29. For 75/10,  $CL = 3$ ,  $t_{CK} = 7.5ns$ ; For 7,  $CL = 2$ ,  $t_{CK} = 7.5ns$
30. CKE is HIGH during refresh command period  $t_{RFC}$  (MIN) else CKE is LOW. The  $I_{DDQ}$  limit is actually a nominal value and does not result in a fail value.

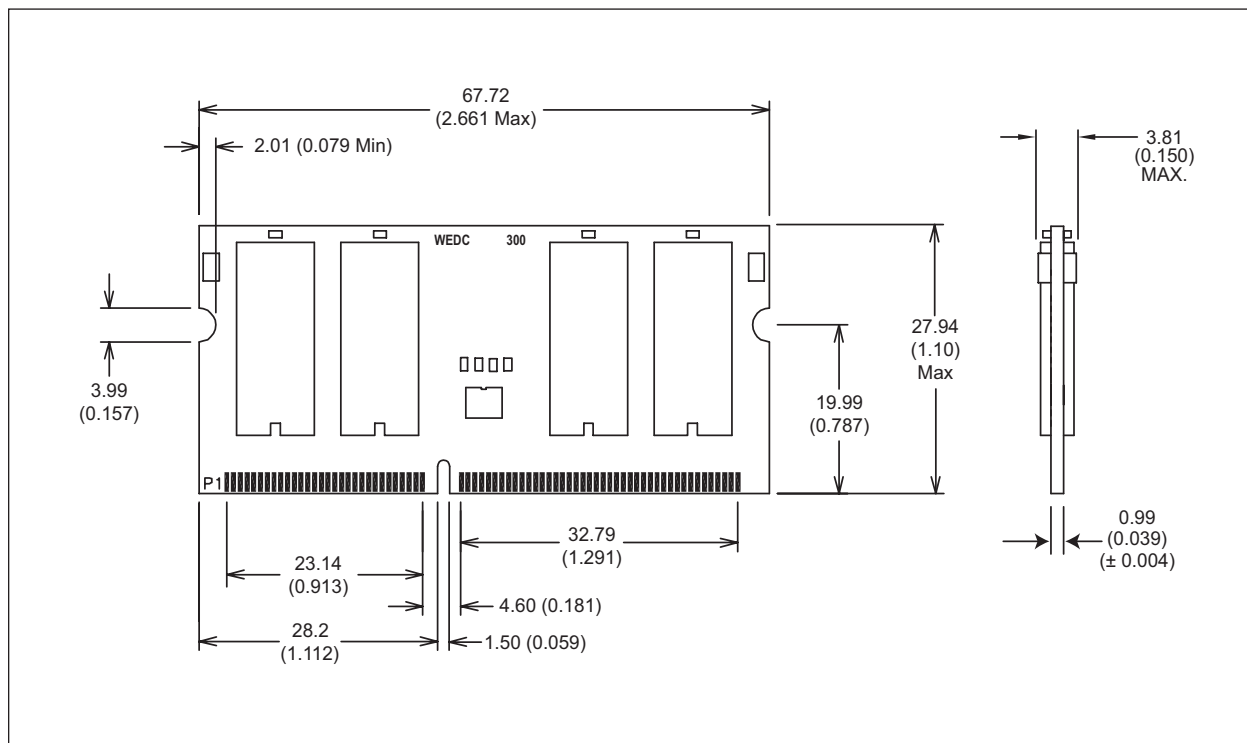


### PACKAGE DIMENSIONS FOR AD1

Ordering Information	Speed	CAS Latency	Height*
W3DG7268V10AD1	100MHz	CL=2	27.94 (1.10") MAX
W3DG7268V7AD1	133MHz	CL=2	27.94 (1.10") MAX
W3DG7268V75AD1	133MHz	CL=3	27.94 (1.10") MAX

Note: For industrial temperature range product, add an "I" to the end of the part number.

### PACKAGE DIMENSIONS FOR AD1



\* All Dimensions are in millimeters and (inches).



**Document Title**

256MB - 64Mx72 SDRAM UNBUFFERED

**Revision History**

Rev #	History	Release Date	Status
Rev 0	Created Datasheet	6-2-03	Advanced
Rev 1	1.1 Updated CAP and IDD Spec. 1.2 Added AD1 package option 1.3 Created document title page 1.4 Moved from Advanced to Preliminary	6-04	Preliminary
Rev 2	2.1 Added AC Spec 2.2 Updated CAP Spec.	10-13-04	Preliminary