



512K x 72 SYNCHRONOUS PIPELINE BURST ZBL SRAM

FEATURES

- Fast clock speed: 150, 133, and 100MHz
- Fast access times: 3.8ns, 4.2ns, and 5.0ns
- Fast OE# access times: 3.8ns, 4.2ns, and 5.0ns
- High performance 3-1-1-1 access rate
- 2.5V \pm 5% power supply
- Common data inputs and data outputs
- Byte write enable and global write control
- Six chip enables for depth expansion and address pipeline
- Internally self-timed write cycle
- Burst control pin (interleaved or linear burst sequence)
- Automatic power-down for portable applications
- Commercial, industrial and military temperature ranges
- Packaging:
 - 152 PBGA package 17 x 23mm

BENEFITS

- 30% space savings compared to equivalent TQFP solution
- Reduced part count
- 24% I/O reduction
- Laminate interposer for optimum TCE match
- Low Profile
- Reduce layer count for board routing
- Suitable for hi-reliability applications
- User configurable as 1M x 36 or 2M x 18
- Upgradable to 1M x 72 (contact factory for availability)

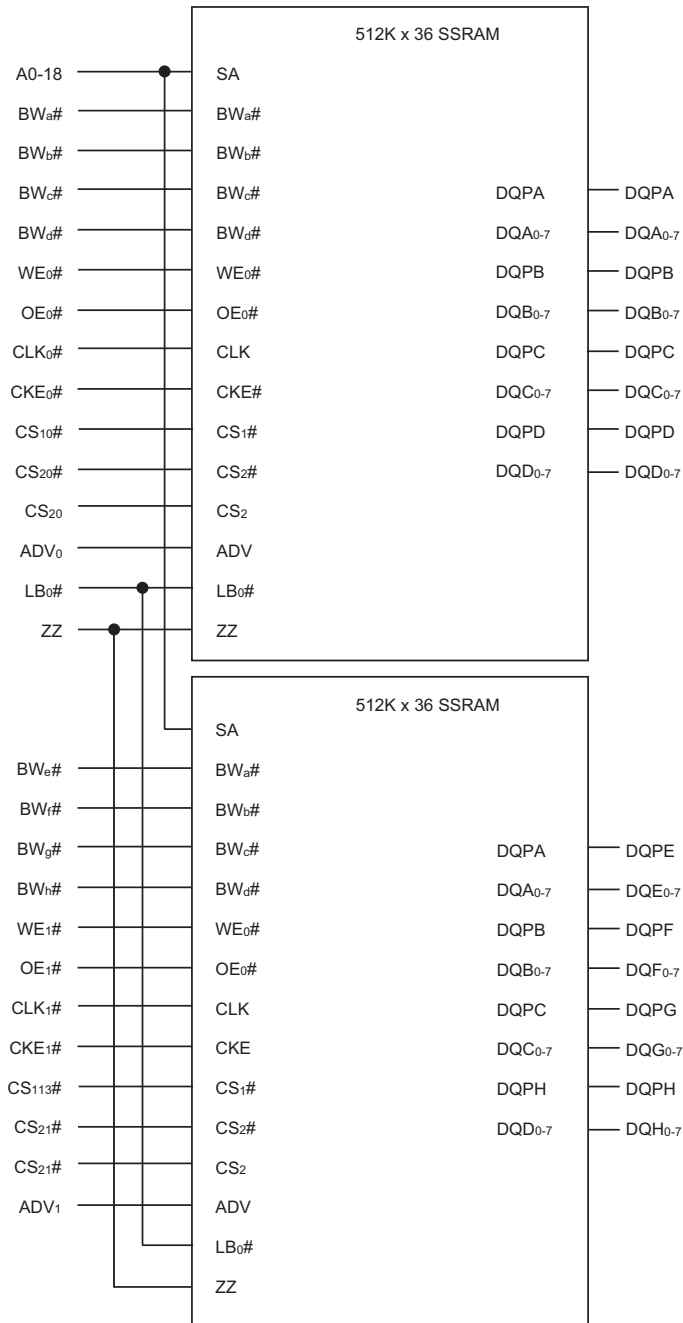
DESCRIPTION

The WEDC SyncBurst - SRAM employs high-speed, low-power CMOS design that is fabricated using an advanced CMOS process. WEDC's 32Mb SyncBurst SRAMs integrate two 512K x 36 SSRAMs into a single BGA package to provide 512K x 72 configuration. All synchronous inputs pass through registers controlled by a positive-edge-triggered single-clock input (CLK). The ZBL or Zero Bus Latency Memory utilizes all the bandwidth in any combination of operating cycles. Address, data inputs, and all control signals except output enable and linear burst order are synchronized to input clock. Burst order control must be tied "High or Low." Asynchronous inputs include the sleep mode enable (ZZ). Output Enable controls the outputs at any given time. Write cycles are internally self-timed and initiated by the rising edge of the clock input. This feature eliminates complex off-chip write pulse generation and provides increased timing flexibility for incoming signals.

* This product is under development, is not qualified or characterized and is subject to change without notice.



FUNCTIONAL BLOCK DIAGRAM





PIN CONFIGURATION

(TOP VIEW)

	1	2	3	4	5	6	7	8	9
A	-	ADV0	OE0#	DQB2	DQB4	DQB6	DNU	DQA6	DQA2
B	CKE0#	WE0#	DQB7	DQB5	DQB3	DQB0	DQA7	DQA3	DQA1
C	CLK0	CS20#	DQC2	DQPC	DQPB	DQB1	DQD7	DQA4	DQA0
D	BWA#	BWB#	DQC3	VSS	VSS	VSS	DQD6	DQA5	DQPA
E	BWC#	BWD#	DQC4	VCCQ	VCCQ	VCCQ	DQD5	DQPD	ZZ
F	CS10#	CS20	DQC5	VCCQ	VCCQ	VSS	DQD4	DNU*	A0
G	A7	DQC0	DQC7	VSS	VCC	VCC	DQD3	A1	A3
H	A18	DQC1	DQC6	VCC	VCC	VCC	DQD2	A2	A5
J	A9	A6	DQF2	VSS	VSS	VSS	DQD1	A4	A16
K	A8	DQF4	DQF3	VCC	VCC	VCC	DQD0	A14	A15
L	A17	DQF5	DQF6	VCC	VCC	VSS	DQE6	A12	A13
M	ADV1	OE1#	DQF7	VSS	VCCQ	VSSQ	DQE7	A10	A11
N	CKE1#	WE1#	DQPF	VCCQ	VCCQ	VCCQ	DQE5	DQE3	LBO#
P	CLK1	CS21#	DQF1	VSS	VSS	VSS	DQE4	DQE2	DQE0
R	BWE#	BWF#	DQF0	DQG1	DQG4	DQH1	DQH2	DQE1	DQPE
T	BWG#	BWH#	DQG0	DQG2	DQG5	DQH0	DQH4	DQH7	DQPH
U	CS11#	CS21	DQG3	DQPG	DQG6	DQG7	DQH3	DQH5	DQH6

NOTES:

DNU means Do Not Use and are reserved for future use.

* Pin F8 reserved for A19 upgrade to 1M x 72.



FUNCTION DESCRIPTION

The WEDPZ512K72S-XBX is an ZBL SSRAM designed to sustain 100% bus bandwidth by eliminating turnaround cycle when there is transition from Read to Write, or vice versa. All inputs (with the exception of OE#, LBO# and ZZ) are synchronized to rising clock edges.

All read, write and deselect cycles are initiated by the ADV input. Subsequent burst addresses can be internally generated by the burst advance pin (ADV). ADV should be driven to Low once the device has been deselected in order to load a new address for next operation.

Clock Enable (CKE#) pin allows the operation of the chip to be suspended as long as necessary. When CKE# is high, all synchronous inputs are ignored and the internal device registers will hold their previous values. NBL SSRAM latches external address and initiates a cycle when CKE and ADV are driven low at the rising edge of the clock.

Output Enable (OE#) can be used to disable the output at any given time. Read operation is initiated when at the rising edge of the clock, the address presented to the address inputs are latched in the address register, CKE# is driven low, the write enable input signals WE# are driven high, and ADV driven low. The internal array is read between the first rising edge and the second rising edge of the clock and the data is latched in the output register. At the second clock edge the data is driven out of the SRAM. During read operation OE# must be driven low for the device to drive out the requested data.

Write operation occurs when WE# is driven low at the rising edge of the clock. BW#[h:a] can be used for byte write operation. The pipe-lined ZBL SSRAM uses a late-late write cycle to utilize 100% of the bandwidth. At the first rising edge of the clock, WE# and address are registered, and the data associated with that address is required two cycles later.

Subsequent addresses are generated by ADV High for the burst access as shown below. The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the LBO# pin. When this pin is low, linear burst sequence is selected. And when this pin is high, Interleaved burst sequence is selected.

During normal operation, ZZ must be driven low. When ZZ is driven high, the SRAM will enter a Power Sleep Mode after two cycles. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM operates after two cycles of wake up time.

BURST SEQUENCE TABLE

(Interleaved Burst, LBO# = High)									
LBO# Pin	High	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
First Address		0	0	0	1	1	0	1	1
		0	1	0	0	1	1	1	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	1	0	0	1	0	0

NOTE: LBO pin must be tied to High or Low, and Floating State must not be allowed.

(Linear Burst, LBO# = Low)									
LBO# Pin	High	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
First Address		0	0	0	1	1	0	1	1
		0	1	1	0	1	1	0	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	0	0	0	1	1	0



TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

CE#x	ADV	WE#	BW#x	OE#	CKE#	CLK	Address Accessed	Operation
H	L	X	X	X	L	↑	N/A	Deselect
X	H	X	X	X	L	↑	N/A	Continue Deselect
L	L	H	X	L	L	↑	External Address	Begin Burst Read Cycle
X	H	X	X	L	L	↑	Next Address	Continue Burst Read Cycle
L	L	H	X	H	L	↑	External Address	NOP/Dummy Read
X	H	X	X	H	L	↑	Next Address	Dummy Read
L	L	L	L	X	L	↑	External Address	Begin Burst Write Cycle
X	H	X	L	X	L	↑	Next Address	Continue Burst Write Cycle
L	L	L	H	X	L	↑	N/A	NOP/Write Abort
X	H	X	H	X	L	↑	Next Address	Write Abort
X	X	X	X	X	H	↑	Current Address	Ignore Clock

NOTES:

- 1) X means "Don't Care."
- 2) The rising edge of clock is symbolized by (↑).
- 3) A continue deselect cycle can only be entered if a deselect cycle is executed first.
- 4) WRITE# = L means Write operation in WRITE TRUTH TABLE.
WRITE# = H means Read operation in WRITE TRUTH TABLE.
- 5) Operation finally depends on status of asynchronous input pins (ZZ and OE#).
- 6) CE#x refers to the combination of CS#1 and CS#2.

WRITE TRUTH TABLE

WE#	BW#a	BW#b	BW#c	BW#d	Operation
H	X	X	X	X	Read
L	L	H	H	H	Write Byte a
L	H	L	H	H	Write Byte b
L	H	H	L	H	Write Byte c
L	H	H	H	L	Write Byte d
L	L	L	L	L	Write All Bytes
L	H	H	H	H	Write Abort/NOP

NOTES:

- 1) X means "Don't Care."
- 2) All inputs in this table must meet setup and hold time around the rising edge of CLK (↑).
- 3) Replace BW#a with BW#e, BW#b, with BW#f, BW#c with BW#g and BW#d with BW#h for operation of IC2.



ABSOLUT MAXIMUM RATINGS*

V_{IN} Voltage or any other pin relative to V_{SS}	-0.3V to +3.6V
Voltage on V_{CC} supply relative to V_{SS}	-0.3V to +3.6V
Storage temperature (BGA)	-55°C to +150°C

* Stress greater than those listed under "Absolute Maximum Ratings: may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS

(-55°C T_A +125°C)

Description	Symbol	Conditions	Min	Max	Units	Notes
Input High (Logic 1) Voltage	V_{IH}		1.7	$V_{CC} + 0.3$	V	1
Input Low (Logic 0) Voltage	V_{IL}		-0.3	0.7	V	1
Input Leakage Current	I_{IL}	$V_{CC} = \text{Max}, 0V \ V_{IN} \ V_{CC}$	-4	+4	μA	2
Output Leakage Current	I_{LO}	Output(s) Disabled, $V_{OUT} = V_{SS}$ to V_{CCQ}	-2	+2	μA	
Output High Voltage	V_{OH}	$I_{OH} = -1.0mA$	2.0	---	V	1
Output Low Voltage	V_{OL}	$I_{OL} = 1.0mA$	---	0.4	V	1
Supply Voltage	V_{CC}		2.375	2.625	V	1
I/O Power Supply	V_{CCQ}		2.375	2.625	V	1

NOTES:

- 1) All voltages referenced to V_{SS} (GND)
- 2) ZZ pin has an internal pull-up and input leakage = $\pm 20 \mu A$.

DC CHARACTERISTICS

(-55°C T_A +125°C)

Description	Symbol	Conditions	150MHz (Max)	133MHz (Max)	100MHz (Max)	Units	Notes
Power Supply Current: Operating	I_{DD}	Device Selected; All Inputs $\leq V_{IL}$ or $\geq V_{IH}$; Cycle Time $\geq T_{CYC}$ MIN; $V_{CC} = \text{MAX}$; Output Open	700	650	600	mA	1
Power Supply Current: Standby	I_{SB2}	Device Deselected; $V_{CC} = \text{MAX}$; All Inputs $\leq V_{IL}$ or $\geq V_{IH}$ All Inputs Static; CLK Frequency = MAX Output Open, ZZ $\geq V_{CC} - 0.2V$	120	120	120	mA	
Clock Running Standby Current	I_{SB}	Device Deselected; $V_{CC} = \text{MAX}$; All Inputs $\leq V_{SS} + 0.2$ or $V_{CC} - 0.2$; $f = \text{MAX}$; ZZ $\leq V_{IL}$	180	180	160	mA	

NOTE:

I_{DD} is specified with no output current and increases with faster cycle times. I_{DD} increases with faster cycle times and greater output loading.

BGA CAPACITANCE

($T_A = +25^\circ C$, $f = 1MHz$)

Description	Symbol	Max	Units	Notes
Control Input Capacitance (LBO#, ZZ)	C_{IC}	16	pF	1
Control Input Capacitance	C_I	8	pF	1
Input/Output Capacitance (DQ)	C_O	10	pF	1
Address Capacitance	C_A	16	pF	1
Clock Capacitance	C_{CK}	6	pF	1

NOTE:

- 1) This parameter is not tested but guaranteed by design.

THERMAL RESISTANCE

Parameter	Symbol	Max	Unit
Thermal Resistance: Die Junction to Ambient	θ_{JA}	28.7	$^\circ C/W$
Thermal Resistance: Die Junction to Ball	θ_{JB}	16.0	$^\circ C/W$
Thermal Resistance: Die Junction to Case	θ_{JC}	7.1	$^\circ C/W$

Note: Refer to Application Note "PBGA Thermal Resistance Correlation" for further information regarding WEDC's thermal modeling.



AC CHARACTERISTICS

(-55°C Ta +125°C)

Parameter	Symbol	150MHz		133MHz		100MHz		Units
		Min	Max	Min	Max	Min	Max	
Clock Time	t _{CYC}	6.7		7.5		10.0		ns
Clock Access Time	t _{CD}	--	3.8	--	4.2	--	5.0	ns
Output enable to Data Valid	t _{OE}	--	3.8	--	4.2	--	5.0	ns
Clock High to Output Low-Z	t _{LZC}	1.5	--	1.5	--	1.5	--	ns
Output Hold from Clock High	t _{OH}	1.5	--	1.5	--	1.5	--	ns
Output Enable Low to output Low-Z	t _{LZOE}	0.0	--	0.0	--	0.0	--	ns
Output Enable High to Output High-Z	t _{HZOE}	--	3.0	--	3.5	--	3.5	ns
Clock High to Output High-Z	t _{HZC}	--	3.0	--	3.5	--	3.5	ns
Clock High Pulse Width	t _{CH}	2.5	--	2.5	--	3.0	--	ns
Clock Low Pulse Width	t _{CL}	2.5	--	2.5	--	3.0	--	ns
Address Setup to Clock High	t _{AS}	1.5	--	1.5	--	1.5	--	ns
CKE Setup to Clock High	t _{CES}	1.5	--	1.5	--	1.5	--	ns
Data Setup to Clock High	t _{DS}	1.5	--	1.5	--	1.5	--	ns
Write Setup to Clock High	t _{WS}	1.5	--	1.5	--	1.5	--	ns
Address Advance to Clock High	t _{ADVS}	1.5		1.5		1.5		ns
Chip Select Setup to Clock High	t _{CSS}	1.5		1.5		1.5		ns
Address Hold to Clock high	t _{AH}	0.5	--	0.5	--	0.5	--	ns
CKE Hold to Clock High	t _{CEH}	0.5	--	0.5	--	0.5	--	ns
Data Hold to Clock High	t _{DH}	0.5	--	0.5	--	0.5	--	ns
Write Hold to Clock High	t _{WH}	0.5	--	0.5	--	0.5	--	ns
Address Advance to Clock High	t _{ADVH}	0.5	--	0.5	--	0.5	--	ns
Chip Select Hold to Clock High	t _{CSH}	0.5	--	0.5	--	0.5	--	ns

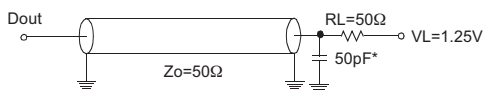
NOTES:

- 1) All Address inputs must meet the specified setup and hold times for all rising clock (CLK) edges when ADV is sampled low and CS#x is sampled valid. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.
- 2) Chip enable must be valid at each rising edge of CLK (when ADV is Low) to remain enabled.
- 3) A write cycle is defined by WE# low having been registered into the device at ADV Low. A Read cycle is defined by WE# High with ADV Low. Both cases must meet setup and hold times.

AC TEST CONDITIONS

Parameter	Value
Input Pulse Level	0 to 2.5V
Input Rise and Fall Time	1.0V/ns
Input and Output Timing Reference Levels	1.25V
Output Load	See Output Load (A & B)

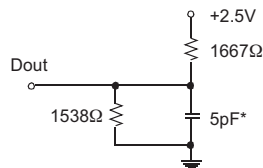
OUTPUT LOAD (A)



*Including Scope and Jig Capacitance

OUTPUT LOAD (B)

(for TLZC, TLZOE, THZOE, and THZC)





SNOOZE MODE

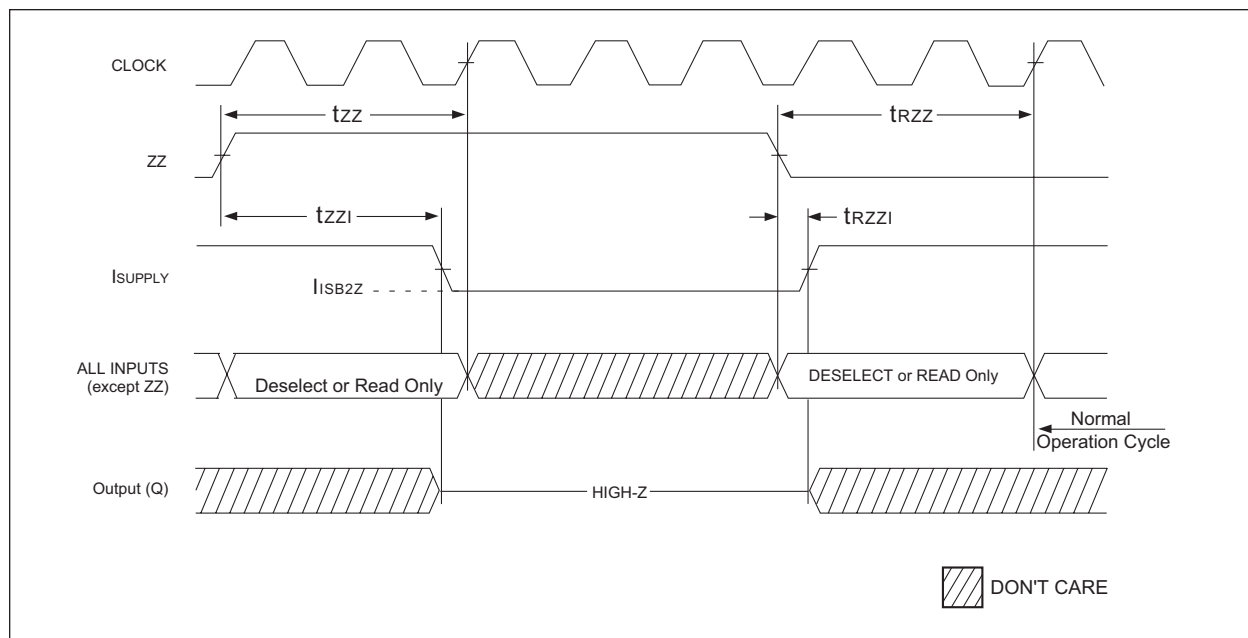
SNOOZE MODE is a low-current, “power-down” mode in which the device is deselected and current is reduced to ISB_{2Z} . The duration of SNOOZE MODE is dictated by the length of time Z is in a HIGH state. After the device enters SNOOZE MODE, all inputs except ZZ become gated inputs and are ignored. ZZ is an asynchronous, active HIGH input that causes the device to enter SNOOZE MODE.

When ZZ becomes a logic HIGH, ISB_{2Z} is guaranteed after the setup time t_{ZZ} is met. Any READ or WRITE operation pending when the device enters SNOOZE MODE is not guaranteed to complete successfully. Therefore, SNOOZE MODE must not be initiated until valid pending operations are completed.

SNOOZE MODE

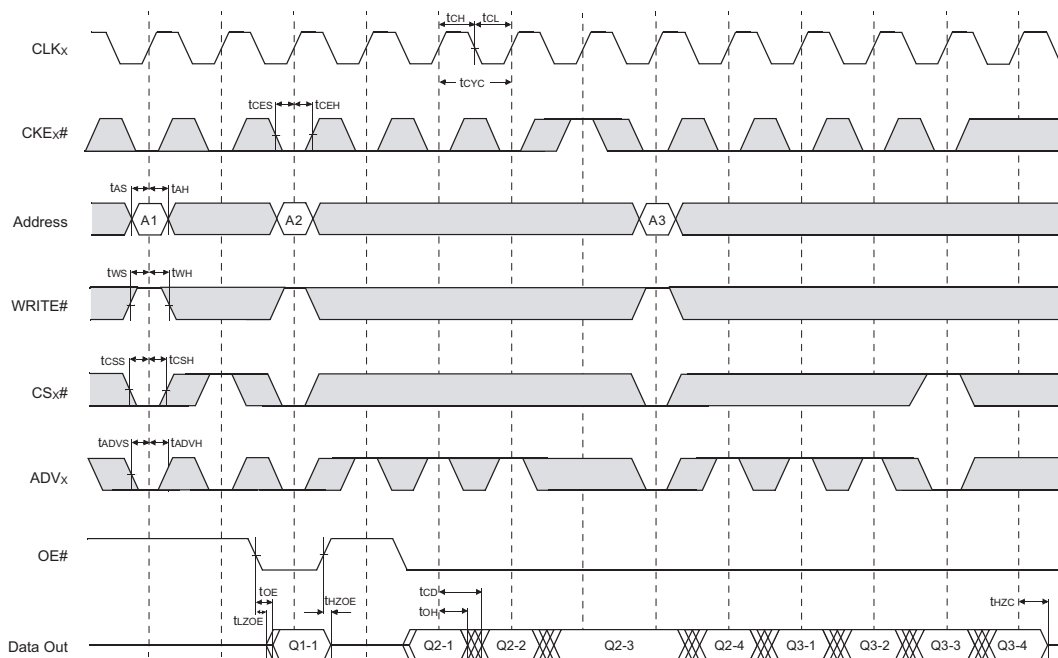
Description	Conditions	Symbol	Min	Max	Units
Current during SNOOZE MODE	$ZZ \geq V_{IH}$	ISB_{2Z}		20	mA
ZZ active to input ignored		t_{ZZ}		2	cycle
ZZ inactive to input sampled		t_{RZZ}	2		cycle
ZZ active to snooze current		t_{ZZI}		2	cycle
ZZ inactive to exit snooze current		t_{RZZI}	0		ns

SNOOZE MODE TIMING DIAGRAM





TIMING WAVEFORM OF READ CYCLE

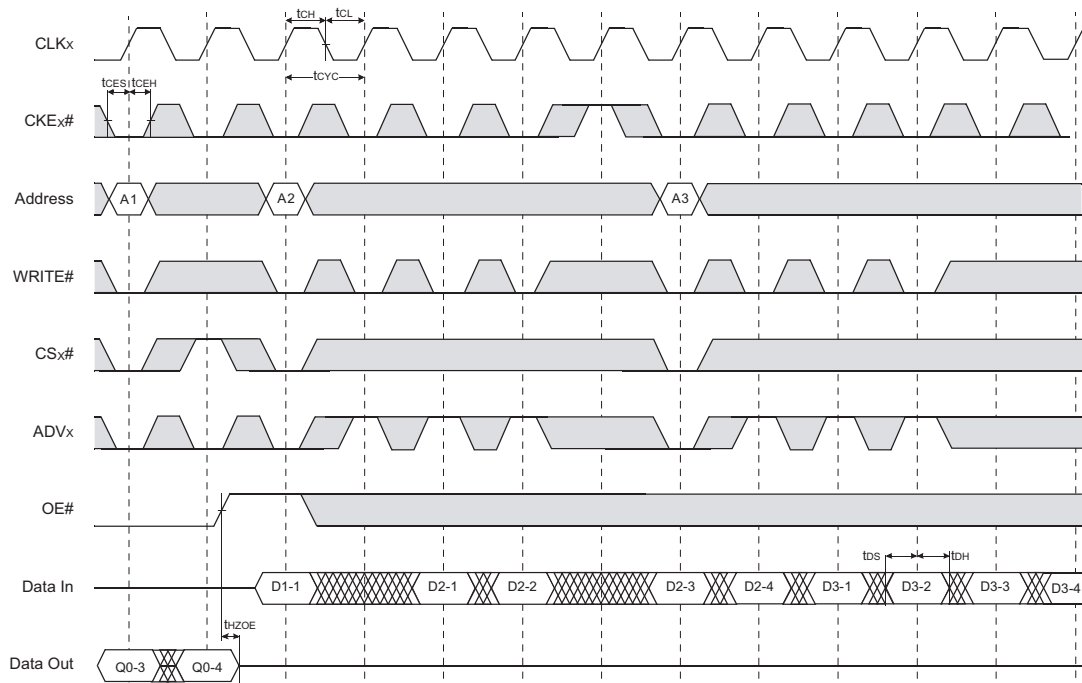


NOTES: WRITE# = L means WEx# = L, and BWx# = L
CSx# refers to the combination of CS10#, CS20 and CS20#, or CS11#, CS21 and CS21#.

□ Don't Care
⊗ Undefined



TIMING WAVEFORM OF WRITE CYCLE

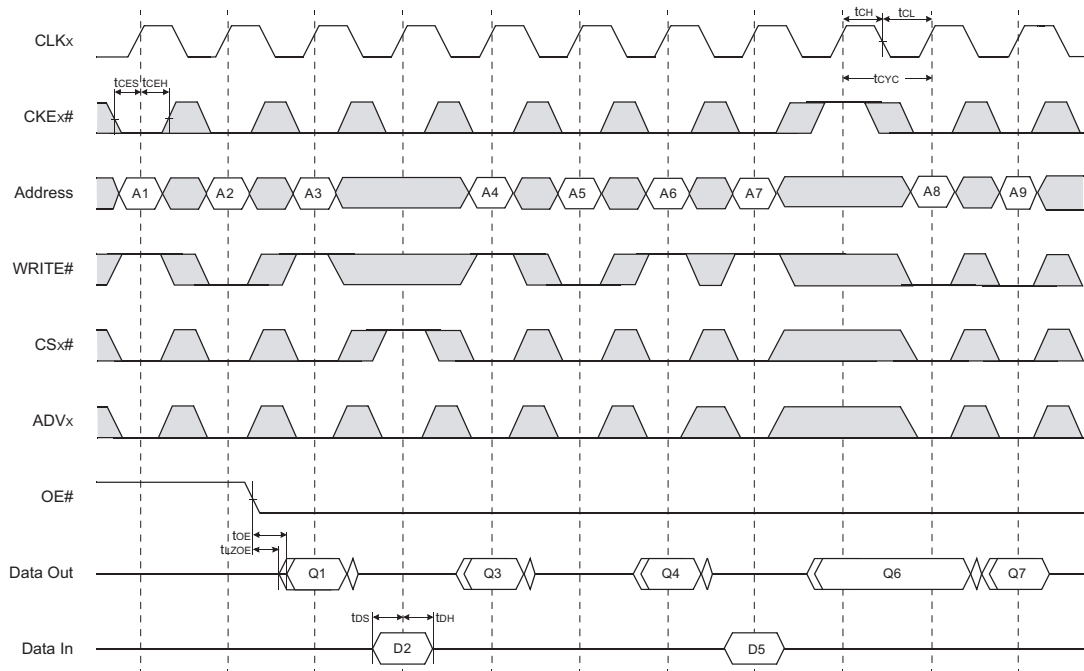


NOTES: WRITE# = L means WEx# = L, and BWx# = L.
CSx# refers to the combination of CS₀#, CS₂₀ and CS₂₀#, or CS₁#, CS₂₁ and CS₂₁#.

□ Don't Care
⊠ Undefined



TIMING WAVEFORM OF SINGLE READ/WRITE

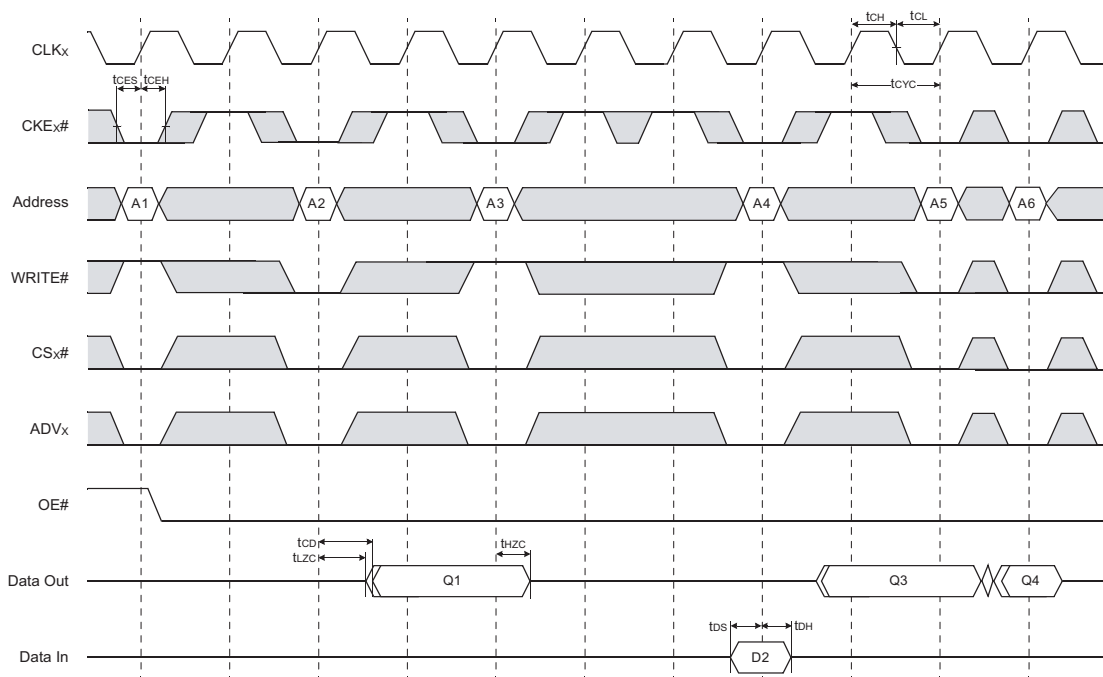


NOTES: WRITE# = L means WEx# = L, and BWx# = L.
CSx# refers to the combination of CS1₀#, CS2₀ and CS2₀#, or CS1₁#, CS2₁ and CS2₁#.

□ Don't Care
⊗ Undefined



TIMING WAVEFORM OF CKE OPERATION



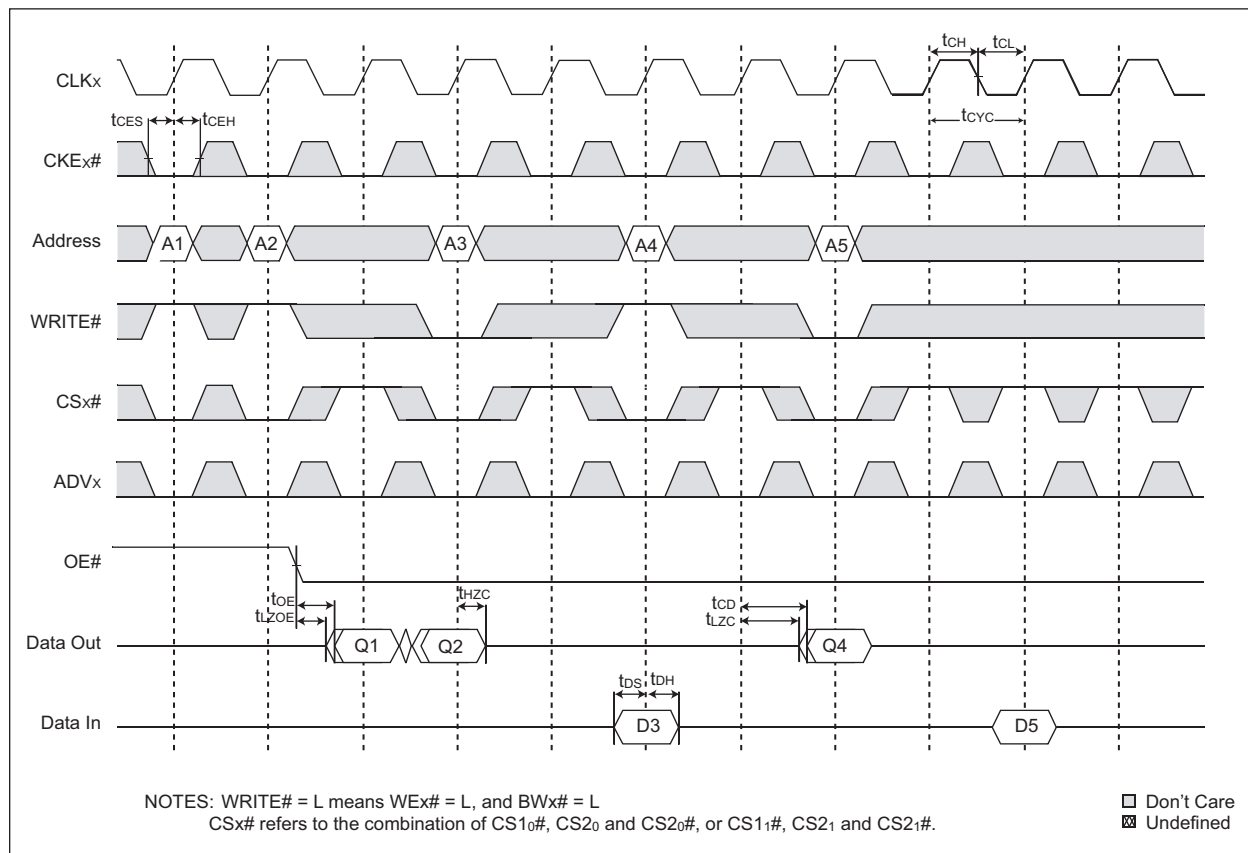
NOTES: WRITE# = L means WEx# = L, and BWx# = L

CSx# refers to the combination of CS10#, CS20 and CS20#, or CS11#, CS21 and CS21#.

□ Don't Care
 X Undefined



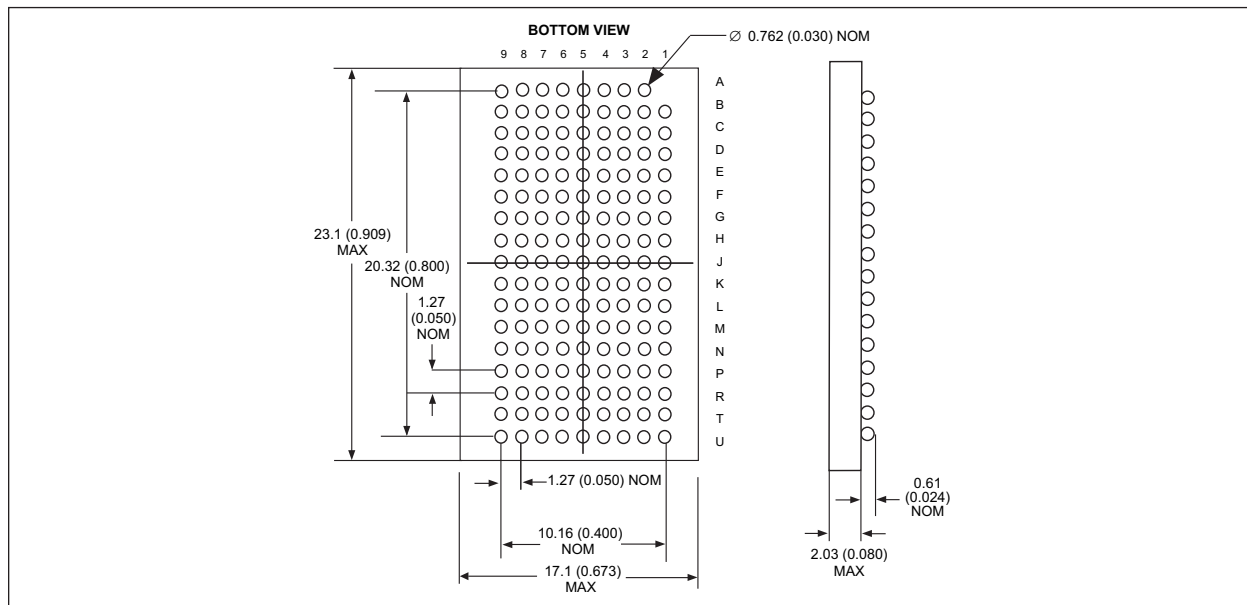
TIMING WAVEFORM OF CE OPERATION





PACKAGE DIMENSION:

152 BUMP PBGA



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

WED P Z 512K 72 S - XXX B X

DEVICE GRADE:

- M** = Military -55°C to +125°C
- I** = Industrial -40°C to +85°C
- C** = Commercial 0°C to +70°C

PACKAGE:

- B** = 152 Plastic Ball Grid Array (PBGA)

FREQUENCY (MHz)

- 100** = 100MHz
- 133** = 133MHz
- 150** = 150MHz

2.5V Voltage

CONFIGURATION, 512K x 72

SSRAM ZBL

PLASTIC

WHITE ELECTRONIC DESIGNS CORP.



Document Title

512K x 72 Synchronous SRAM – NBL

Revision History

Rev #	History	Release Date	Status
Rev 0	Initial Release	February 2001	Advanced
Rev 1	Changes (Pg. 1, 5, 6, 13) 1.1 Block Diagram: Change DQ _D to DQ _{PD} , Font Consistency 1.2 Electrical Characteristics Note 2: Change reference to mA instead of MA. 1.3 DC Characteristics: Adjust location of Units & Notes for I _{SB2} . 1.4 AC Characteristics: Change temperature range to (-55°C ≤ T _A ≤ +125°C) 1.5 Package Dimension: Adjust length line to end of package 1.6 Block Diagram: Adjust look for consistency 1.7 DC Characteristics: ISB2 condition should read All Inputs ≤ V _{IL} or ≥ V _{IH} instead of > V _{IH} 1.8 Figure 2: Inputs transition should not be shown fully connected. 1.9 Figure 6: Unknown text deleted from timing diagram 1.10 Package Dimension: Ball diameter arrow corrected to point to ball.	April 2001	Advanced
Rev 2	Change (Pg. 1) 1.1 Change status from Advanced to Preliminary	November 2001	Preliminary
Rev 3	Changes (Pg. 1, 2) 1.1 Block Diagram: Address lines should be A0-18 1.2 Pin Configuration: Add Note *Pin F8 reserved for A19 upgrade to 1Mx72.	November 2001	Preliminary
Rev 4	Changes (Pg. 1, 5) 1.1 BGA Capacitance: Remove references to temperature in individual conditions 1.2 Change CI from 10pF to 8pF 1.3 Change CA from 20pF to 16pF 1.4 Change CCK from 7pF to 6pF 1.5 Add Control Input Capacitance (CIC) 16pF	November 2002	Preliminary
Rev 5	Changes (Pg. 5) 1.1 Add Thermal Resistance table 1.2 Update current values 1.3 Update package mechanical drawing	May 2003	Preliminary
Rev 6	Changes (Pg. 1, 13, 14, 15) 1.1 Change mechanical drawing to new style	November 2003	Preliminary