



512Kx8 MONOLITHIC FLASH, SMD 5962-96692

FEATURES

- Access Times of 60, 70, 90, 120, 150ns
- Packaging
 - 32 pin, Hermetic Ceramic, 0.600" DIP (Package 300)
 - 32 lead, Hermetic Ceramic, 0.400" SOJ (Package 101)
 - 32 pin, Rectangular Ceramic Leadless Chip Carrier (Package 601)
 - 32 lead Flatpack (Package 220)
- 1,000,000 Erase/Program Cycles Minimum
- Sector Erase Architecture
 - 8 equal size sectors of 64K bytes each
 - Any combination of sectors can be concurrently erased. Also supports full chip erase

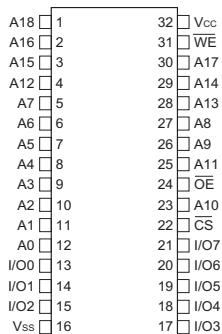
- Organized as 512Kx8
- Commercial, Industrial and Military Temperature Ranges
- 5 Volt Programming. 5V \pm 10% Supply.
- Low Power CMOS
- Embedded Erase and Program Algorithms
- TTL Compatible Inputs and CMOS Outputs
- Page Program Operation and Internal Program Control Time.

Note: For programming information refer to Flash Programming 4M5 Application Note.

PIN CONFIGURATION FOR WMF512K8-XXX5

32 DIP
32 CSOJ
32 Flatpack

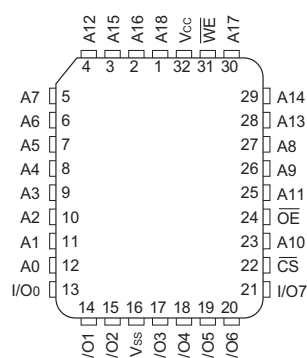
TOP VIEW



PIN CONFIGURATION FOR WMF512K8-XCLX5

32 CLCC

TOP VIEW



PIN DESCRIPTION

A0-18	Address Inputs
I/O0-7	Data Input/Output
CS	Chip Select
OE	Output Enable
WE	Write Enable
Vcc	+5.0V Power
Vss	Ground



ABSOLUTE MAXIMUM RATINGS (1)

Parameter		Unit
Operating Temperature	-55 to +125	°C
Supply Voltage (V _{CC}) (1)	-2.0 to +7.0	V
Signal Voltage Range(any pin except A ₉) (2)	-2.0 to +7.0	V
Storage Temperature Range	-65 to +150	°C
Lead Temperature (soldering, 10 seconds)	+300	°C
Data Retention Mil Temp	20	years
Endurance - erase/program cycles (Mil Temp)	100,000 min	cycles
A ₉ Voltage for sector protect (V _{ID}) (3)	-2.0 to +14.0	V

NOTES:

1. Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2. Minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, inputs may overshoot V_{SS} to -2.0 V for periods of up to 20ns. Maximum DC voltage on output and I/O pins is V_{CC} + 0.5V. During voltage transitions, outputs may overshoot to V_{CC} + 2.0 V for periods of up to 20ns.
3. Minimum DC input voltage on A₉ pin is -0.5V. During voltage transitions, A₉ may overshoot V_{SS} to -2V for periods of up to 20ns.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{CC}	4.5	5.5	V
Input High Voltage	V _{IH}	2.0	V _{CC} + 0.5	V
Input Low Voltage	V _{IL}	-0.5	+0.8	V
Operating Temp. (Mil.)	T _A	-55	+125	°C
Operating Temp. (Ind.)	T _A	-40	+85	°C
A ₉ Voltage for Sector Protect	V _{ID}	11.5	12.5	V

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Conditions	Max	Unit
Address Input capacitance	C _{AD}	V _{IO} = 0 V, f = 1.0 MHz	15	pF
Output Enable capacitance	C _{OE}	V _{IN} = 0 V, f = 1.0 MHz	15	pF
Write Enable capacitance	C _{WE}	V _{IN} = 0 V, f = 1.0 MHz	15	pF
Chip Select capacitance	C _{CS}	V _{IN} = 0 V, f = 1.0 MHz	15	pF
Data I/O capacitance	C _{I/O}	V _{IO} = 0 V, f = 1.0 MHz	15	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS - CMOS COMPATIBLE (V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C TO +125°C)

Parameter	Symbol	Conditions	Min		Unit
				Max	
Input Leakage Current	I _{LI}	V _{CC} = 5.5, V _{IN} = GND to V _{CC}		10	μA
Output Leakage Current	I _{LOx32}	V _{CC} = 5.5, V _{IN} = GND to V _{CC}		10	μA
V _{CC} Active Current for Read (1)	I _{CC1}	$\overline{CS} = V_{IL}, \overline{OE} = V_{IH}, f = 5\text{MHz}$		50	mA
V _{CC} Active Current for Program or Erase (2)	I _{CC2}	$\overline{CS} = V_{IL}, \overline{OE} = V_{IH}$		60	mA
V _{CC} Standby Current	I _{CC4}	V _{CC} = 5.5, $\overline{CS} = V_{IH}, f = 5\text{MHz}$		1.6	mA
Output Low Voltage	V _{OL}	I _{OL} = 8.0 mA, V _{CC} = 4.5		0.45	V
Output High Voltage	V _{OH1}	I _{OH} = -2.5 mA, V _{CC} = 4.5	0.85 x V _{CC}		V
Low V _{CC} Lock-Out Voltage	V _{LKO}		3.2	4.2	V

NOTES:

1. The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 5 MHz). The frequency component typically is less than 2 mA/MHz, with \overline{OE} at V_{IH}.
2. I_{CC} active while Embedded Algorithm (program or erase) is in progress.
3. DC test conditions: V_{IL} = 0.3V, V_{IH} = V_{CC} - 0.3V



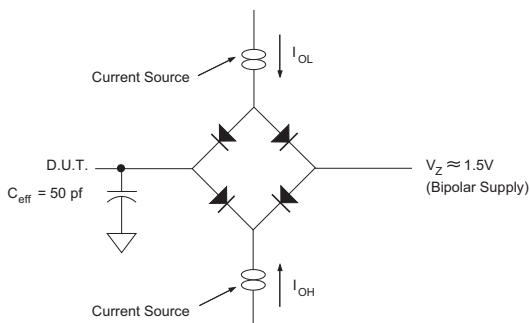
AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, \overline{CS} CONTROLLED ($V_{CC} = 5.0V$, $V_{SS} = 0V$, $T_A = -55^\circ C$ TO $+125^\circ C$)

Parameter	Symbol		-60		-70		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{AVAV}	t _{WC}	60		70		90		120		150		ns
Write Enable Setup Time	t _{WLEL}	t _{WS}	0		0		0		0		0		ns
Chip Select Pulse Width	t _{ELEH}	t _{CP}	40		45		45		50		50		ns
Address Setup Time	t _{AVEL}	t _{AS}	0		0		0		0		0		ns
Data Setup Time	t _{DVEH}	t _{DS}	40		45		45		50		50		ns
Data Hold Time	t _{EHDX}	t _{DH}	0		0		0		0		0		ns
Address Hold Time	t _{ELAX}	t _{AH}	40		45		45		50		50		ns
Chip Select Pulse Width High	t _{EH}	t _{CPH}	20		20		20		20		20		ns
Duration of Byte Programming Operation (1)	t _{WHWH1}			300		300		300		300		300	μs
Sector Erase Time (2)	t _{WHWH2}			15		15		15		15		15	sec
Read Recovery Time	t _{GHEL}		0		0		0		0		0		ns
Chip Programming Time				11		11		11		11		11	sec
Chip Erase Time (3)				64		64		64		64		64	sec

NOTES:

1. Typical value for t_{WHWH1} is 7μs.
2. Typical value for t_{WHWH2} is 1sec.
3. Typical value for Chip Erase time is 8sec.

AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V _{IL} = 0, V _{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

Notes:

V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z₀ = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.



AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, WE CONTROLLED
(V_{CC} = 5.0V, T_A = -55°C TO +125°C)

Parameter	Symbol		<u>-60</u>		<u>-70</u>		<u>-90</u>		<u>-120</u>		<u>-150</u>		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{AVAV}	t _{WC}	60		70		90		120		150		ns
Chip Select Setup Time	t _{ELWL}	t _{CS}	0		0		0		0		0		ns
Write Enable Pulse Width	t _{WLWH}	t _{WP}	40		45		45		50		50		ns
Address Setup Time	t _{AVWH}	t _{AS}	0		0		0		0		0		ns
Data Setup Time	t _{DVWH}	t _{DS}	40		45		45		50		50		ns
Data Hold Time	t _{WHDX}	t _{DH}	0		0		0		0		0		ns
Address Hold Time	t _{WHAX}	t _{AH}	40		45		45		50		50		ns
Write Enable Pulse Width High	t _{WHWL}	t _{WPH}	20		20		20		20		20		ns
Duration of Byte Programming Operation (1)	t _{WHWH1}			300		300		300		300		300	μs
Sector Erase Time (2)	t _{WHWH2}			15		15		15		15		15	sec
Read Recovery Time before Write	t _{GHWL}		0		0		0		0		0		ms
V _{CC} Set-up Time		t _{VCS}	50		50		50		50		50		μs
Chip Programming Time				11		11		11		11		11	sec
Output Enable Setup Time		t _{OES}	0		0		0		0		0		ns
Output Enable Hold Time (4)		t _{OEH}	10		10		10		10		10		ns
Chip Erase Time (3)				64		64		64		64		64	sec

NOTES:

1. Typical value for t_{WHWH1} is 7μs.
2. Typical value for t_{WHWH2} is 1sec.
3. Typical value for Chip Erase time is 8sec.
4. For Toggle and Data Polling.

AC CHARACTERISTICS – READ ONLY OPERATIONS
(V_{CC} = 5.0V, T_A = -55°C TO +125°C)

Parameter	Symbol		<u>-60</u>		<u>-70</u>		<u>-90</u>		<u>-120</u>		<u>-150</u>		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{AVAV}	t _{RC}	60		70		90		120		150		ns
Address Access Time	t _{AVQV}	t _{ACC}		60		70		90		120		150	ns
Chip Select Access Time	t _{ELQV}	t _{CE}		60		70		90		120		150	ns
Output Enable to Output Valid	t _{GLQV}	t _{OE}		35		35		35		50		55	ns
Chip Select to Output High Z (1)	t _{EHQZ}	t _{DF}		20		20		20		30		35	ns
Output Enable High to Output High Z (1)	t _{GHQZ}	t _{DF}		20		20		20		30		35	ns
Output Hold from Address, CS or OE Change, whichever is First	t _{AXQX}	t _{OH}	0		0		0		0		0		ns

NOTES:

1. Guaranteed by design, but not tested



The diagram illustrates the timing relationships for a memory device. The signals shown are:

- Addresses:** A bus signal that becomes stable at the start of an access and returns to high impedance at the end.
- \overline{CS} (Chip Select):** An active-low signal that is asserted (goes low) at the start of an access and deasserted (goes high) at the end.
- \overline{OE} (Output Enable):** An active-low signal that is asserted (goes low) at the start of an access and deasserted (goes high) at the end.
- \overline{WE} (Write Enable):** An active-low signal that is asserted (goes low) during write operations and deasserted (goes high) during read operations.
- Outputs:** Data bus signals that transition from High Z to Output Valid at the start of an access and return to High Z at the end.

Key timing parameters are indicated:

- t_{RC} (Read Cycle Time):** The total time from the start of the access (when \overline{CS} is asserted) to the end of the access (when \overline{CS} is deasserted).
- t_{ACC} (Access Time):** The time from the start of the access (when \overline{CS} is asserted) to the point where the output is valid.
- t_{OE} (Output Enable Delay):** The time from the deassertion of \overline{OE} to the point where the output returns to High Z.
- t_{CE} (Chip Enable Delay):** The time from the deassertion of \overline{CS} to the point where the output returns to High Z.
- t_{OH} (Output Hold Time):** The time from the point where the output returns to High Z to the end of the access (when \overline{CS} is deasserted).
- t_{DF} (Data Hold Time):** The time from the point where the output returns to High Z to the end of the access (when \overline{CS} is deasserted).

The timing diagram illustrates the sequence of operations for the 555H/PA device. The signals shown are Addresses, CS, OE, WE, Data, and a 5.0 V supply. The diagram includes a 'Data Polling' section indicated by a hatched area. Key timing parameters are labeled as follows:

- Addresses:** Shows the sequence of addresses: 5555H, PA, Data Polling (hatched), PA, and a final address. Timing parameters include t_{wc} (wait cycle), t_{AS} (address setup), t_{AH} (address hold), and t_{rc} (refresh cycle).
- CS (Chip Select):** Shows the timing for t_{GHWL} (high-to-low delay) and t_{WP} (write pulse width).
- OE (Output Enable):** Shows the timing for t_{GHWL} (high-to-low delay) and t_{WHWH1} (write high-to-high delay).
- WE (Write Enable):** Shows the timing for t_{WP} (write pulse width), t_{cs} (chip select setup), t_{ds} (data setup), t_{dh} (data hold), and t_{ce} (chip enable).
- Data:** Shows the data bus activity, including the address **A0H** and the data **PD**. Timing parameters include t_{ds} (data setup), t_{dh} (data hold), t_{OE} (output enable delay), t_{CE} (chip enable delay), t_{DF} (data fall time), and t_{OH} (output hold time).
- 5.0 V:** The supply voltage reference.

1. PA is the address of the memory location to be programmed.
2. PD is the data to be programmed at byte address.
3. I/O_7 is the output of the complement of the data written to the device.
4. I/O_{out} is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.



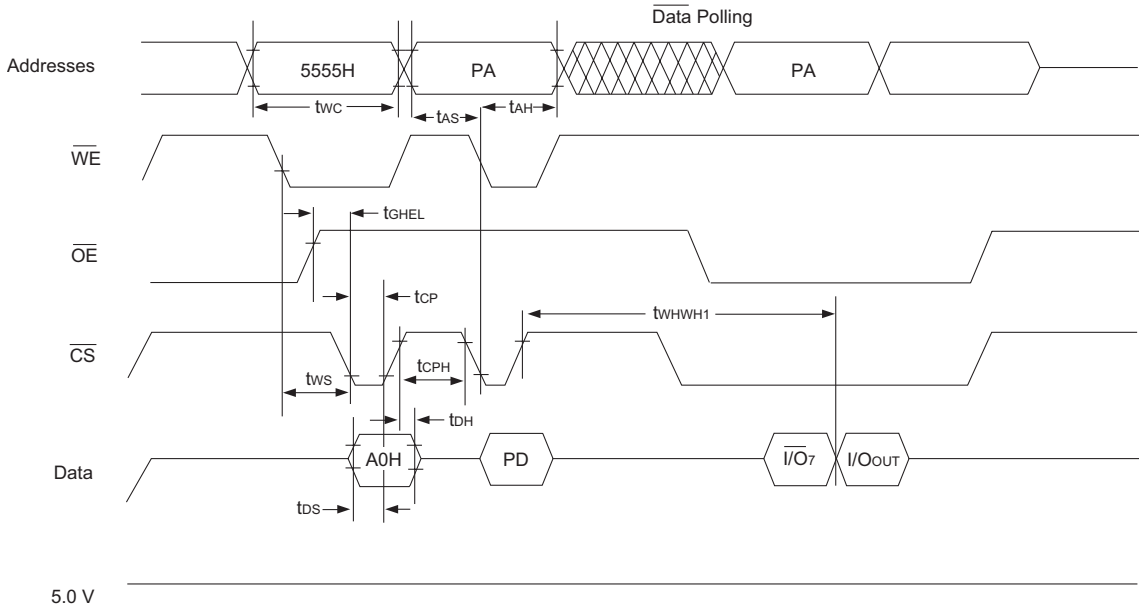
The timing diagram illustrates the electrical characteristics of the 28C01B EPROM. It shows the relationship between the Address bus, Chip Select (\overline{CS}), Output Enable (\overline{OE}), Write Enable (\overline{WE}), Data bus, and Power Supply (V_{CC}). The Address bus contains the sequence 5555H, 2AAAH, 5555H, 5555H, 2AAAH, and SA. The Data bus shows the sequence AAH, 55H, 80H, AAH, 55H, and 10H/30H. Key timing parameters are indicated: t_{AS} (Address Setup), t_{AH} (Address Hold), t_{GHWL} (\overline{CS} to \overline{OE} delay), t_{wP} (\overline{WE} pulse width), t_{wPH} (\overline{WE} pulse high time), t_{cs} (\overline{CS} setup), t_{ds} (\overline{CS} delay), and t_{vcs} (V_{CC} setup).

1. SA is the Sector Address for Sector Erase.

The timing diagram for the 74VHC04-07 illustrates the relationship between control signals and data signals. The control signals are \overline{CS} , \overline{OE} , and \overline{WE} . The data signals are I/O_7 and I/O_{0-6} . The diagram shows the setup and hold times for \overline{CS} (t_{CH}), the delay from \overline{OE} to the output (t_{OE}), the hold time for \overline{OE} (t_{OEh}), the delay from \overline{WE} to the output (t_{CE}), the delay from the output to \overline{OH} (t_{OH}), the delay from the output to \overline{OF} (t_{OF}), and the delay from the output to \overline{WHWH} (t_{WHWH}). The data signals are shown as I/O_7 and I/O_{0-6} , with states like $I/O_7 = \text{Valid Data}$, $I/O_{0-6} = \text{Invalid}$, and High Z .



ALTERNATE $\overline{\text{CS}}$ CONTROLLED PROGRAMMING OPERATION TIMINGS

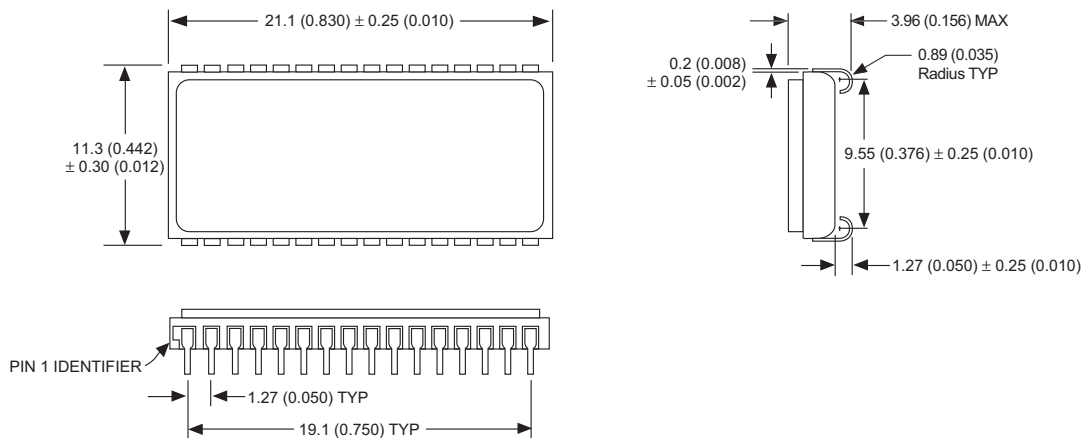


Notes:

1. PA represents the address of the memory location to be programmed.
2. PD represents the data to be programmed at byte address.
3. I/O7 is the output of the complement of the data written to the device.
4. I/OOUT is the output of the data written to the device.
5. Figure indicates the last two bus cycles of a four bus cycle sequence.

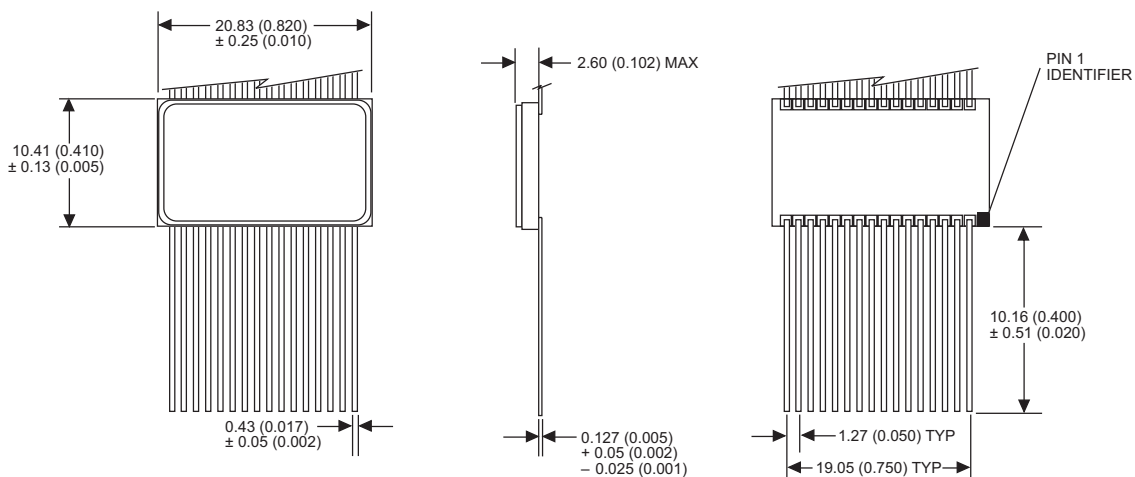


PACKAGE 101: 32 LEAD, CERAMIC SOJ



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

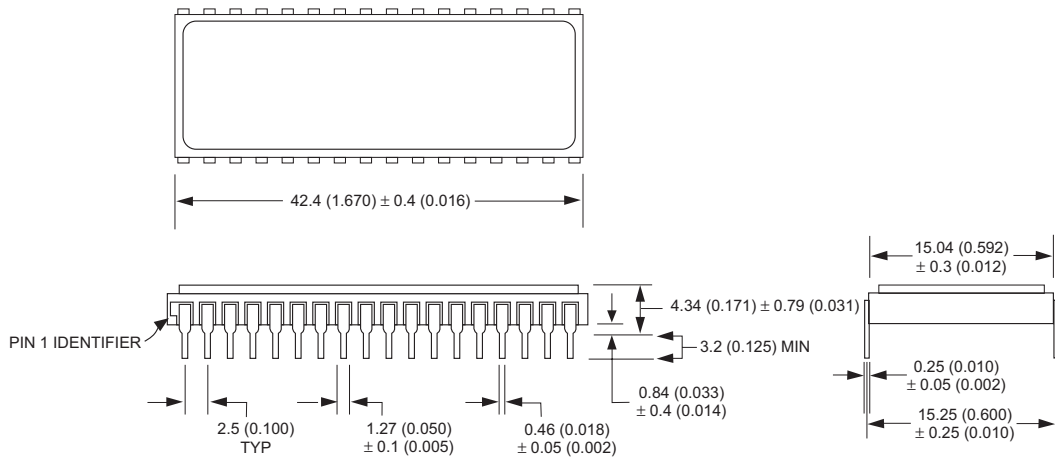
PACKAGE 220: 32 LEAD, CERAMIC FLATPACK



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



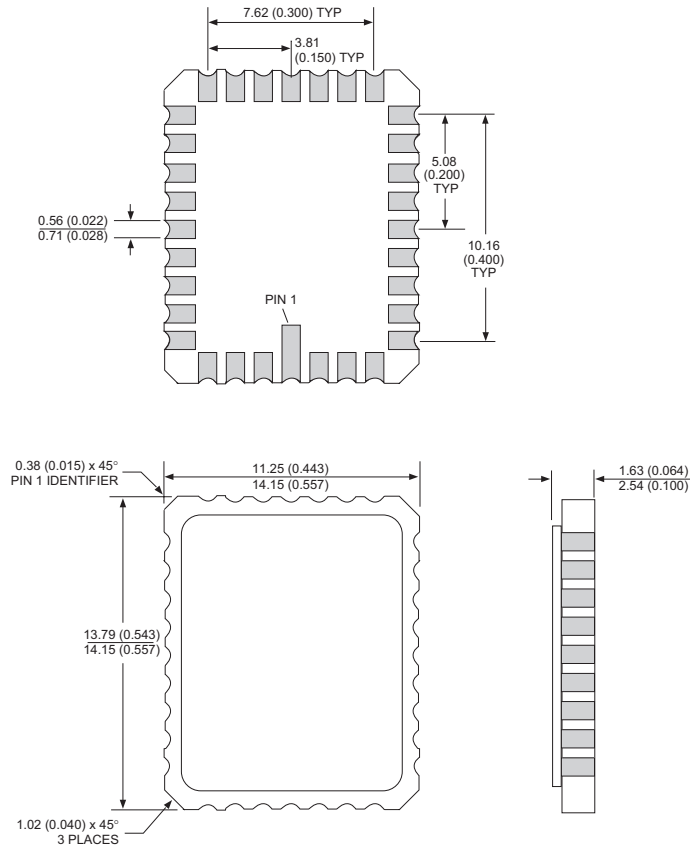
PACKAGE 300: 32 PIN, CERAMIC DIP, SINGLE CAVITY SIDE BRAZED



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



PACKAGE 601: 32 PIN, RECTANGULAR CERAMIC LEADLESS CHIP CARRIER



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



ORDERING INFORMATION

W M F 512K 8 - XXX X X 5 X

WHITE ELECTRONIC DESIGNS CORP. _____

MONOLITHIC _____

Flash _____

ORGANIZATION, 512K x 8 _____

ACCESS TIME (ns) _____

PACKAGE TYPE: _____

C = 32 Pin Ceramic DIP (Package 300)
CL = 32 Pin Rectangular Ceramic Leadless Chip Carrier (Package 601)
DE = 32 Lead Ceramic SOJ (Package 101)
FE = 32 Lead Flatpack (Package 220)

DEVICE GRADE: _____

M = Military Screened -55°C to +125°C
I = Industrial -40°C to +85°C
C = Commercial 0°C to +70°C

V_{PP} PROGRAMMING VOLTAGE _____

5 = 5V

LEAD FINISH: _____

Blank = Gold plated leads
A = Solder dip leads

DEVICE TYPE	SECTOR SIZE	SPEED	PACKAGE	SMD NO.
512K x 8 Flash Monolithic	64KByte	150ns	32 pin DIP (C)	5962-96692 01HXX
512K x 8 Flash Monolithic	64KByte	120ns	32 pin DIP (C)	5962-96692 02HXX
512K x 8 Flash Monolithic	64KByte	90ns	32 pin DIP (C)	5962-96692 03HXX
512K x 8 Flash Monolithic	64KByte	70ns	32 pin DIP (C)	5962-96692 04HXX
512K x 8 Flash Monolithic	64KByte	150ns	32 lead SOJ (DE)	5962-96692 01HYX
512K x 8 Flash Monolithic	64KByte	120ns	32 lead SOJ (DE)	5962-96692 02HYX
512K x 8 Flash Monolithic	64KByte	90ns	32 lead SOJ (DE)	5962-96692 03HYX
512K x 8 Flash Monolithic	64KByte	70ns	32 lead SOJ (DE)	5962-96692 04HYX
512K x 8 Flash Monolithic	64KByte	150ns	32 lead Flatpack (FE)	5962-96692 01HUX
512K x 8 Flash Monolithic	64KByte	120ns	32 lead Flatpack (FE)	5962-96692 02HUX
512K x 8 Flash Monolithic	64KByte	90ns	32 lead Flatpack (FE)	5962-96692 03HUX
512K x 8 Flash Monolithic	64KByte	70ns	32 lead Flatpack (FE)	5962-96692 04HUX



Document Title

512K x 8 Flash Monolithic

Revision History

<u>Rev #</u>	<u>History</u>	<u>Release Date</u>	<u>Status</u>
	Initial Release	September 1996	Preliminary
	Changes (Pg. 1)	May 1997	Final
	1.1 Change status to Final		
	Changes (Pg. 1)	February 1998	Final
	1.1 Correct typo of Ceramic		
	Changes (Pg. 10)	April 1998	Final
	1.1 Remove pedestal from Flatpack package drawing		
	Changes (Pg. 1)	February 1999	Final
	1.1 Change name from 'FP' to Flatpack		
Rev 2	Changes (Pg. 1, 2, 3, 4, 13)	May 1999	Final
	1.1 Change number of max program/erases to 1,000,000		
	1.2 Change temperature of max program/erases to 25C		
	1.3 Absolute Maximum Ratings Table:		
	1.3.1 Change Data Retention to 20years		
	1.3.2 Change Endurance to 100,000 cycles minimum		
	1.4 Write/Erase/Program Operations Tables:		
	1.4.1 Change t_{WHWH1} to 300ms		
	1.4.2 Add Note (1) Typical $t_{WHWH1} = 7ms$		
	1.4.3 Change t_{WHWH2} to 15sec		
	1.4.4 Add Note (2) Typical $t_{WHWH2} = 1 sec$		
	1.4.5 Change Chip Programming Time to 11 sec		
	1.4.6 Change Chip Erase Time too 64 sec		
	1.4.7 Add Note (3) Chip Erase Time = 8 sec		
	1.5 Ordering Information		
	1.5.1 Change Company Name to White EDC		
	1.6 Change Title Style to new WEDC look		
Rev 3	Changes (Pg. 1, 2, 10, 12, 13)	May 1999	Final
	1.1 Change package 206 to package 220		
	1.2 Remove temperature range notice for Endurance		
	1.3 Change width spec to 0.457" minimum for package 601		
Rev 4	Changes (Pg. 1, 3, 4)	January 2003	Final
	1.1 Add 60ns speed grade option		