

## 256Kx32 SRAM MODULE PRELIMINARY\*

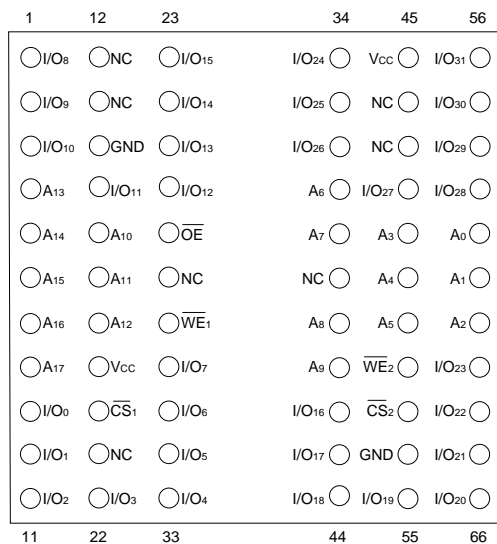
### FEATURES

- Access Times 20, 25, 35ns
- MIL-STD-883 Compliant Devices Available
- Packaging
  - 66 pin, PGA Type, 1.185 inch square, Hermetic Ceramic HIP (Package 401)
  - 68 lead, 40mm, Hermetic CQFP (Package 501)
- Organized as 256Kx32, User Configurable as 512Kx16
- Upgradable to 512Kx32 for future expansion
- Data I/O Compatible with 3.3V devices
- 2V Data Retention devices available (WS256K32L-XXX low power version only)
- Commercial, Industrial and Military Temperature Range
- 5 Volt Power Supply
- Low Power CMOS
- TTL Compatible Inputs and Outputs
- Weight
  - WS256K32N-XXH - 13 grams typical
  - WS256K32-XG4X - 20 grams typical

\* This data sheet describes a product under development, not fully characterized, and is subject to change without notice.

**FIG. 1 PIN CONFIGURATION FOR WS256K32N-XXH**

#### TOP VIEW



#### PIN DESCRIPTION

I/O <sub>0</sub> -31	Data Inputs/Outputs
A <sub>0</sub> -17	Address Inputs
WE <sub>1</sub> -2	Write Enables
CS <sub>1</sub> -2	Chip Selects
OE	Output Enable
V <sub>CC</sub>	Power Supply
GND	Ground
NC	Not Connected

#### BLOCK DIAGRAM

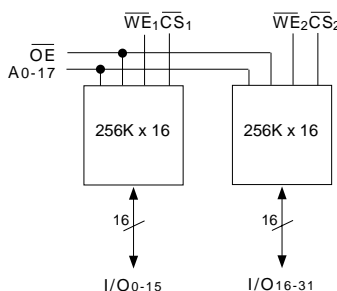
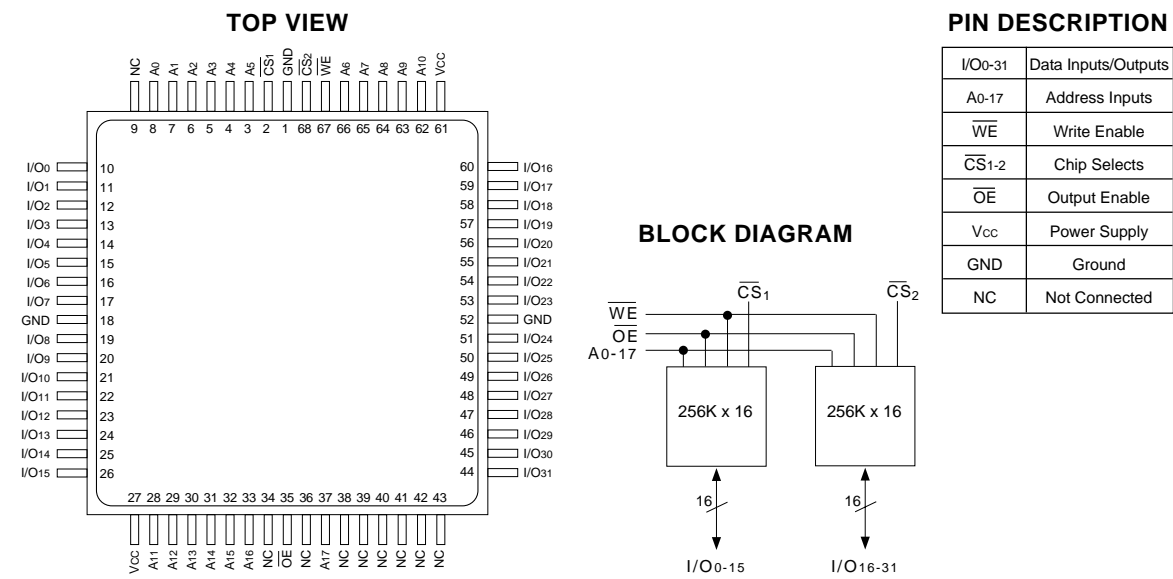
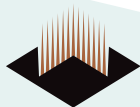




FIG. 2 PIN CONFIGURATION FOR WS256K32-XG4X





## ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T <sub>A</sub>	-55	+125	°C
Storage Temperature	T <sub>STG</sub>	-65	+150	°C
Signal Voltage Relative to GND	V <sub>G</sub>	-0.5	V <sub>CC</sub> +0.5	V
Junction Temperature	T <sub>J</sub>		150	°C
Supply Voltage	V <sub>CC</sub>	-0.5	7.0	V

## RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V <sub>CC</sub>	4.5	5.5	V
Input High Voltage	V <sub>IH</sub>	2.2	V <sub>CC</sub> + 0.3	V
Input Low Voltage	V <sub>IL</sub>	-0.5	+0.8	V
Operating Temp (Mil)	T <sub>A</sub>	-55	+125	°C

## TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	H	H	Out Disable	High Z	Active
L	X	L	Write	Data In	Active

## CAPACITANCE

(T<sub>A</sub> = +25°C)

Parameter	Symbol	Conditions	Max	Unit
$\overline{OE}$ capacitance	C <sub>OE</sub>	V <sub>IN</sub> = 0 V, f = 1.0 MHz	28	pF
$\overline{WE}$ 1-2 capacitance HIP (PGA)	C <sub>WE</sub>	V <sub>IN</sub> = 0 V, f = 1.0 MHz	20	pF
CQFP G4			28	
$\overline{CS}$ 1-2 capacitance	C <sub>CS</sub>	V <sub>IN</sub> = 0 V, f = 1.0 MHz	20	pF
Data I/O capacitance	C <sub>I/O</sub>	V <sub>I/O</sub> = 0 V, f = 1.0 MHz	20	pF
Address input capacitance	C <sub>AD</sub>	V <sub>IN</sub> = 0 V, f = 1.0 MHz	28	pF

This parameter is guaranteed by design but not tested.

## DC CHARACTERISTICS

(V<sub>CC</sub> = 5.0V, GND = 0V, T<sub>A</sub> = -55°C to +125°C)

Parameter	Symbol	Conditions	Units	
			Min	Max
Input Leakage Current	I <sub>LI</sub>	V <sub>CC</sub> = 5.5, V <sub>IN</sub> = GND to V <sub>CC</sub>		10
Output Leakage Current	I <sub>LO</sub>	$\overline{CS}$ = V <sub>IH</sub> , $\overline{OE}$ = V <sub>IH</sub> , V <sub>OUT</sub> = GND to V <sub>CC</sub>		10
Operating Supply Current x 32 Mode	I <sub>CC</sub> x 32	$\overline{CS}$ = V <sub>IL</sub> , $\overline{OE}$ = V <sub>IH</sub> , f = 5MHz, V <sub>CC</sub> = 5.5		550
Standby Current	I <sub>SB</sub>	$\overline{CS}$ = V <sub>IH</sub> , $\overline{OE}$ = V <sub>IH</sub> , f = 5MHz, V <sub>CC</sub> = 5.5		34
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 8mA, V <sub>CC</sub> = 4.5		0.4
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -4.0mA, V <sub>CC</sub> = 4.5	2.4	

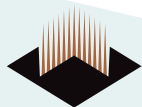
NOTE: DC test conditions: V<sub>IH</sub> = V<sub>CC</sub> - 0.3V, V<sub>IL</sub> = 0.3V

## LOW POWER DATA RETENTION CHARACTERISTICS

(WS256K32L-XXX ONLY)

(T<sub>A</sub> = -55°C to +125°C)

Parameter	Symbol	Conditions	Units		
			Min	Typ	Max
Data Retention Supply Voltage	V <sub>DR</sub>	$\overline{CS} \geq V_{CC} - 0.2V$	2.0		5.5
Data Retention Current	I <sub>CCDR3</sub>	V <sub>CC</sub> = 3V		1.0	16



### AC CHARACTERISTICS

(V<sub>CC</sub> = 5.0V, GND = 0V, T<sub>A</sub> = -55°C to +125°C)

Parameter	Symbol	-20		-25		-35		Units
		Min	Max	Min	Max	Min	Max	
Read Cycle								
Read Cycle Time	t <sub>RC</sub>	20		25		35		ns
Address Access Time	t <sub>AA</sub>		20		25		35	ns
Output Hold from Address Change	t <sub>OH</sub>	0		0		0		ns
Chip Select Access Time	t <sub>ACS</sub>		20		25		35	ns
Output Enable to Output Valid	t <sub>OE</sub>		12		15		20	ns
Chip Select to Output in Low Z	t <sub>CLZ</sub> <sup>1</sup>	5		5		5		ns
Output Enable to Output in Low Z	t <sub>OLZ</sub> <sup>1</sup>	0		0		0		ns
Chip Disable to Output in High Z	t <sub>CHZ</sub> <sup>1</sup>		12		15		20	ns
Output Disable to Output in High Z	t <sub>OHZ</sub> <sup>1</sup>		12		15		20	ns

1. This parameter is guaranteed by design but not tested.

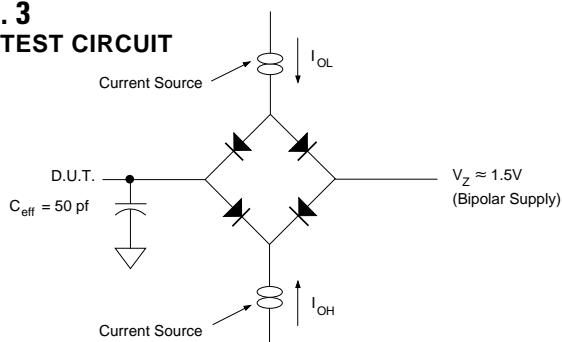
### AC CHARACTERISTICS

(V<sub>CC</sub> = 5.0V, GND = 0V, T<sub>A</sub> = -55°C to +125°C)

Parameter	Symbol	-20		-25		-35		Units
		Min	Max	Min	Max	Min	Max	
Write Cycle								
Write Cycle Time	t <sub>WC</sub>	20		25		35		ns
Chip Select to End of Write	t <sub>CW</sub>	17		20		25		ns
Address Valid to End of Write	t <sub>AW</sub>	17		20		25		ns
Data Valid to End of Write	t <sub>DW</sub>	12		15		20		ns
Write Pulse Width	t <sub>WP</sub>	17		20		25		ns
Address Setup Time	t <sub>AS</sub>	0		0		0		ns
Address Hold Time	t <sub>AH</sub>	2		2		2		ns
Output Active from End of Write	t <sub>OW</sub> <sup>1</sup>	0		0		0		ns
Write Enable to Output in High Z	t <sub>WHZ</sub> <sup>1</sup>		8		10		15	ns
Data Hold Time	t <sub>DH</sub>	0		0		0		ns

1. This parameter is guaranteed by design but not tested.

**FIG. 3**  
**AC TEST CIRCUIT**



### AC TEST CONDITIONS

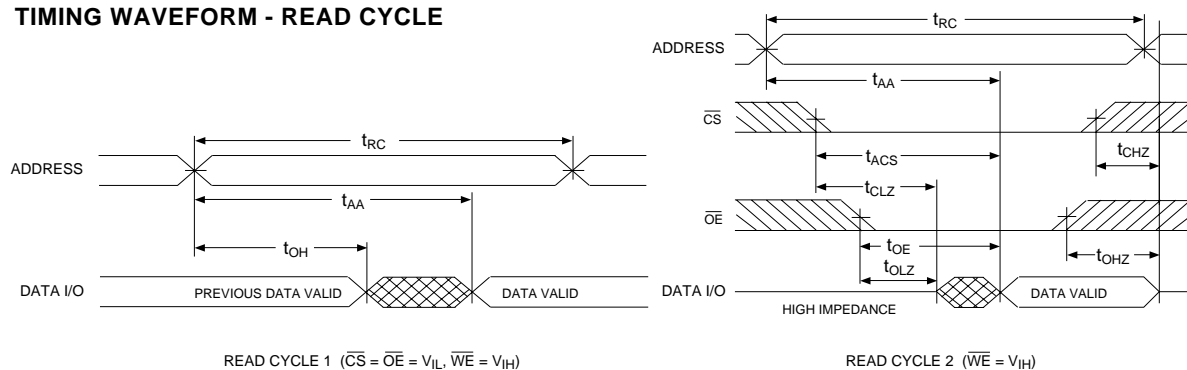
Parameter	Typ	Unit
Input Pulse Levels	$V_{IL} = 0, V_{IH} = 3.0$	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

#### NOTES:

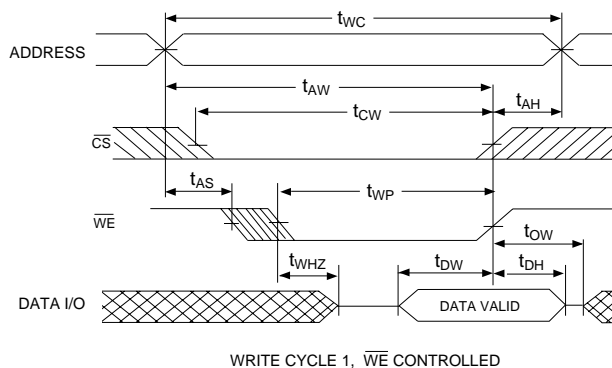
V<sub>Z</sub> is programmable from -2V to +7V.  
I<sub>OL</sub> & I<sub>OH</sub> programmable from 0 to 16mA.  
Tester Impedance Z<sub>0</sub> = 75 Ω.  
V<sub>Z</sub> is typically the midpoint of V<sub>OH</sub> and V<sub>OL</sub>.  
I<sub>OL</sub> & I<sub>OH</sub> are adjusted to simulate a typical resistive load circuit.  
ATE tester includes jig capacitance.



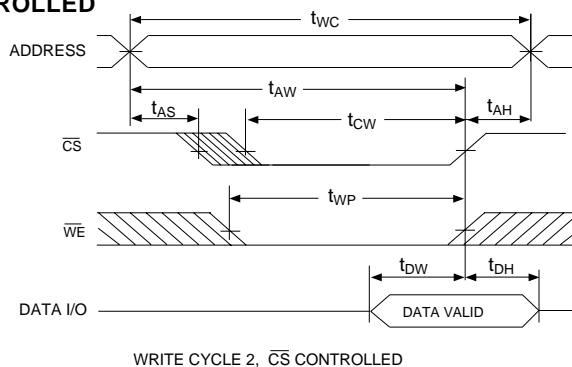
**FIG. 4**  
**TIMING WAVEFORM - READ CYCLE**



**FIG. 5**  
**WRITE CYCLE -  $\overline{WE}$  CONTROLLED**

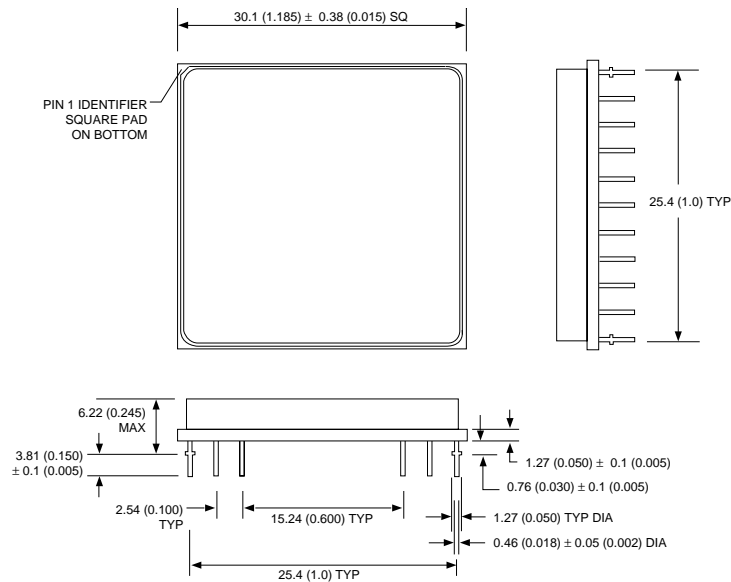


**FIG. 6**  
**WRITE CYCLE -  $\overline{CS}$  CONTROLLED**



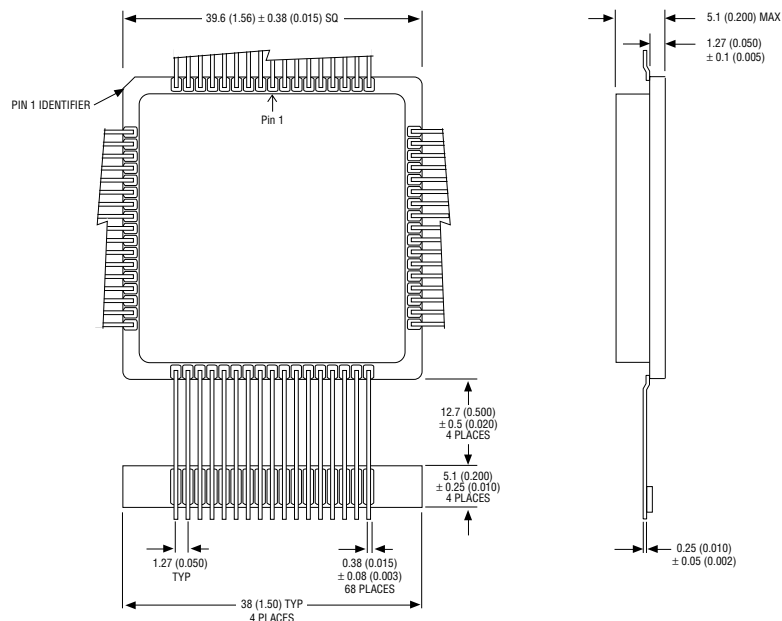


### PACKAGE 401: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H)

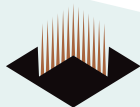


ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

### PACKAGE 501: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G4)



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### ORDERING INFORMATION

**W S 256K32 X - XXX X X X**

#### LEAD FINISH:

Blank = Gold plated leads

A = Solder dip leads

#### DEVICE GRADE:

M = Military Screened -55°C to +125°C

I = Industrial -40°C to +85°C

C = Commercial 0°C to +70°C

#### PACKAGE:

H = Ceramic Hex-In-Line Package, HIP (Package 401)

G4 = 40mm Ceramic Quad Flat Pack, CQFP (Package 501)

#### ACCESS TIME (ns)

#### IMPROVEMENT MARK

N = No Connect at pins 21, 28 and 39 in HIP for Upgrades

Blank = Standard Power

L = Low Power Data Retention

#### ORGANIZATION, 256Kx32

User configurable as 512Kx16

#### SRAM

#### WHITE ELECTRONIC DESIGNS CORP.