

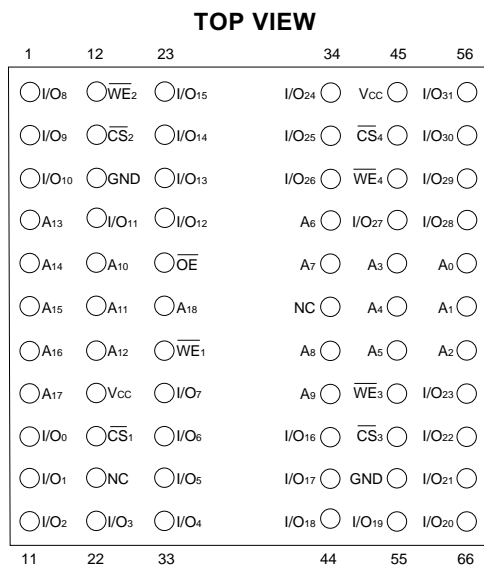
## 512Kx32 SRAM 3.3V MODULE *ADVANCED\**

## FEATURES

- Access Times of 70, 85, 100, 120ns
  - Packaging
    - 66-pin, PGA Type, 1.185 inch square, Hermetic Ceramic HIP (Package 401)
    - 68 lead, Hermetic CQFP (G2T), 22.4mm (0.880 inch) square 4.57mm (0.180 inch) high (Package 509). Designed to fit JEDEC 68 lead 0.990" CQFJ footprint.
  - Organized as 512Kx32, User Configurable as 1024Kx16 or 2Mx8
  - Commercial, Industrial and Military Temperature Ranges
  - TTL Compatible Inputs and Outputs
  - Low Voltage
    - 3.3V  $\pm$ 10% Power Supply
  - Low Power CMOS
  - Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
  - Weight
    - WS512K32V-XG2TX - 8 grams typical
    - WS512K32V-XXH - 13 grams typical
- \* This data sheet describes a product that may or may not be under development and is subject to change or cancellation without notice.*

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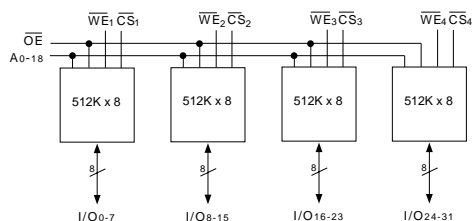
**FIG. 1 PIN CONFIGURATION FOR WS512K32V-XHX**



## PIN DESCRIPTION

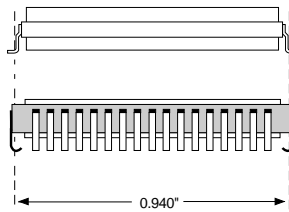
I/O <sub>0-31</sub>	Data Inputs/Outputs
A <sub>0-18</sub>	Address Inputs
WE <sub>1-4</sub>	Write Enables
CS <sub>1-4</sub>	Chip Selects
OE	Output Enable
V <sub>cc</sub>	Power Supply
GND	Ground
NC	Not Connected

### BLOCK DIAGRAM





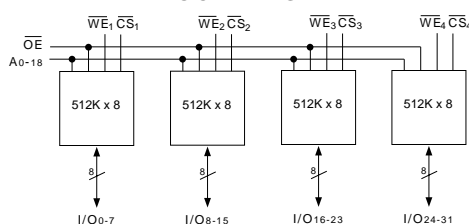
	NC	A0	A1	A2	A3	A4	A5	CS3	GND	CS4	WE1	A6	A7	A8	A9	A10	VCC	
	9	8	7	6	5	4	3	2	1	68	67	66	65	64	63	62	61	
I/O <sub>0</sub>	10																60	I/O <sub>16</sub>
I/O <sub>1</sub>	11																59	I/O <sub>17</sub>
I/O <sub>2</sub>	12																58	I/O <sub>18</sub>
I/O <sub>3</sub>	13																57	I/O <sub>19</sub>
I/O <sub>4</sub>	14																56	I/O <sub>20</sub>
I/O <sub>5</sub>	15																55	I/O <sub>21</sub>
I/O <sub>6</sub>	16																54	I/O <sub>22</sub>
I/O <sub>7</sub>	17																53	I/O <sub>23</sub>
GND	18																52	GND
I/O <sub>8</sub>	19																51	I/O <sub>24</sub>
I/O <sub>9</sub>	20																50	I/O <sub>25</sub>
I/O <sub>10</sub>	21																49	I/O <sub>26</sub>
I/O <sub>11</sub>	22																48	I/O <sub>27</sub>
I/O <sub>12</sub>	23																47	I/O <sub>28</sub>
I/O <sub>13</sub>	24																46	I/O <sub>29</sub>
I/O <sub>14</sub>	25																45	I/O <sub>30</sub>
I/O <sub>15</sub>	26																44	I/O <sub>31</sub>
	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	
	VCC	A11	A12	A13	A14	A15	A16	CS1	OE	CS2	A17	WE2	VE3	VE4	A18	NC	NC	



The WEDC 68 lead G2T CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2T has the TCE and lead inspection advantage of the CQFP form.

I/O <sub>0-31</sub>	Data Inputs/Outputs
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WE <sub>1-4</sub>	Write Enables
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V <sub>cc</sub>	Power Supply
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### BLOCK DIAGRAM





## ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T <sub>A</sub>	-55	+125	°C
Storage Temperature	T <sub>STG</sub>	-65	+150	°C
Signal Voltage Relative to GND	V <sub>G</sub>	-0.5	V <sub>CC</sub> +0.5	V
Junction Temperature	T <sub>J</sub>		150	°C
Supply Voltage	V <sub>CC</sub>	-0.5	4.0	V

## TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	H	H	Out Disable	High Z	Active
L	X	L	Write	Data In	Active

## CAPACITANCE

(T<sub>A</sub> = +25°C)

Parameter	Symbol	Conditions	Max	Unit
$\overline{OE}$ Capacitance	C <sub>OE</sub>	V <sub>IN</sub> = 0 V, f = 1.0 MHz	50	pF
$\overline{WE}$ Capacitance HIP (PGA) CQFP G2T	C <sub>WE</sub>	V <sub>IN</sub> = 0 V, f = 1.0 MHz	20 15	pF
$\overline{CS}$ Capacitance	C <sub>CS</sub>	V <sub>IN</sub> = 0 V, f = 1.0 MHz	20	pF
Data I/O Capacitance	C <sub>I/O</sub>	V <sub>I/O</sub> = 0 V, f = 1.0 MHz	20	pF
Address Input Capacitance	C <sub>AD</sub>	V <sub>IN</sub> = 0 V, f = 1.0 MHz	50	pF

This parameter is guaranteed by design but not tested.

## DC CHARACTERISTICS

(V<sub>CC</sub> = 3.3V, V<sub>SS</sub> = 0V, T<sub>A</sub> = -55°C to +125°C)

Parameter	Symbol	Conditions	Min	Max	Units
Input Leakage Current	I <sub>LI</sub>	V <sub>CC</sub> = 3.6, V <sub>IN</sub> = GND to V <sub>CC</sub>		10	μA
Output Leakage Current	I <sub>LO</sub>	$\overline{CS}$ = V <sub>IH</sub> , $\overline{OE}$ = V <sub>IH</sub> , V <sub>OUT</sub> = GND to V <sub>CC</sub>		10	μA
Operating Supply Current x 32 Mode	I <sub>CC</sub> x 32	$\overline{CS}$ = V <sub>IL</sub> , $\overline{OE}$ = V <sub>IH</sub> , f = 5MHz, V <sub>CC</sub> = 3.6		100	mA
Standby Current	I <sub>SB</sub>	$\overline{CS}$ = V <sub>IH</sub> , $\overline{OE}$ = V <sub>IH</sub> , f = 5MHz, V <sub>CC</sub> = 3.6		2.0	mA
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2.1mA, V <sub>CC</sub> = 3.0		0.4	V
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -1.0mA, V <sub>CC</sub> = 3.0	2.4		V

NOTE: DC test conditions: V<sub>IH</sub> = V<sub>CC</sub> - 0.3V, V<sub>IL</sub> = 0.3V



### AC CHARACTERISTICS

(VCC = 3.3V, VSS = 0V, TA = -55°C to +125°C)

Parameter Read Cycle	Symbol	-70		-85		-100		-120		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	trc	70		85		100		120		ns
Address Access Time	tAA		70		85		100		120	ns
Output Hold from Address Change	toH	5		5		5		5		ns
Chip Select Access Time	tACS		70		85		100		120	ns
Output Enable to Output Valid	toE		35		40		50		60	ns
Chip Select to Output in Low Z	tCLZ <sup>1</sup>	10		10		10		10		ns
Output Enable to Output in Low Z	tOLZ <sup>1</sup>	5		5		5		5		ns
Chip Disable to Output in High Z	tCHZ <sup>1</sup>		25		25		35		35	ns
Output Disable to Output in High Z	toHZ <sup>1</sup>		25		25		35		35	ns

1. This parameter is guaranteed by design but not tested.

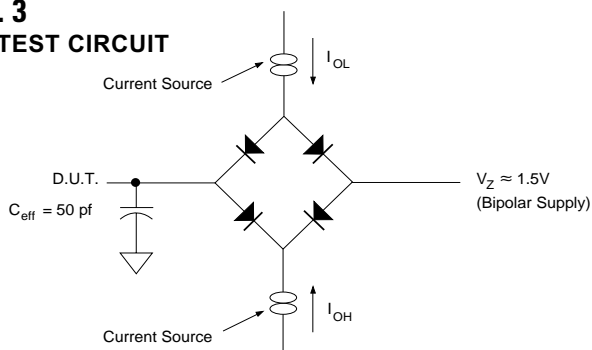
### AC CHARACTERISTICS

(VCC = 3.3V, VSS = 0V, TA = -55°C to +125°C)

Parameter Write Cycle	Symbol	-70		-85		-100		-120		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	twc	70		85		100		120		ns
Chip Select to End of Write	tcw	60		75		80		100		ns
Address Valid to End of Write	tAW	60		75		80		100		ns
Data Valid to End of Write	tdw	30		30		40		40		ns
Write Pulse Width	tWP	50		50		60		60		ns
Address Setup Time	tAS	0		0		0		0		ns
Address Hold Time	tAH	5		5		5		5		ns
Output Active from End of Write	tOW <sup>1</sup>	5		5		5		5		ns
Write Enable to Output in High Z	tWHZ <sup>1</sup>		25		25		35		35	ns
Data Hold from Write Time	tdH	0		0		0		0		ns

1. This parameter is guaranteed by design but not tested.

**FIG. 3**  
**AC TEST CIRCUIT**



### AC TEST CONDITIONS

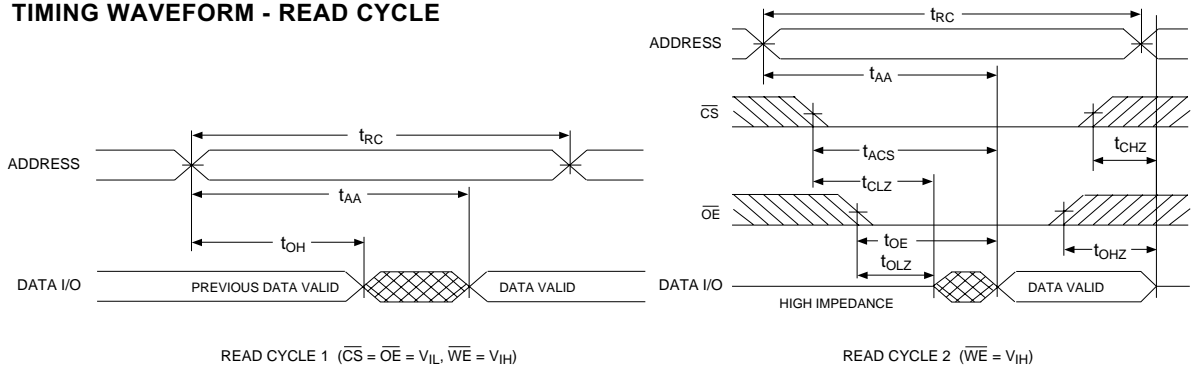
Parameter	Typ	Unit
Input Pulse Levels	V <sub>IL</sub> = 0, V <sub>IH</sub> = 2.5	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

#### NOTES:

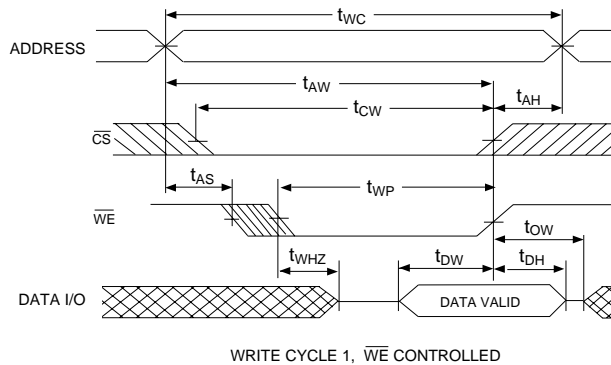
V<sub>Z</sub> is programmable from -2V to +7V.  
I<sub>OL</sub> & I<sub>OH</sub> programmable from 0 to 16mA.  
Tester Impedance Z<sub>0</sub> = 75 Ω.  
V<sub>Z</sub> is typically the midpoint of V<sub>OH</sub> and V<sub>OL</sub>.  
I<sub>OL</sub> & I<sub>OH</sub> are adjusted to simulate a typical resistive load circuit.  
ATE tester includes jig capacitance.



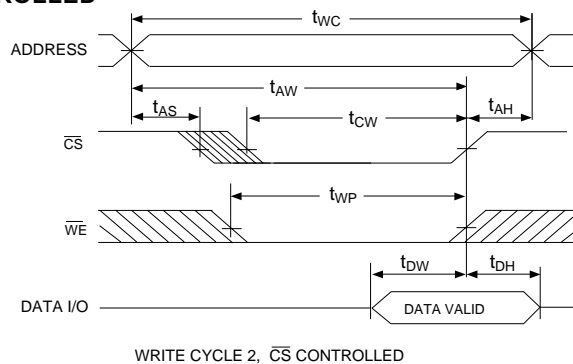
**FIG. 4**  
**TIMING WAVEFORM - READ CYCLE**



**FIG. 5**  
**WRITE CYCLE -  $\overline{WE}$  CONTROLLED**

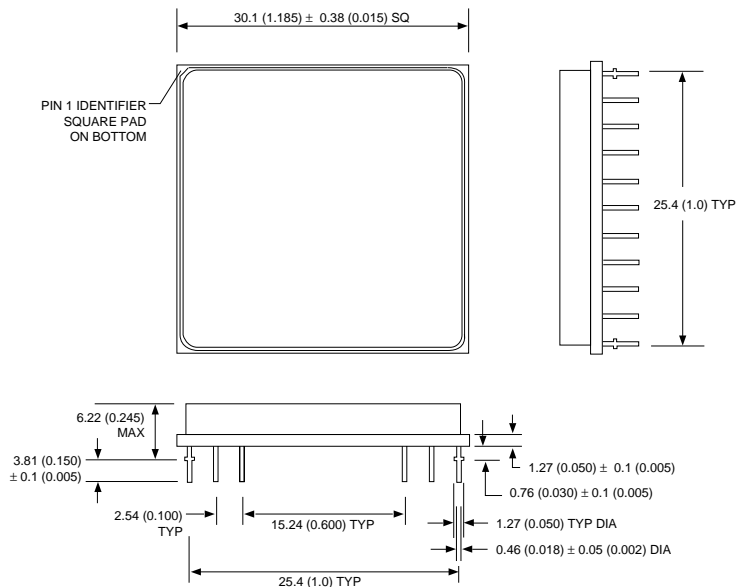


**FIG. 6**  
**WRITE CYCLE -  $\overline{CS}$  CONTROLLED**





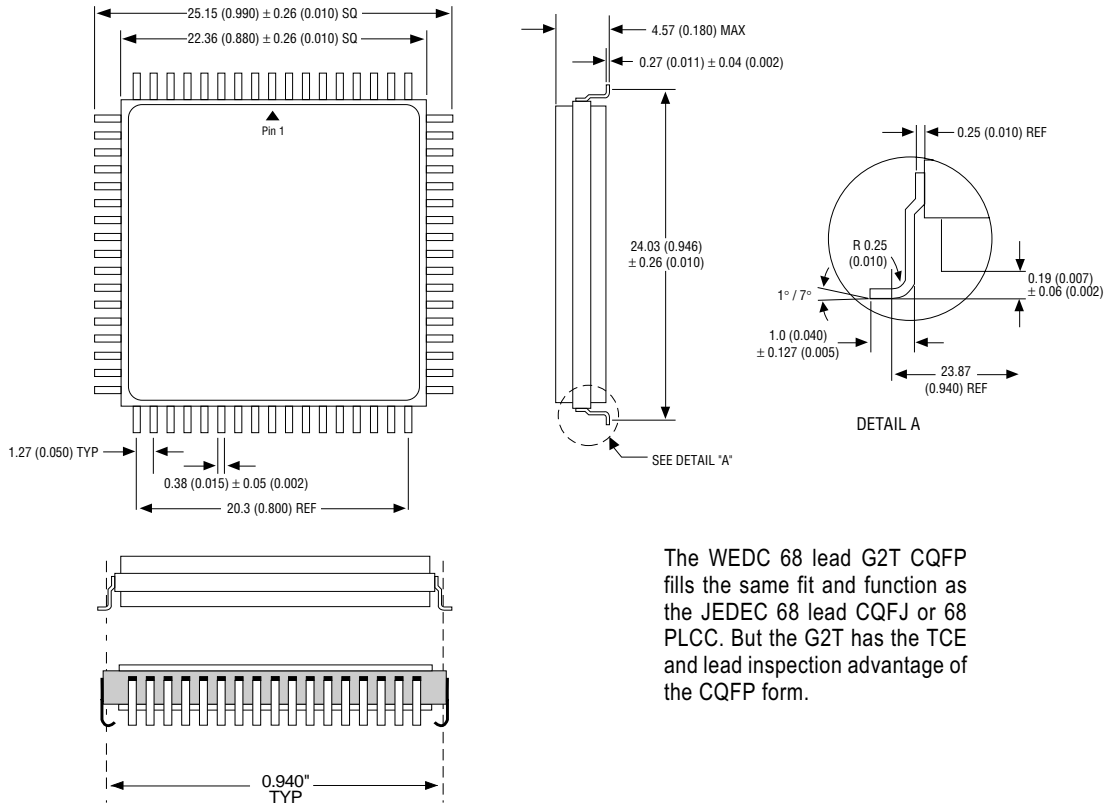
### PACKAGE 401: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



### PACKAGE 509: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G2T)



The WEDC 68 lead G2T CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2T has the TCE and lead inspection advantage of the CQFP form.

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### ORDERING INFORMATION

W S 512K 32 X V - XXX X X X

#### LEAD FINISH:

Blank = Gold plated leads

A = Solder dip leads

#### DEVICE GRADE:

Q = MIL-STD-883 Compliant

M = Military Screened -55°C to +125°C

I = Industrial -40°C to 85°C

C = Commercial 0°C to +70°C

#### PACKAGE TYPE:

H = Ceramic Hex-In-line Package, HIP (Package 401)

G2T = 22.4mm Ceramic Quad Flat Pack, Low Profile CQFP (Package 509)

#### ACCESS TIME (ns)

Low Voltage Supply 3.3V  $\pm$  10%

#### IMPROVEMENT MARK:

N = No Connect at pin 21 and 39 in HIP for Upgrades

#### ORGANIZATION, 512Kx32

User configurable as 1Mx16 or 2Mx8

#### SRAM

WHITE ELECTRONIC DESIGNS CORP.