



## 512Kx32 SRAM 3.3V MULTICHIP PACKAGE PRELIMINARY\*

### FEATURES

- Access Times of 15, 17, 20ns
- Low Voltage Operation
- Packaging
  - 66-pin, PGA Type, 1.075 inch square, Hermetic Ceramic HIP (Package 400)
  - 68 lead, 23.9mm (0.940 inch) sq., Low Profile CQFP, (G1T), 4.06 (0.160 inch) high, (Package 524)
  - 68 lead, 22.4mm (0.880 inch) CQFP, (G2U), 3.56mm (0.140"), (Package 510)
  - 68 lead, 23.9mm (0.940 inch) sq., Low Profile CQFP, (G1U)<sup>1</sup>, 3.56mm (0.140 inch) high, (Package 519)
- Organized as 512Kx32; User Configurable as 1Mx16 or 2Mx8
- Commercial, Industrial and Military Temperature Ranges

- Low Voltage Operation:
  - 3.3V  $\pm$  10% Power Supply
- Low Power CMOS
- TTL Compatible Inputs and Outputs
- Fully Static Operation:
  - No clock or refresh required.
- Three State Output.
- Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight

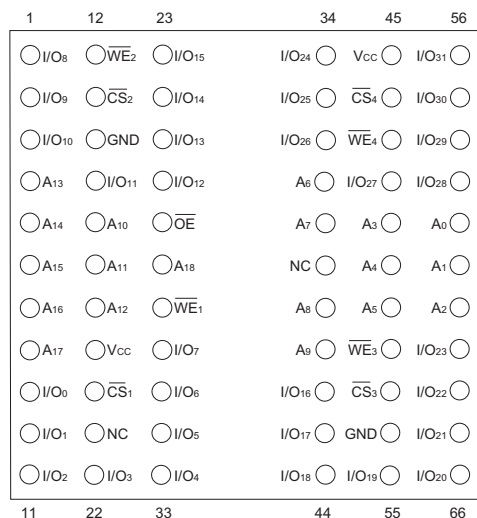
WS512K32V-XG1TX - 5 grams typical  
 WS512K32V-XG1UX<sup>1</sup> - 5 grams typical  
 WS512K32V-XG2UX - 8 grams typical  
 WS512K32NV-XH1X - 13 grams typical

*Note 1: Package Not Recommended For New Design*

*\*This data sheet describes a product under development, not fully characterized, and is subject to change without notice.*

### PIN CONFIGURATION FOR WS512K32NV-XH1X

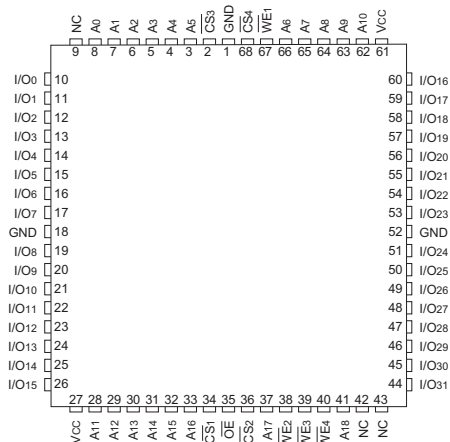
#### TOP VIEW





### PIN CONFIGURATION FOR WS512K32V-XG1TX, WS512K32V-XG2UX AND WS512K32V-XG1UX<sup>1</sup>

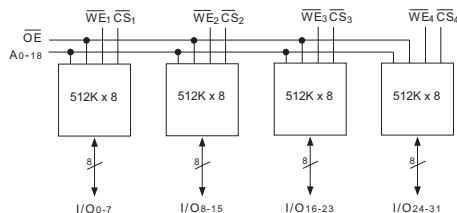
TOP VIEW



PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-18	Address Inputs
$\overline{WE}$ 1-4	Write Enables
$\overline{CS}$ 1-4	Chip Selects
$\overline{OE}$	Output Enable
Vcc	Power Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM



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## ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T <sub>A</sub>	-55	+125	°C
Storage Temperature	T <sub>STG</sub>	-65	+150	°C
Signal Voltage Relative to GND	V <sub>G</sub>	-0.5	4.6	V
Junction Temperature	T <sub>J</sub>		150	°C
Supply Voltage	V <sub>CC</sub>	-0.5	4.6	V

## RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V <sub>CC</sub>	3.0	3.6	V
Input High Voltage	V <sub>IH</sub>	2.2	V <sub>CC</sub> + 0.3	V
Input Low Voltage	V <sub>IL</sub>	-0.3	+0.8	V

## TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active
L	H	H	Out Disable	High Z	Active

## CAPACITANCE (T<sub>A</sub> = +25°C)

Parameter	Symbol	Conditions	Max	Unit
$\overline{OE}$ capacitance	C <sub>OE</sub>	V <sub>IN</sub> = 0 V, f = 1.0 MHz	50	pF
$\overline{WE}$ 1-4 capacitance HIP (PGA) CQFP G2U/G1U/G1T	C <sub>WE</sub>	V <sub>IN</sub> = 0 V, f = 1.0 MHz	20 20	pF
$\overline{CS}$ 1-4 capacitance	C <sub>CS</sub>	V <sub>IN</sub> = 0 V, f = 1.0 MHz	20	pF
Data I/O capacitance	C <sub>I/O</sub>	V <sub>I/O</sub> = 0 V, f = 1.0 MHz	20	pF
Address input capacitance	C <sub>AD</sub>	V <sub>IN</sub> = 0 V, f = 1.0 MHz	50	pF

*This parameter is guaranteed by design but not tested.*

## DC CHARACTERISTICS (V<sub>CC</sub> = 3.3V ± 0.3V, T<sub>A</sub> = -55°C TO +125°C)

Parameter	Sym	Conditions	Min	Max	Units
Input Leakage Current	I <sub>LI</sub>	V <sub>IN</sub> = GND to V <sub>CC</sub>		10	μA
Output Leakage Current	I <sub>LO</sub>	$\overline{CS}$ = V <sub>IH</sub> , $\overline{OE}$ = V <sub>IH</sub> , V <sub>OUT</sub> = GND to V <sub>CC</sub>		10	μA
Operating Supply Current (x 32 Mode)	I <sub>CC</sub> x 32	$\overline{CS}$ = V <sub>IL</sub> , $\overline{OE}$ = V <sub>IH</sub> , f = 5MHz, V <sub>CC</sub> = 3.6V		400	mA
Standby Current	I <sub>SB</sub>	$\overline{CS}$ = V <sub>IH</sub> , $\overline{OE}$ = V <sub>IH</sub> , f = 5MHz, V <sub>CC</sub> = 3.6V		200	mA
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 4.0mA		0.4	V
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -4.0mA	2.4		V

NOTE: DC test conditions: V<sub>IH</sub> = V<sub>CC</sub> - 0.3V, V<sub>IL</sub> = 0.3V.

NOTE: Contact factory for low power option.



## AC CHARACTERISTICS (V<sub>CC</sub> = 3.3V, T<sub>A</sub> = -55°C TO +125°C)

Parameter	Symbol	-15		-17		-20		Units
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t <sub>RC</sub>	15		17		20		ns
Address Access Time	t <sub>AA</sub>		15		17		20	ns
Output Hold from Address Change	t <sub>OH</sub>	0		0		0		ns
Chip Select Access Time	t <sub>ACS</sub>		15		17		20	ns
Output Enable to Output Valid	t <sub>OE</sub>		8		8		10	ns
Chip Select to Output in Low Z	t <sub>CLZ</sub> <sup>1</sup>	1		1		1		ns
Output Enable to Output in Low Z	t <sub>OLZ</sub> <sup>1</sup>	0		0		0		ns
Chip Disable to Output in High Z	t <sub>CHZ</sub> <sup>1</sup>		8		8		10	ns
Output Disable to Output in High Z	t <sub>OHZ</sub> <sup>1</sup>		8		8		10	ns

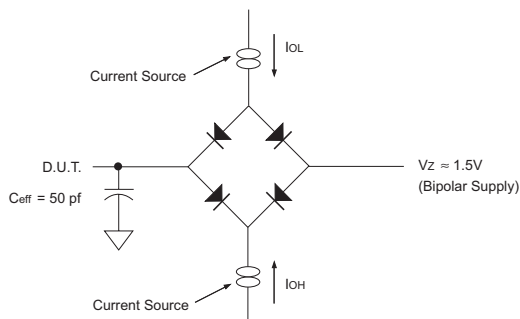
1. This parameter is guaranteed by design but not tested.

## AC CHARACTERISTICS (V<sub>CC</sub> = 3.3V, T<sub>A</sub> = -55°C TO +125°C)

Parameter	Symbol	-15		-17		-20		Units
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t <sub>WC</sub>	15		17		20		ns
Chip Select to End of Write	t <sub>CW</sub>	12		12		14		ns
Address Valid to End of Write	t <sub>AW</sub>	12		12		14		ns
Data Valid to End of Write	t <sub>DW</sub>	9		9		10		ns
Write Pulse Width	t <sub>WP</sub>	12		14		14		ns
Address Setup Time	t <sub>AS</sub>	0		0		0		ns
Address Hold Time	t <sub>AH</sub>	0		0		0		ns
Output Active from End of Write	t <sub>OW</sub> <sup>1</sup>	2		3		3		ns
Write Enable to Output in High Z	t <sub>WHZ</sub> <sup>1</sup>		8		8		9	ns
Data Hold Time	t <sub>DH</sub>	0		0		0		ns

1. This parameter is guaranteed by design but not tested.

### AC TEST CIRCUIT



### AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V <sub>IL</sub> = 0, V <sub>IH</sub> = 2.5	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

#### Notes:

V<sub>Z</sub> is programmable from -2V to +7V.

I<sub>OL</sub> & I<sub>OH</sub> programmable from 0 to 16mA.

Tester Impedance Z<sub>o</sub> = 75Ω.

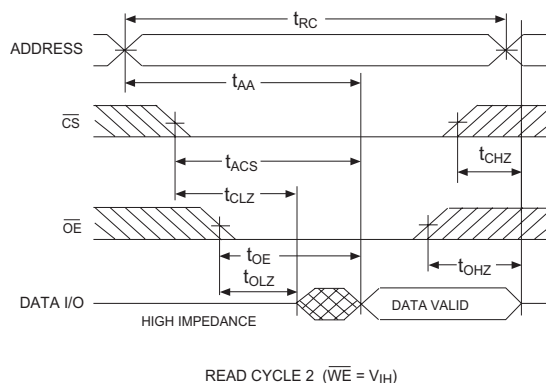
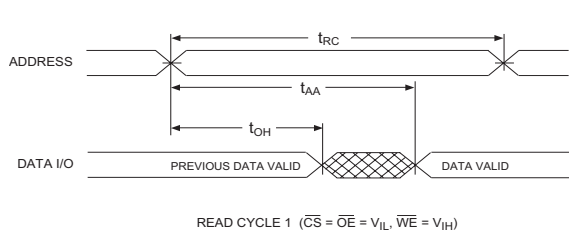
V<sub>Z</sub> is typically the midpoint of V<sub>OH</sub> and V<sub>OL</sub>.

I<sub>OL</sub> & I<sub>OH</sub> are adjusted to simulate a typical resistive load circuit.

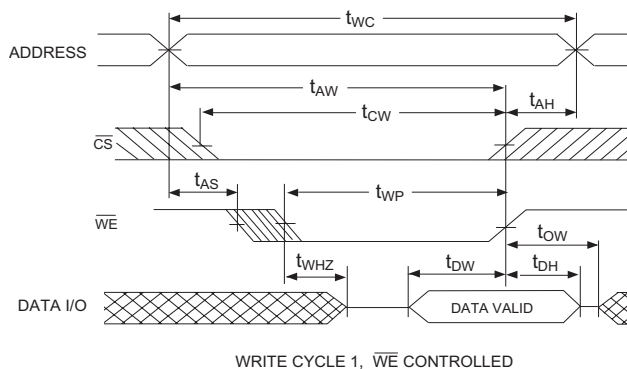
ATE tester includes jig capacitance.



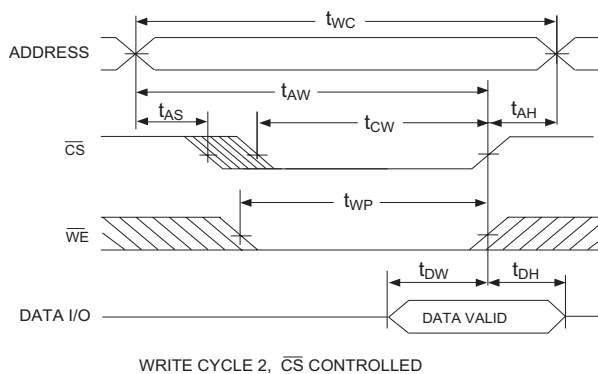
## TIMING WAVEFORM - READ CYCLE



## WRITE CYCLE - $\overline{WE}$ CONTROLLED



## WRITE CYCLE - $\overline{CS}$ CONTROLLED



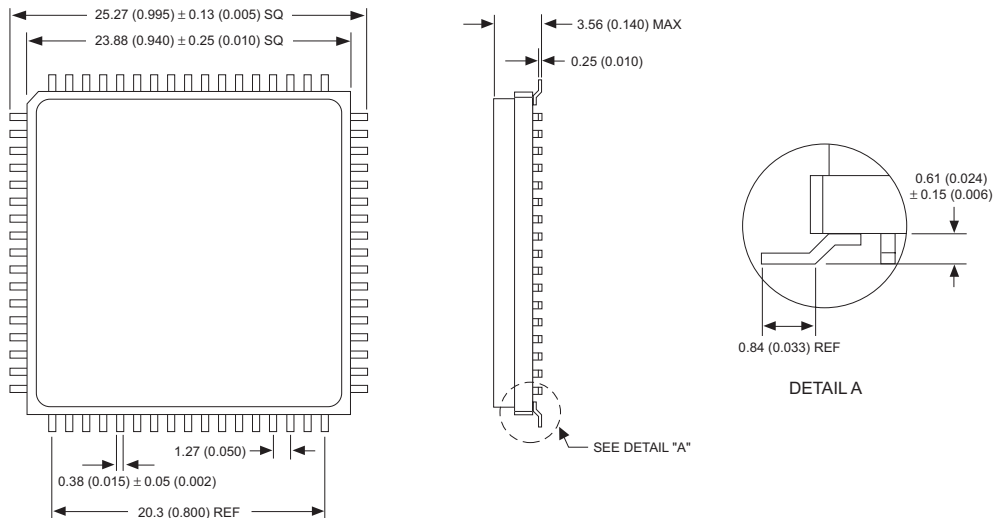


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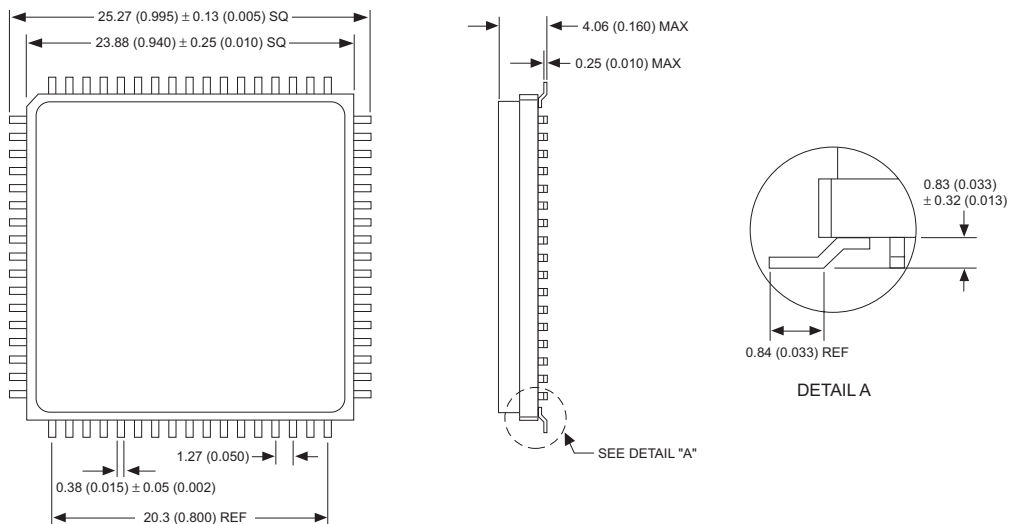
## PACKAGE 519: 68 LEAD, LOW PROFILE CERAMIC QUAD FLAT PACK, CQFP (G1U)<sup>1</sup>



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## PACKAGE 524: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G1T)



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### ORDERING INFORMATION

	W	S	512K 32	X	V	- XXX	X	X	X
WHITE ELECTRONIC DESIGNS CORP. _____									
SRAM _____									
ORGANIZATION, 512Kx32 _____ User configurable as 1Mx16 or 2Mx8									
IMPROVEMENT MARK: _____ N = No Connect at pin 21 and 39 in HIP for Upgrades (H1 only)									
Low Voltage Supply 3.3V $\pm$ 10% _____									
ACCESS TIME (ns) _____									
PACKAGE TYPE: _____ H1 = 1.075" sq. Ceramic Hex In Line Package, HIP (Package 400) G2U = 22.4mm Ceramic Quad Flat Pack, CQFP (Package 510) G1U <sup>1</sup> = 23.9mm Ceramic Quad Flat Pack, Low Profile CQFP (Package 519) G1T = 23.9mm Ceramic Quad Flat Pack, Low Profile CQFP (Package 524)									
DEVICE GRADE: _____ M = Military            -55°C to +125°C I = Industrial        -40°C to +85°C C = Commercial      0°C to +70°C									
LEAD FINISH: _____ Blank = Gold plated leads A = Solder dip leads									

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