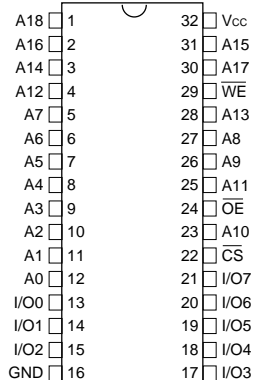




### 512Kx8 SRAM MODULE, SMD 5962-92078

FIG. 1

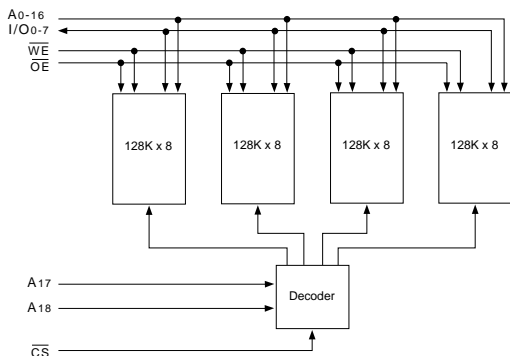
#### PIN CONFIGURATION TOP VIEW



#### PIN DESCRIPTION

A0-18	Address Inputs
I/O0-7	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
Vcc	+5.0V Power
GND	Ground

#### BLOCK DIAGRAM



#### FEATURES

- Access Times 20, 25, 35, 45ns
- Standard Microcircuit Drawing, 5962-92078
- MIL-STD-883 Compliant Devices Available
- Rad Tolerant Devices Available
- JEDEC Standard 32 pin, Hermetic Ceramic DIP (Package 300)
- Commercial, Industrial and Military Temperature Range (-55°C to +125°C)
- Organized as 512K x 8
- 5 Volt Power Supply
- Low Power CMOS
- TTL Compatible Inputs and Outputs
- Battery Back-Up Operation



## ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T <sub>A</sub>	-55	+125	°C
Storage Temperature	T <sub>STG</sub>	-65	+150	°C
Signal Voltage Relative to GND	V <sub>S</sub>	-0.5	V <sub>CC</sub> +0.5	V
Junction Temperature	T <sub>J</sub>		150	°C
Supply Voltage	V <sub>CC</sub>	-0.5	7.0	V

## RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V <sub>CC</sub>	4.5	5.5	V
Input High Voltage	V <sub>IH</sub>	2.2	V <sub>CC</sub> + 0.3	V
Input Low Voltage	V <sub>IL</sub>	-0.5	+0.8	V
Operating Temp. (Mil.)	T <sub>A</sub>	-55	+125	°C

## TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active
L	H	H	Out Disable	High Z	Active

## CAPACITANCE

(T<sub>A</sub> = +25°C)

Parameter	Symbol	Condition	Max	Unit
Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> = 0V, f = 1.0MHz	45	pF
Output capacitance	C <sub>OUT</sub>	V <sub>OUT</sub> = 0V, f = 1.0MHz	45	pF

This parameter is guaranteed by design but not tested.

## DC CHARACTERISTICS

(V<sub>CC</sub> = 5.0V, GND = 0V, T<sub>A</sub> = -55°C to +125°C)

Parameter	Symbol	Conditions	-20		-25		-35		-45		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
Input Leakage Current	I <sub>LI</sub>	V <sub>CC</sub> = 5.5, V <sub>IN</sub> = GND to V <sub>CC</sub>		10		10		10		10	μA
Output Leakage Current	I <sub>LO</sub>	$\overline{CS}$ = V <sub>IH</sub> , $\overline{OE}$ = V <sub>IH</sub> , V <sub>OUT</sub> = GND to V <sub>CC</sub>		10		10		10		10	μA
Operating Supply Current	I <sub>CC</sub>	$\overline{CS}$ = V <sub>IL</sub> , $\overline{OE}$ = V <sub>IH</sub> , f = 5MHz, V <sub>CC</sub> = 5.5		210		210		210		210	mA
Standby Current	I <sub>SB</sub>	$\overline{CS}$ = V <sub>IH</sub> , $\overline{OE}$ = V <sub>IH</sub> , f = 5MHz		80		60		60		55	mA
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 8mA, V <sub>CC</sub> = 4.5		0.4		0.4		0.4		0.4	V
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -4.0mA, V <sub>CC</sub> = 4.5	2.4		2.4		2.4		2.4		V

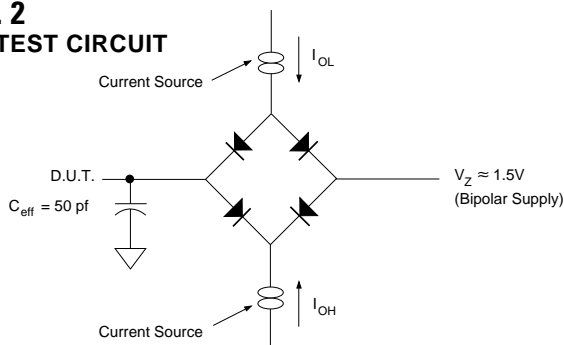
NOTE: DC test conditions: V<sub>IH</sub> = V<sub>CC</sub> - 0.3V, V<sub>IL</sub> = 0.3V

## DATA RETENTION CHARACTERISTICS

(T<sub>A</sub> = -55°C to +125°C)

Parameter	Symbol	Conditions	-20			-25			-35			-45			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Data Retention Supply Voltage	V <sub>DR</sub>	$\overline{CS}$ ≥ V <sub>CC</sub> - 0.2V	2.0		5.5	2.0		5.5	2.0		5.5	2.0		5.5	V
Data Retention Current	I <sub>CCDR1</sub>	V <sub>CC</sub> = 3V		8.0	12.8		8.0	12.8		8.0	12.8		8.0	12.8	mA

**FIG. 2**  
**AC TEST CIRCUIT**



## AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V <sub>IL</sub> = 0, V <sub>IH</sub> = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

### NOTES:

V<sub>Z</sub> is programmable from -2V to +7V.  
I<sub>OL</sub> & I<sub>OH</sub> programmable from 0 to 16mA.  
Tester Impedance Z<sub>0</sub> = 75 Ω.  
V<sub>Z</sub> is typically the midpoint of V<sub>OH</sub> and V<sub>OL</sub>.  
I<sub>OL</sub> & I<sub>OH</sub> are adjusted to simulate a typical resistive load circuit.  
ATE tester includes jig capacitance.



### AC CHARACTERISTICS

(V<sub>CC</sub> = 5.0V, GND = 0V, T<sub>A</sub> = -55°C to +125°C)

Parameter Read Cycle	Symbol	-20		-25		-35		-45		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t <sub>RC</sub>	20		25		35		45		ns
Address Access Time	t <sub>AA</sub>		20		25		35		45	ns
Output Hold from Address Change	t <sub>OH</sub>	3		3		3		3		ns
Chip Select Access Time	t <sub>ACS</sub>		20		25		35		45	ns
Output Enable to Output Valid	t <sub>OE</sub>		10		10		25		35	ns
Chip Select to Output in Low Z	t <sub>CLZ</sub> <sup>1</sup>	3		3		3		3		ns
Output Enable to Output in Low Z	t <sub>OLZ</sub> <sup>1</sup>	0		0		0		0		ns
Chip Disable to Output in High Z	t <sub>CHZ</sub> <sup>1</sup>		15		17		20		30	ns
Output Disable to Output in High Z	t <sub>OHZ</sub> <sup>1</sup>		12		15		20		25	ns

1. This parameter is guaranteed by design but not tested.

### AC CHARACTERISTICS

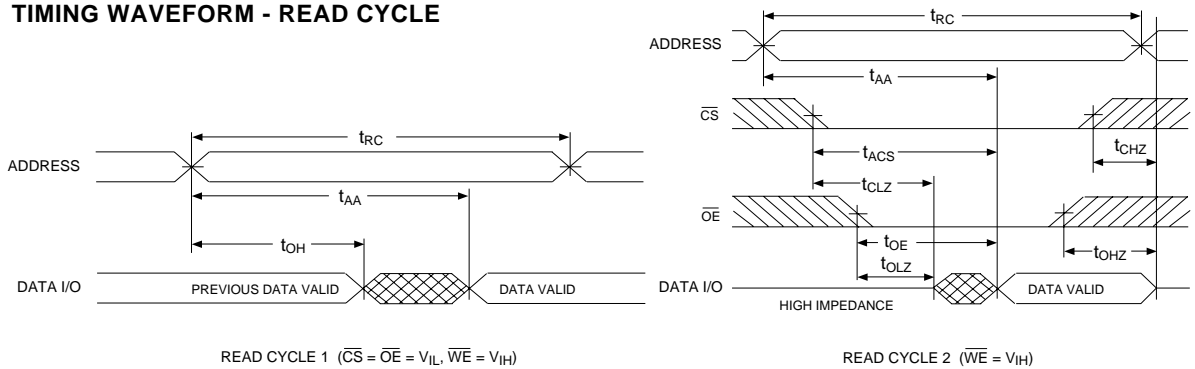
(V<sub>CC</sub> = 5.0V, GND = 0V, T<sub>A</sub> = -55°C to +125°C)

Parameter Write Cycle	Symbol	-20		-25		-35		-45		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t <sub>WC</sub>	20		25		35		45		ns
Chip Select to End of Write	t <sub>CW</sub>	16		20		25		30		ns
Address Valid to End of Write	t <sub>AW</sub>	16		20		25		30		ns
Data Valid to End of Write	t <sub>DW</sub>	15		15		20		25		ns
Write Pulse Width	t <sub>WP</sub>	16		20		25		30		ns
Address Setup Time	t <sub>AS</sub>	2		2		2		2		ns
Address Hold Time	t <sub>AH</sub>	2		2		2		2		ns
Output Active from End of Write	t <sub>OW</sub> <sup>1</sup>	4		5		5		5		ns
Write Enable to Output in High Z	t <sub>WHZ</sub> <sup>1</sup>		10	0	15	0	20	0	25	ns
Data Hold Time	t <sub>DH</sub>	1		1		1		1		ns

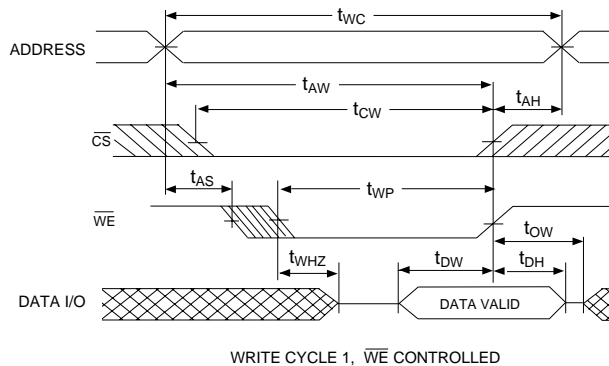
1. This parameter is guaranteed by design but not tested.



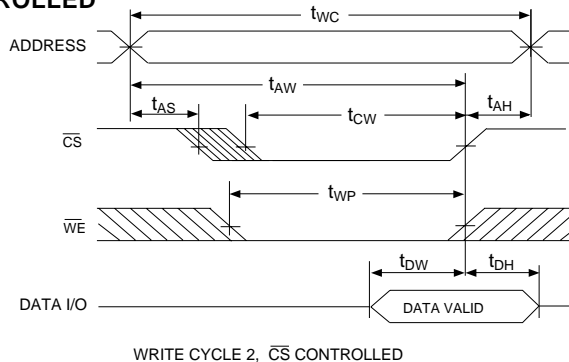
**FIG. 3**  
**TIMING WAVEFORM - READ CYCLE**



**FIG. 4**  
**WRITE CYCLE -  $\overline{WE}$  CONTROLLED**

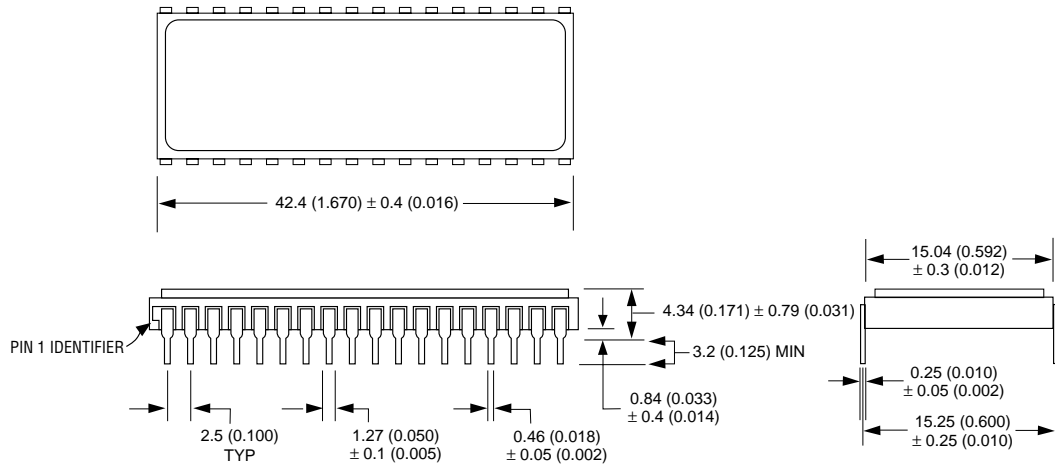


**FIG. 5**  
**WRITE CYCLE -  $\overline{CS}$  CONTROLLED**





### PACKAGE 300: 32 PIN, CERAMIC DIP, SINGLE CAVITY SIDE BRAZED



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



### ORDERING INFORMATION

**W S 512K 8 - XXX C X X**

#### LEAD FINISH:

Blank = Gold plated leads

A = Solder dip leads

#### DEVICE GRADE:

Q = MIL-STD-883 Compliant

M = Military Screened -55°C to +125°C

I = Industrial -40°C to +85°C

C = Commercial 0°C to +70°C

#### PACKAGE:

C = Ceramic 0.600" DIP (Package 300)

#### ACCESS TIME (ns)

#### ORGANIZATION, 512K x 8

#### SRAM

#### WHITE MICROELECTRONICS

DEVICE TYPE	SPEED	PACKAGE	SMD NO.
512K x 8 SRAM	45ns	32 pin DIP	5962-92078 06HTX
512K x 8 SRAM	35ns	32 pin DIP	5962-92078 07HTX
512K x 8 SRAM	25ns	32 pin DIP	5962-92078 08HTX
512K x 8 SRAM	20ns	32 pin DIP	5962-92078 09HTX