

## 1GB – 2x64Mx64 DDR SDRAM UNBUFFERED, w/PLL

### FEATURES

- Double-data-rate architecture
- PC2700 and PC2100
- Bi-directional data strobes (DQS)
- Differential clock inputs (CK & CK#)
- Programmable Read Latency 2, 2.5 (clock)
- Programmable Burst Length (2,4,8)
- Programmable Burst type (sequential & interleave)
- Auto and self refresh, (8K/64ms refresh)
- Serial presence detect with EEPROM
- Power supply:  $V_{cc}/V_{cca}$ : 2.5V  $\pm$  0.2V
- Dual Rank
- 200 pin SO-DIMM package
  - Package height options:  
D4: 31.75 mm (1.25")

NOTE: Consult factory for availability of:

- RoHS compliant products
- Vendor source control options
- Industrial temperature option

### DESCRIPTION

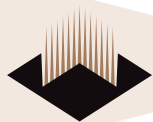
The WV3EG265M64EFSU is a 2x64Mx64 Double Data Rate SDRAM memory module based on 512Mb DDR SDRAM component. The module consists of sixteen 64Mx8 bit with 4 banks DDR SDRAMs in FBGA packages mounted on a 200 pin substrate.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges and Burst Lengths allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

\* This product is subject to change without notice.

### OPERATING FREQUENCIES

	DDR333 @CL=2.5	DDR266 @CL=2	DDR266 @CL=2.5
Clock Speed	166MHz	133MHz	133MHz
CL-tRCD-tRP	2.5-3-3	2-2-2	2.5-3-3

**PIN CONFIGURATION**

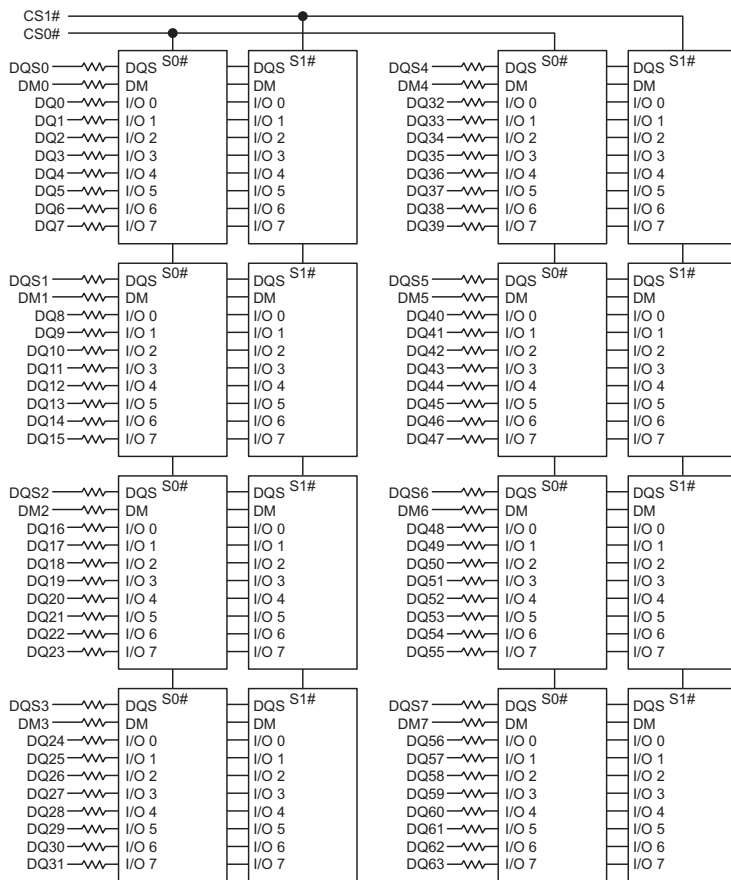
PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	VREF	51	Vss	101	A9	151	DQ42
2	VREF	52	Vss	102	A8	152	DQ46
3	Vss	53	DQ19	103	Vss	153	DQ43
4	Vss	54	DQ23	104	Vss	154	DQ47
5	DQ0	55	DQ24	105	A7	155	Vcc
6	DQ4	56	DQ28	106	A6	156	Vcc
7	DQ1	57	Vcc	107	A5	157	Vcc
8	DQ5	58	Vcc	108	A4	158	NC
9	Vcc	59	DQ25	109	A3	159	Vss
10	Vcc	60	DQ29	110	A2	160	NC
11	DQS0	61	DQS3	111	A1	161	Vss
12	DM0	62	DM3	112	A0	162	Vss
13	DQ2	63	Vss	113	Vcc	163	DQ48
14	DQ6	64	Vss	114	Vcc	164	DQ52
15	Vss	65	DQ26	115	A10	165	DQ49
16	Vss	66	DQ30	116	BA1	166	DQ53
17	DQ3	67	DQ27	117	BA0	167	Vcc
18	DQ7	68	DQ31	118	RAS#	168	Vcc
19	DQ8	69	Vcc	119	WE#	169	DQS6
20	DQ12	70	Vcc	120	CAS#	170	DM6
21	Vcc	71	NC	121	CS0#	171	DQ50
22	Vcc	72	NC	122	CS1#	172	DQ54
23	DQ9	73	NC	123	NC	173	Vss
24	DQ13	74	NC	124	NC	174	Vss
25	DQS1	75	Vss	125	Vss	175	DQ51
26	DM1	76	Vss	126	Vss	176	DQ55
27	Vss	77	NC	127	DQ32	177	DQ56
28	Vss	78	NC	128	DQ36	178	DQ60
29	DQ10	79	NC	129	DQ33	179	Vcc
30	DQ14	80	NC	130	DQ37	180	Vcc
31	DQ11	81	Vcc	131	Vcc	181	DQ57
32	DQ15	82	Vcc	132	Vcc	182	DQ61
33	Vcc	83	NC	133	DQS4	183	DQS7
34	Vcc	84	NC	134	DM4	184	DM7
35	CK0	85	NC	135	DQ34	185	Vss
36	Vcc	86	NC	136	DQ38	186	Vss
37	CK0#	87	Vss	137	Vss	187	DQ58
38	Vss	88	Vss	138	Vss	188	DQ62
39	Vss	89	NC	139	DQ35	189	DQ59
40	Vss	90	Vss	140	DQ39	190	DQ63
41	DQ16	91	NC	141	DQ40	191	Vcc
42	DQ20	92	Vcc	142	DQ44	192	Vcc
43	DQ17	93	Vcc	143	Vcc	193	SDA
44	DQ21	94	Vcc	144	Vcc	194	SA0
45	Vcc	95	CKE1	145	DQ41	195	SCL
46	Vcc	96	CKE0	146	DQ45	196	SA1
47	DQS2	97	NC	147	DQS5	197	VCCSPD
48	DM2	98	NC	148	DM5	198	SA2
49	DQ18	99	A12	149	Vss	199	NC
50	DQ22	100	A11	150	Vss	200	NC

**PIN DESCRIPTION**

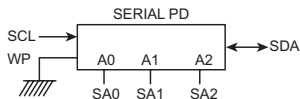
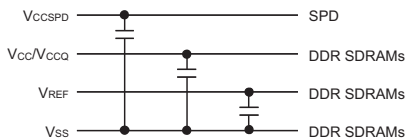
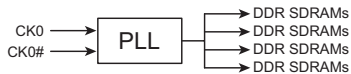
A0-A12	Address input (Multiplexed)
BA0-BA1	Bank Select Address
DQ0-DQ63	Data Input/Output
DQS0-DQS7	Data Strobe Input/Output
CK0, CK0#	Clock Input
CKE0, CKE1	Clock Enable input
CS0#, CS1#	Chip Select Input
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
DM0-DM7	Data-In Mask
Vcc	Power Supply (2.5V)
Vccq	Power Supply for DQS (2.5V)
Vss	Ground
VREF	Power Supply for Reference
VCCSPD	Serial EEPROM Power Supply (2.3V to 3.6V)
SDA	Serial data I/O
SCL	Serial clock
SA0-SA2	Address in EEPROM
NC	No Connect



## FUNCTIONAL BLOCK DIAGRAM



BA0-BA1 → BA0-BA1: DDR SDRAMs  
A0-A12 → A0-A12: DDR SDRAMs  
RAS# → RAS#: DDR SDRAMs  
CAS# → CAS#: DDR SDRAMs  
WE# → WE#: DDR SDRAMs  
CS1# → CS1#: DDR SDRAMs  
CS0# → CS0#: DDR SDRAMs



NOTE: All datalines are terminated through a 22 ohm series resistor

**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Value	Units
Voltage on any pin relative to Vss	V <sub>IN</sub> , V <sub>OUT</sub>	-0.5 to 3.3	V
Voltage on Vcc supply relative to Vss	V <sub>CC</sub>	-1.0 to 3.6	V
Voltage on Vccq supply relative to Vss	V <sub>CCQ</sub>	-1.0 to 3.6	V
Storage Temperature	T <sub>STG</sub>	-55 to +150	°C
Operating Temperature	T <sub>A</sub>	0 to +70	°C
Power Dissipation	P <sub>D</sub>	16	W
Short Circuit Current	I <sub>OS</sub>	50	mA

## Note:

- Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.  
Functional operation should be restricted to recommended operating condition.  
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

**DC CHARACTERISTICS**0°C ≤ T<sub>A</sub> ≤ 70°C, V<sub>CC</sub> = 2.5V ± 0.2V

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage DDR266/DDR333 (nominal V <sub>CC</sub> of 2.5V)	V <sub>CC</sub>	2.3	2.7		
I/O Supply voltage DDR266/DDR333 (nominal V <sub>CC</sub> of 2.5V)	V <sub>CCQ</sub>	2.3	2.7	V	
I/O Reference voltage	V <sub>REF</sub>	0.49*V <sub>CCQ</sub>	0.51*V <sub>CCQ</sub>	V	1
I/O Termination voltage	V <sub>TT</sub>	V <sub>REF</sub> -0.04	V <sub>REF</sub> +0.04	V	2
Input logic high voltage	V <sub>IH</sub> (DC)	V <sub>REF</sub> +0.15	V <sub>CCQ</sub> +0.30	V	
Input logic low voltage	V <sub>IL</sub> (DC)	-0.3	V <sub>REF</sub> -0.15	V	
Input voltage level, CK and CK#	V <sub>IN</sub> (DC)	-0.3	V <sub>CCQ</sub> +0.30	V	
Input differential voltage, CK and CK#	V <sub>ID</sub> (DC)	0.3	V <sub>CCQ</sub> +0.60	V	3
Input crossing point voltage, CK and CK#	V <sub>IX</sub> (DC)	0.3	V <sub>CCQ</sub> +0.60	V	
Input leakage current	Addr, CAS#, RAS#, WE#	I <sub>I</sub>	-32	32	uA
	CS#, CKE		-16	16	uA
	CK, CK#		-10	-10	uA
	DM		-4	4	uA
Output leakage current	I <sub>OZ</sub>	-10	10	uA	
Output high current (normal strength); V <sub>OUT</sub> = V + 0.84V	I <sub>OH</sub>	-16.8	—	mA	
Output high current (normal strength); V <sub>OUT</sub> = V <sub>TT</sub> - 0.84V	I <sub>OL</sub>	16.8	—	mA	
Output high current (half strength); V <sub>OUT</sub> = V <sub>TT</sub> + 0.45V	I <sub>OH</sub>	-9	—	mA	
Output high current (half strength); V <sub>OUT</sub> = V <sub>TT</sub> - 0.45V	I <sub>OL</sub>	9	—	mA	

## NOTES:

- V<sub>REF</sub> is expected to be equal to 0.5\*V<sub>CCQ</sub> of the transmitting device, and to track variations in the DC level of the same. Peak to peak noise on V<sub>REF</sub> may not exceed ±2% of the DC value
- V<sub>TT</sub> is not applied directly to the device. V<sub>TT</sub> is a system supply for signal termination resistors, is expected to be set equal to V<sub>REF</sub>, and must track variations in the DC level of V<sub>REF</sub>
- V<sub>ID</sub> is the magnitude of the difference between the input level on CK and the input level on CK#.

**CAPACITANCE**V<sub>CC</sub> = 2.5V, V<sub>CCQ</sub> = 2.5V, T<sub>A</sub> = 25°C, f = 1MHz

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A0-A12, BA0-BA1, RAS#, CAS#, WE#)	C <sub>IN1</sub>	28	44	pF
Input Capacitance (CKE0, CKE1)	C <sub>IN2</sub>	16	24	pF
Input Capacitance (CS0#, CS1#)	C <sub>IN3</sub>	16	24	pF
Input Capacitance (CLK0, CLK0#)	C <sub>IN4</sub>	6	7.5	pF
Input Capacitance (DM0-DM7)	C <sub>IN5</sub>	11	13	pF
Data and DQS input/output capacitance (DQ0-DQ63)	C <sub>OUT1</sub>	11	13	pF

**I<sub>DD</sub> SPECIFICATIONS AND TEST CONDITIONS**Recommended operating conditions, 0°C ≤ T<sub>A</sub> ≤ 70°C, V<sub>CCQ</sub> = 2.5V ± 0.2V, V<sub>CC</sub> = 2.5V ± 0.2V

Parameter	Symbol	Conditions	DDR333 @ CL = 2.5	DDR266 @ CL = 2	DDR266 @ CL = 2.5	Unit
Operating current	I <sub>DD0</sub> *	One device bank active; Active-Precharge; t <sub>RC</sub> = t <sub>RC(MIN)</sub> ; t <sub>CK</sub> = t <sub>CK(MIN)</sub> ; DQ, DM and DQS inputs change once per clock cycle; Address and control inputs change once every two clock cycles	1360	1240	1240	mA
Operating current	I <sub>DD1</sub> *	One device bank; Active-Read-Precharge; BL = 4; t <sub>RC</sub> = t <sub>RC(MIN)</sub> ; t <sub>CK</sub> = t <sub>CK(MIN)</sub> ; I <sub>OUT</sub> = 0mA; Address and control inputs change once per clock cycle	1600	1480	1480	mA
Percharge power-down standby current	I <sub>DD2P</sub> **	All device banks are idle; Power-down mode; t <sub>CK</sub> = t <sub>CK(MIN)</sub> ; CKE = LOW	360	360	360	mA
Idle standby current	I <sub>DD2F</sub> **	CS# = HIGH; All device banks are idle; t <sub>CK</sub> = t <sub>CK(MIN)</sub> ; CKE = HIGH; Address and other control inputs changing once per clock cycle. V <sub>IN</sub> = V <sub>REF</sub> for DQ, DQS and DM	1000	920	920	mA
Active power-down standby current	I <sub>DD3P</sub> **	One device bank active; Power-down mode; t <sub>CK</sub> = t <sub>CK(MIN)</sub> ; CKE = LOW	840	760	760	mA
Active standby current	I <sub>DD3N</sub> **	CS# = HIGH; CKE = HIGH; One device bank active; t <sub>RC</sub> = t <sub>RAS(MAX)</sub> ; t <sub>CK</sub> = t <sub>CK(MIN)</sub> ; DQ, DM and DQS inputs change twice per clock cycle; Address and other control inputs changing once per clock cycle	1080	1000	1000	mA
Operating current	I <sub>DD4R</sub> *	Burst = 2; Reads; Continuous burst; One device bank active; Address and other control inputs changing once per clock cycle; t <sub>CK</sub> = t <sub>CK(MIN)</sub> ; I <sub>OUT</sub> = 0mA	1640	1480	1480	mA
Operating current	I <sub>DD4W</sub> *	Burst = 2; Writes; Continuous burst; One device bank active; Address and other control inputs changing once per clock cycle; t <sub>CK</sub> = t <sub>CK(MIN)</sub> ; DQ, DM and DQS inputs change twice per clock cycle	1720	1400	1400	mA
Auto refresh current	I <sub>DD5</sub> **	t <sub>RC</sub> = t <sub>RFC(MIN)</sub>	4920	4760	4760	mA
Self refresh current	I <sub>DD6</sub> **	CKE < 0.2V	360	360	360	mA
Operating current	I <sub>DD7</sub> *	Four device bank interleaving Reads Burst = 4 with auto precharge; t <sub>RC</sub> = t <sub>RFC(MIN)</sub> ; t <sub>CK</sub> = t <sub>CK(MIN)</sub> ; Address and control inputs change only during Active READ, or WRITE commands	3560	3120	3120	mA

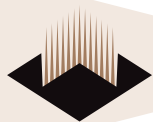
## NOTE:

I<sub>DD</sub> specification is based on Micron components. Other DRAM Manufacturers specification may be different.\* Value calculated as one module rank in this operating condition and all other module ranks in I<sub>DD2P</sub> (CKE low) mode.

\*\* Value calculated reflects all module ranks in this operating condition.

**AC OPERATING TEST CONDITIONS**

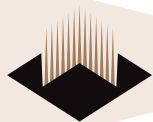
Parameter/Condition	Symbol	Min	Max	Unit
Input High (Logic 1) Voltage	V <sub>IH(AC)</sub>	V <sub>REF</sub> +0.31		V
Input Low (Logic 0) Voltage	V <sub>IL(AC)</sub>		V <sub>REF</sub> -0.31	V
Input Differential Voltage, CK and CK# inputs	V <sub>ID(AC)</sub>	0.7	V <sub>CCQ</sub> +0.6	V
Input Crossing Point Voltage, CK and CK3 inputs	V <sub>IX(AC)</sub>	0.5*V <sub>CCQ</sub> -0.2	0.5*V <sub>CCQ</sub> +0.2	V

**AC TIMING PARAMETERS**0 ≤ T<sub>A</sub> ≤ 70°C, V<sub>CC</sub> = 2.5V, V<sub>CCQ</sub> = 2.5V

Parameter		Symbol	335		262		265		Unit
			Min	Max	Min	Max	Min	Max	
Row cycle time		t <sub>RC</sub>	60		65		65		ns
Refresh row cycletime		t <sub>RFC</sub>	72		75		75		ns
Row active time		t <sub>RAS</sub>	42	70K	40	120K	40	120K	ns
RAS# to CAS# delay		t <sub>RCD</sub>	15		20		20		ns
Row precharge time		t <sub>RP</sub>	15		20		20		ns
Row active to Rowactivedelay		t <sub>RRD</sub>	12		15		15		ns
Write recovery time		t <sub>WR</sub>	15		15		15		ns
Last data into Read command		t <sub>WTR</sub>	1		1		1		ns
Clock cycle time	CL=2.0	t <sub>CK</sub>	7.5	13	7.5	13	10	13	ns
	CL=2.5		6	13	7.5	13	7.5	13	ns
Clock high leve width		t <sub>CH</sub>	0.45	0.55	0.45	0.55	0.45	0.55	tCK
Clock low level width		t <sub>CL</sub>	0.55	0.55	0.55	0.55	0.55	0.55	tCK
DQS-out access time from CK/CK#		t <sub>DQSK</sub>	-0.6	+0.6	-0.75	+0.75	-0.75	+0.75	ns
Output data access time from CK/CK#		t <sub>AC</sub>	-0.7	+0.7	-0.75	+0.75	-0.75	+0.75	ns
Data strobe edge to ouput data edge		t <sub>DQSQ</sub>	—	0.45	—	0.5	—	0.5	ns
Read Preamble		t <sub>RPRE</sub>	0.9	1.1	0.9	1.1	0.9	1.1	tCK
Read Postamble		t <sub>RPST</sub>	0.4	0.6	0.4	0.6	0.4	0.6	tCK
CK to valid DQS-in		t <sub>DQSS</sub>	0.75	1.25	0.75	1.25	0.75	1.25	tCK
DQS-in setup time		t <sub>WPRES</sub>	0		0		0		ns
DQS-in hold time		t <sub>WPRE</sub>	0.25		0.25		0.25		tCK
DQS falling edge to CK rising-setup time		t <sub>DSS</sub>	0.2		0.2		0.2		tCK
DQS falling edge from CK rising-hold time		t <sub>DSH</sub>	0.2		0.2		0.2		tCK
DQS-in high level width		t <sub>DQSH</sub>	0.35		0.35		0.35		tCK
DQS-in low level width		t <sub>DQSL</sub>	0.35		0.35		0.35		tCK
Address and Control Input setup time (fast)		t <sub>ISF</sub>	0.75		0.9		0.9		ns
Address and Control Input hold time (fast)		t <sub>ISHF</sub>	0.75		0.9		0.9		ns
Address and Control Input setup time (slow)		t <sub>ISS</sub>	0.8		1		1		ns
Address and Control Input hold time (slow)		t <sub>ISHS</sub>	0.8		1		1		ns
Data-out high impedance time from CK/CK#		t <sub>HZ</sub>		+0.7		+0.75		+0.75	ns
Data-out low impedance time from CK/CK#		t <sub>LZ</sub>	-0.7		-0.75		-0.75		ns

Note:

AC Timing Parameters are based on Micron components. Other DRAM Manufacturers parameters may be different.

**AC TIMING PARAMETERS (Continued)**0 ≤ T<sub>A</sub> ≤ 70°C, V<sub>CC</sub> = 2.5V, V<sub>CCQ</sub> = 2.5V

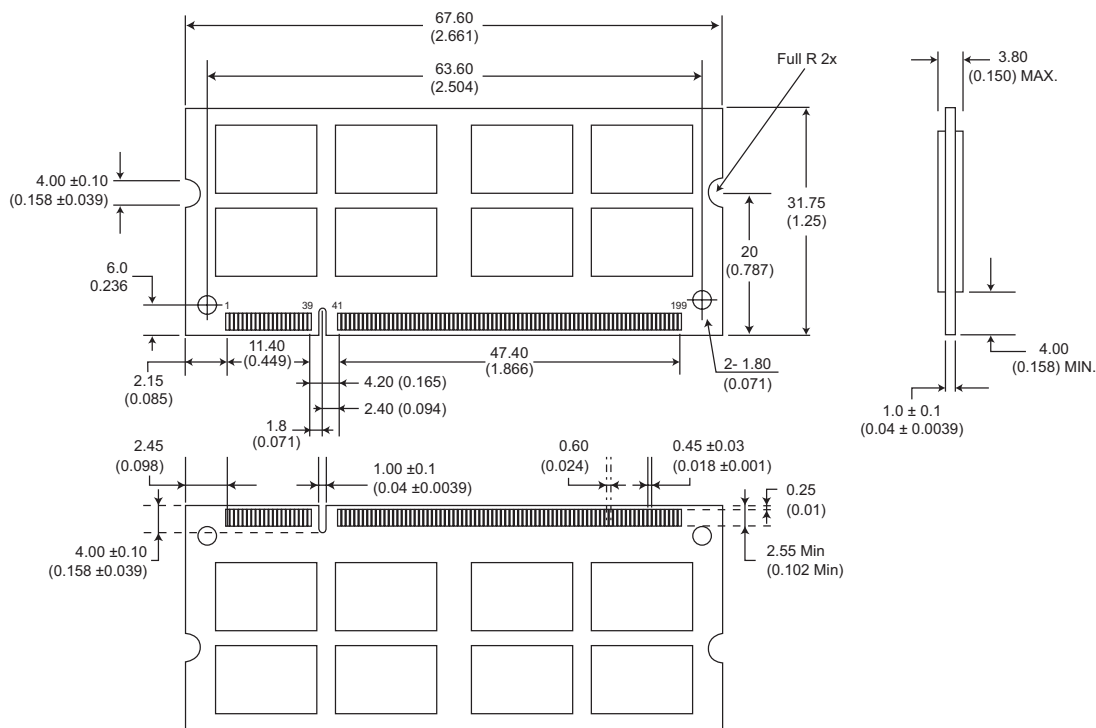
Parameter	Symbol	335		262		265		Unit
		Min	Max	Min	Max	Min	Max	
Mode register set cycle time	t <sub>MRD</sub>	10		10		10		ns
DQ & DM setup time to DQS	t <sub>DS</sub>	0.45		0.5		0.5		ns
DQ & DM hold time to DQS	t <sub>DH</sub>	0.4		0.5		0.5		ns
Control & Address input pulse width	t <sub>IPW</sub>	2.2		2.2		2.2		ns
DQ & DM input pulse width	t <sub>DIPW</sub>	1.75		1.75		1.75		ns
Exit self refresh to non-Read command	t <sub>XSNR</sub>	75		75		75		ns
Exit self refresh to read command	t <sub>XSRD</sub>	200		200		200		t <sub>CK</sub>
Refresh interval time	t <sub>REFI</sub>		7.8		7.8		7.8	us
Output DQS valid window	t <sub>QH</sub>	t <sub>HP</sub> - t <sub>QHS</sub>	—	t <sub>HP</sub> - t <sub>QHS</sub>	—	t <sub>HP</sub> - t <sub>QHS</sub>	—	ns
Clock half period	t <sub>HP</sub>	t <sub>CLmin</sub> or t <sub>CHmin</sub>	—	t <sub>CLmin</sub> or t <sub>CHmin</sub>	—	t <sub>CLmin</sub> or t <sub>CHmin</sub>	—	ns
Data hold skew factor	t <sub>QHS</sub>		0.55		0.75		0.75	ns
DQS write postamble time	t <sub>WPST</sub>	0.4	0.6	0.4	0.6	0.4	0.6	ns
Active to Read with Auto precharge command	t <sub>RAP</sub>	15		20		20		ns
Auto precharge write recovery + Precharge time	t <sub>RAL</sub>	(t <sub>WR</sub> /t <sub>CK</sub> ) + (t <sub>RP</sub> /t <sub>CK</sub> )		(t <sub>WR</sub> /t <sub>CK</sub> ) + (t <sub>RP</sub> /t <sub>CK</sub> )		(t <sub>WR</sub> /t <sub>CK</sub> ) + (t <sub>RP</sub> /t <sub>CK</sub> )		t <sub>CK</sub>

**ORDERING INFORMATION FOR D4**

Part Number	Speed	CAS Latency	t <sub>RC</sub> D	t <sub>RP</sub>	Height*
WV3EG265M64EFSU335D4-x	166MHz/333Mb/s	2.5	3	3	31.75mm (1.25")
WV3EG265M64EFSU262D4-x	133MHz/266Mb/s	2	2	2	31.75mm (1.25")
WV3EG265M64EFSU265D4-x	133MHz/266Mb/s	2.5	3	3	31.75mm (1.25")

**NOTES:**

- Consult Factory for availability of RoHS compliant products. (G = RoHS Compliant)
- Vendor specific part numbers are used to provide memory components source control. The place holder for this is shown as lower case "-x" in the part numbers above and is to be replaced with the respective vendors code. Consult factory for qualified sourcing options. (M = Micron, S = Samsung & consult factory for others)
- Consult factory for availability of industrial temperature (-40°C to 85°C) option

**PACKAGE DIMENSIONS FOR D4**

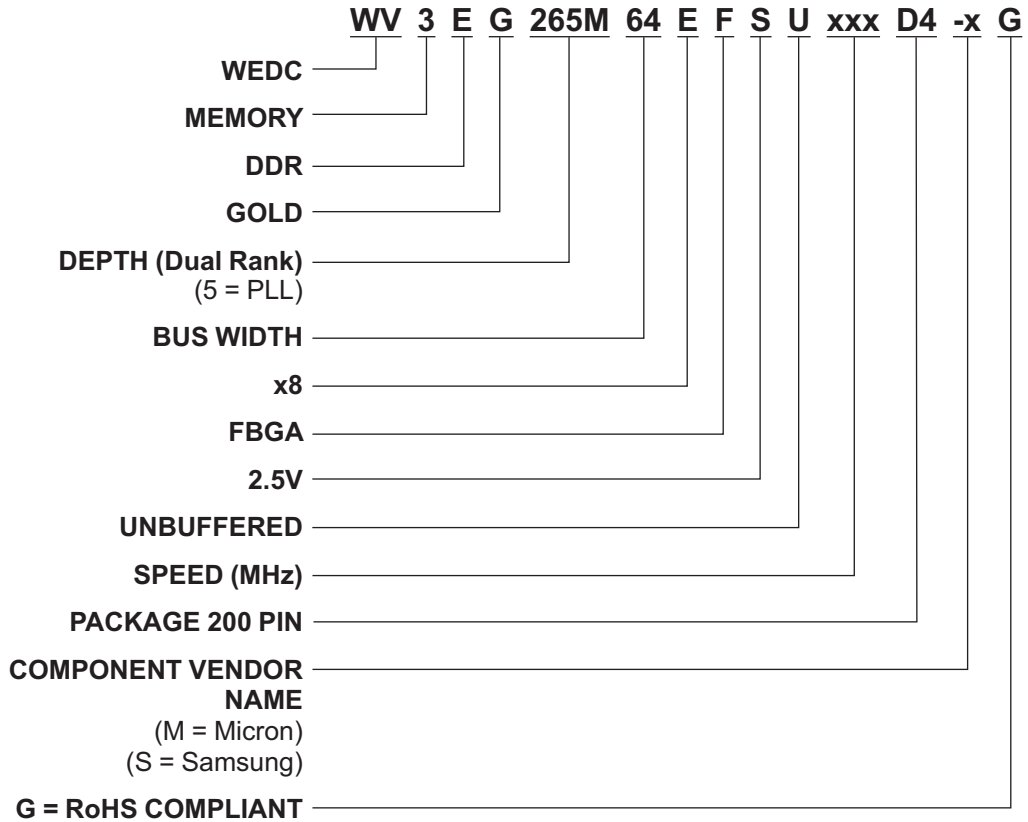
Tolerances: ±0.15 (0.006) unless otherwise specified

\* ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)





### PART NUMBERING GUIDE





## Document Title

1GB – 2x64Mx64 DDR SDRAM UNBUFFERED, w/PLL

## Revision History

Rev #	History	Release Date	Status
Rev 0	Initial Release	8-05	Preliminary
Rev 1	Moved from Preliminary to Final	10-05	Final