



# 1GB – 2x64Mx72 DDR SDRAM, UNBUFFERED, PLL, FBGA

## FEATURES

- Unbuffered 200-pin (SO-DIMM), small-outline, dual-in-line module
- Fast data transfer rate: PC-2100, and PC-2700
- Clock speeds of 133MHz, and 166MHz
- Supports ECC error detection and correction
- $V_{cc} = V_{ccq} = +2.5V \pm 0.2V$  (133 and 166MHz)
- Bi-directional data strobes (DQS)
- Differential clock inputs (CK & CK#)
- Programmable Read Latency: DDR 266 (2, 2.5 clock), DDR333 (2.5 clock)
- Programmable Burst Length (2, 4, 8)
- Programmable Burst type (sequential & interleave)
- Edge aligned data output, center aligned data input
- Auto and self refresh, 7.8 $\mu$ s refresh interval (8K/64ms refresh)
- Serial presence detect (SPD) with EEPROM
- Dual Rank
- Leaded & lead-free/RoHS compliant
- Gold edge contacts
- JEDEC standard 200 pin, small-outline, SO-DIMM package
  - PCB height option:  
31.75 mm (1.25")

NOTE: Consult factory for availability of:

- RoHS compliant products
- Vendor source control options
- Industrial temperature option

## DESCRIPTION

The WV3EG265M72EFSU is a 2x64Mx72 Double Data Rate SDRAM memory module based on 512Mb DDR SDRAM components. The module consists of eighteen 64Mx8 DDR SDRAMs in FBGA packages mounted on a 200 pin FR4 substrate.

\* This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.

## OPERATING FREQUENCIES

	DDR333@CL=2.5	DDR266@CL=2	DDR266@CL=2.5
Clock Speed	166MHz	133MHz	133MHz
CL-tRCD-tRP	2.5-3-3	2-2-2	2.5-3-3

**PIN CONFIGURATION**

PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	VREF	51	Vss	101	A9	151	DQ42
2	VREF	52	Vss	102	A8	152	DQ46
3	Vss	53	DQ19	103	Vss	153	DQ43
4	Vss	54	DQ23	104	Vss	154	DQ47
5	DQ0	55	DQ24	105	A7	155	Vcc
6	DQ4	56	DQ28	106	A6	156	Vcc
7	DQ1	57	Vcc	107	A5	157	Vcc
8	DQ5	58	Vcc	108	A4	158	NC
9	Vcc	59	DQ25	109	A3	159	Vss
10	Vcc	60	DQ29	110	A2	160	NC
11	DQS0	61	DQS3	111	A1	161	Vss
12	DM0	62	DM3	112	A0	162	Vss
13	DQ2	63	Vss	113	Vcc	163	DQ48
14	DQ6	64	Vss	114	Vcc	164	DQ52
15	Vss	65	DQ26	115	A10	165	DQ49
16	Vss	66	DQ30	116	BA1	166	DQ53
17	DQ3	67	DQ27	117	BA0	167	Vcc
18	DQ7	68	DQ31	118	RAS#	168	Vcc
19	DQ8	69	Vcc	119	WE#	169	DQS6
20	DQ12	70	Vcc	120	CAS#	170	DM6
21	Vcc	71	CB0	121	CS0#	171	DQ50
22	Vcc	72	CB4	122	CS1#	172	DQ54
23	DQ9	73	CB1	123	NC	173	Vss
24	DQ13	74	CB5	124	NC	174	Vss
25	DQS1	75	Vss	125	Vss	175	DQ51
26	DM1	76	Vss	126	Vss	176	DQ55
27	Vss	77	DQS8	127	DQ32	177	DQ56
28	Vss	78	DM8	128	DQ36	178	DQ60
29	DQ10	79	CB2	129	DQ33	179	Vcc
30	DQ14	80	CB6	130	DQ37	180	Vcc
31	DQ11	81	Vcc	131	Vcc	181	DQ57
32	DQ15	82	Vcc	132	Vcc	182	DQ61
33	Vcc	83	CB3	133	DQS4	183	DQS7
34	Vcc	84	CB7	134	DM4	184	DM7
35	CK0	85	NC	135	DQ34	185	Vss
36	Vcc	86	NC	136	DQ38	186	Vss
37	CK0#	87	Vss	137	Vss	187	DQ58
38	Vss	88	Vss	138	Vss	188	DQ62
39	Vss	89	NC	139	DQ35	189	DQ59
40	Vss	90	Vss	140	DQ39	190	DQ63
41	DQ16	91	NC	141	DQ40	191	Vcc
42	DQ20	92	Vcc	142	DQ44	192	Vcc
43	DQ17	93	Vcc	143	Vcc	193	SDA
44	DQ21	94	Vcc	144	Vcc	194	SA0
45	Vcc	95	CKE1	145	DQ41	195	SCL
46	Vcc	96	CKE0	146	DQ45	196	SA1
47	DQS2	97	NC	147	DQS5	197	VCCSPD
48	DM2	98	NC	148	DM5	198	SA2
49	DQ18	99	A12	149	Vss	199	NC
50	DQ22	100	A11	150	Vss	200	NC

**PIN NAMES**

Symbol	Description
A0-A12	Address input
BA0, BA1	Bank Address
DQ0-DQ63	Data Input/Output
CB0-CB7	Check Bits
DQS0-DQS8	Data Strobe
CK0, CK0#	Clock Input
CKE0-CKE1	Clock Enable Input
CS0#-CS1#	Chip Select Input
RAS#	Row Address Strobe
CAS#	Column Address Input
WE#	Write Enable
DM0-DM8	Data Write Mask
Vcc	Power Supply
Vss	Ground
VREF	SSTL_2 reference voltage
VCCSPD	Serial EEPROM Positive Power Supply
SDA	Input/Output: Serial Presence-Detect Data
SCL	Serial Clock
SA0-SA2	Presence Detect Address Input
NC	No Connect





## DC ELECTRICAL CHARACTERISTICS

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	Notes
Supply Voltage DRR266/DDR333 (nominal V <sub>CC</sub> 2.5V)		V <sub>CC</sub>	2.3	2.7	V	
I/O Supply Voltage DRR266/DDR333 (nominal V <sub>CCQ</sub> 2.5V)		V <sub>CCQ</sub>	2.3	2.7	V	
I/O Reference Voltage		V <sub>REF</sub>	0.49 × V <sub>CC</sub>	0.51 × V <sub>CC</sub>	V	1
I/O Termination Voltage		V <sub>TT</sub>	V <sub>REF</sub> - 0.04	V <sub>REF</sub> + 0.04	V	2
Input Logic High Voltage		V <sub>IH</sub> (DC)	V <sub>REF</sub> + 0.15	V <sub>CC</sub> + 0.30	V	
Input Logic Low Voltage		V <sub>IL</sub> (DC)	-0.3	V <sub>REF</sub> - 0.15	V	
Input voltage level, CK and CK#		V <sub>IN</sub> (DC)	-0.3	V <sub>REF</sub> + 0.30	V	
Input differential voltage, CK and CK#		V <sub>ID</sub> (DC)	0.3	V <sub>REF</sub> + 0.60	V	3
Input crossing point voltage, CK and CK#		V <sub>IX</sub> (DC)	0.3	V <sub>REF</sub> - 0.60	V	
Input leakage current	Addr CAS#, RAS#, WE#	I <sub>I</sub>	-36	36	μA	
	CS#, CKE		-18	18	μA	
	CK, CK#		-10	10	μA	
	DM		-4	4	μA	
Output leakage current		I <sub>OZ</sub>	-10	10	μA	
Output high current (normal strength) V <sub>OUT</sub> = v +0.84V		I <sub>OH</sub>	-16.8		mA	
Output high current (normal strength) V <sub>OUT</sub> = V <sub>TT</sub> - 0.84V		I <sub>OL</sub>	16.8		mA	
Output high current (half strength) V <sub>OUT</sub> = V <sub>TT</sub> - 0.45V		I <sub>OH</sub>	-9		mA	
Output high current (half strength) V <sub>OUT</sub> = V <sub>TT</sub> - 0.45V		I <sub>OL</sub>	9		mA	

### Notes:

- $V_{REF}$  is expected to equal to  $0.5 \times V_{CCQ}$  of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise on  $V_{REF}$  may not exceed  $\pm 2$  percent of the DC value.
- $V_{TT}$  is not applied directly to the device.  $V_{TT}$  is a system supply for signal termination resistors, is expected to be set equal to  $V_{REF}$  and must track variations in the DC level of  $V_{REF}$ .
- $V_{ID}$  is the magnitude of the difference between the input level on CK and the input level of CK#.

## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Units
$V_{IN}, V_{OUT}$	Voltage on $V_{CC}$ pin relative to $V_{SS}$	-0.5 ~ 3.6	V
$V_{CC}, V_{CCQ}$	Voltage on $V_{CC}$ & $V_{CCQ}$ supply relative to $V_{SS}$	-1.0 ~ 3.6	V
$V_{REF}$	Voltage of $V_{REF}$ supply relative to $V_{SS}$	-1.0 ~ 3.6	V
$T_{STG}$	Storage Temperature	-55 ~ +150	$^{\circ}C$
$T_A$	Operating temperature	0 ~ 70	$^{\circ}C$
$P_D$	Power dissipation	18	W
$I_{OS}$	Short circuit output current	50	mA

### Notes:

- Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceed.  
Functional iteration should be restricted to recommended operation conditions.  
Exposing to higher than recommended voltage for extended periods of time could affect device reliability.

**AC OPERATING CONDITIONS**

Parameter	Symbol	Min	Max	Unit
AC Input High (Logic 1) Voltage	$V_{IH}(AC)$	$V_{REF} + 0.31$	-	V
AC Input High (Logic 0) Voltage	$V_{IL}(AC)$	-	$V_{REF} - 0.31$	V
Input Differential Voltage, CK and CK# inputs	$V_{ID}(AC)$	0.7	$V_{CC} + 0.6$	V
Input Crossing Point Voltage, CK and CK# input	$V_{IX}(AC)$	$0.5 \cdot V_{CC} - 0.2$	$0.5 \cdot V_{CC} + 0.2$	V

**INPUT/OUTPUT CAPACITANCE**

TA=25°C, f=100MHz

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0~A12, BA0~BA1, RAS#, CAS#, WE#)	$C_{IN1}$	31	49	pF
Input capacitance (CKE0, CKE1)	$C_{IN2}$	17.5	26.5	pF
Input capacitance (CS0# - CS1#)	$C_{IN3}$	17.5	26.5	pF
Input capacitance (CLK0, CLK0#)	$C_{IN4}$	6	7.5	pF
Input capacitance (DM0~DM8)	$C_{IN5}$	11	13	pF
Input capacitance (DQ0~DQ63), (CB0~CB7)	$C_{OUT1}$	11	13	pF



### I<sub>CC</sub> SPECIFICATIONS AND CONDITIONS

V<sub>CC</sub>, V<sub>CCQ</sub> = +2.5V ±0.2V

SYM	PARAMETER/CONDITION	MAX			UNITS
		DDR333 @CL=2.5	DDR266 @CL=2	DDR266 @CL=2.5	
I <sub>CC0</sub> *	OPERATING CURRENT: One device bank; Active-Precharge; t <sub>RC</sub> = t <sub>RC</sub> (MIN); t <sub>CK</sub> = t <sub>CK</sub> (MIN); DQ, DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles	1,270	1,180	1,180	mA
I <sub>CC1</sub> *	OPERATING CURRENT: One device bank; Active-Read-Precharge; Burst = 4; t <sub>RC</sub> = t <sub>RC</sub> (MIN); t <sub>CK</sub> = t <sub>CK</sub> (MIN); I <sub>OUT</sub> = 0mA; Address and control inputs changing once per clock cycle	1,540	1,450	1,450	mA
I <sub>CC2P</sub> **	PRECHARGE POWER-DOWN STANDBY CURRENT: All device banks idle; Power-down mode; t <sub>CK</sub> = t <sub>CK</sub> (MIN); CKE = (LOW)	370	370	370	mA
I <sub>CC2F</sub> **	IDLE STANDBY CURRENT: CS# = HIGH; All device banks are idle; t <sub>CK</sub> = t <sub>CK</sub> (MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle. V <sub>IN</sub> = V <sub>REF</sub> for DQ, DQS, and DM	820	820	820	mA
I <sub>CC3P</sub> **	ACTIVE POWER-DOWN STANDBY CURRENT: One device bank active; Power-down mode; t <sub>CK</sub> = t <sub>CK</sub> (MIN); CKE = LOW	820	820	820	mA
I <sub>CC3N</sub> **	ACTIVE STANDBY CURRENT: CS# = HIGH; CKE = HIGH; One device bank active; t <sub>RC</sub> = t <sub>RAS</sub> (MAX); t <sub>CK</sub> = t <sub>CK</sub> (MIN); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	1,090	1,090	1,090	mA
I <sub>CC4R</sub> *	OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; t <sub>CK</sub> = t <sub>CK</sub> (MIN); I <sub>OUT</sub> = 0mA	1,585	1,450	1,450	mA
I <sub>CC4W</sub> *	OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; t <sub>CK</sub> = t <sub>CK</sub> (MIN); DQ, DM, and DQS inputs changing twice per clock cycle	1,675	1,495	1,495	mA
I <sub>CC5</sub> **	AUTO REFRESH BURST CURRENT: t <sub>REFC</sub> = t <sub>RFC</sub> (MIN)	3,970	3,790	3,790	mA
I <sub>CC6</sub> **	SELF REFRESH CURRENT: CKE ≤ 0.2V	370	370	370	mA
I <sub>CC7</sub> *	OPERATING CURRENT: Four device bank interleaving READs (Burst = 4) with auto precharge, t <sub>RC</sub> = minimum t <sub>RC</sub> allowed; t <sub>CK</sub> = t <sub>CK</sub> (MIN); Address and control inputs change only during Active READ, or WRITE commands	3,565	3,250	3,250	mA

Note: I<sub>CC</sub> specification is based on **SAMSUNG** components. Other DRAM Manufacturers specification may be different.

\*: Value calculated as one module rank in this operating condition, and all other module ranks in I<sub>CC2P</sub> (CKE LOW) mode.

\*\*: Value calculated reflects all module ranks in this operating condition.



## DDR SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

$V_{CC} = V_{CCQ} = +2.5V \pm 0.2V$

AC CHARACTERISTICS			335		262		265		UNITS
PARAMETER		SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	
Row cycle time		t <sub>RC</sub>	60		65		65		t <sub>CK</sub>
Refresh row cycle time		t <sub>RFC</sub>	72		75		75		ps
Row active		t <sub>RAS</sub>	42	70K	45	120K	45	120K	ps
RAS# to CAS# delay		t <sub>RCD</sub>	18		20		20		t <sub>CK</sub>
Row precharge time		t <sub>RP</sub>	18		20		20		ns
Row active to row active delay		t <sub>RRD</sub>	12		15		15		ns
Write recovery time		t <sub>WR</sub>	15		15		15		ns
Last data in to READ command		t <sub>WTR</sub>	1		1		1		ns
Clock cycle time	CL = 2.5	t <sub>CK (2.5)</sub>	6	12	7.5	12	7.5	12	ns
	CL =2	t <sub>CK (2)</sub>	7.5	12	7.5	12	10	12	ns
Clock high level width		t <sub>CH</sub>	0.45	0.55	0.45	0.55	0.45	0.55	t <sub>CK</sub>
Clock low level width		t <sub>CL</sub>	0.45	0.55	0.45	0.55	0.45	0.55	t <sub>CK</sub>
DQS-out access time from CK/CK#		t <sub>DQSQ</sub>	-0.6	+0.6	-0.75	+0.75	-0.75	+0.75	ns
Output data access time from CK/CK#		t <sub>AC</sub>	-0.7	+0.7	-0.75	+0.75	-0.75	+0.75	ns
Data stobe edge to output data edge		t <sub>DQSQ</sub>		0.45		0.5		0.5	ns
Read preamble		t <sub>RPRE</sub>	0.9	1.1	0.9	1.1	0.9	1.1	t <sub>CK</sub>
Read postamble		t <sub>RPST</sub>	0.4	0.6	0.4	0.6	0.4	0.6	t <sub>CK</sub>
CK to vaild DQS-in		t <sub>DQSS</sub>	0.75	1.25	0.75	1.25	0.75	1.25	t <sub>CK</sub>
DQS-in setup time		t <sub>WPRES</sub>	0		0		0		ns
DQS-in hold time		t <sub>WPRE</sub>	0.25		0.25		0.25		t <sub>CK</sub>
DQS falling edge to CK rising-setup time		t <sub>DSS</sub>	0.2		0.2		0.2		t <sub>CK</sub>
DQS falling edge to CK rising-hold time		t <sub>DHS</sub>	0.2		0.2		0.2		t <sub>CK</sub>
DQS-in high level width		t <sub>DQHS</sub>	0.35		0.35		0.35		t <sub>CK</sub>
DQS-in low level width		t <sub>DQSL</sub>	0.35		0.35		0.35		t <sub>CK</sub>
Address and control input setup time (fast)		t <sub>ISF</sub>	0.75		0.9		0.9		ns
Address and control input hold time (fast)		t <sub>IHF</sub>	0.75		0.9		0.9		ns
Address and control input setup time (slow)		t <sub>ISS</sub>	0.8		1.0		1.0		ns
Address and control input hold time (slow)		t <sub>IHS</sub>	0.8		1.0		1.0		ns
Data-out high impedance time from CK/CK#		t <sub>HZ</sub>	-0.70	+0.70	-0.75	+0.75	-0.75	+0.75	ns
Data-out low impedance time to CK/CK#		t <sub>LZ</sub>	-0.70	+0.70	-0.75	+0.75	-0.75	+0.75	ns
Mode register set cycle		t <sub>MRD</sub>	12		15		15		ns
DQ & DM setup time to DQS		t <sub>DS</sub>	0.45		0.5		0.5		ns
DQ & DM hold time to DQS		t <sub>DH</sub>	0.45		0.5		0.5		ns
Control & address input pulse width		t <sub>IPW</sub>	2.2		2.2		2.2		ns
DQ & DM input pulse width		t <sub>DIPW</sub>	1.75		1.75		1.75		ns
Exit self refresh to non-read command		t <sub>XSNR</sub>	75		75		75		ns

\* AC specification is based on **SAMSUNG** components. Other DRAM manufactures specification may be different.

Continued on next page

**DDR SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED  
AC OPERATING CONDITIONS (Continued)**

$$V_{CC} = V_{CCQ} = +2.5V \pm 0.2V$$

AC CHARACTERISTICS		335		262		265		UNITS
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	
Exit self refresh to read command	t <sub>XSRD</sub>	200		200		200		t <sub>CK</sub>
Refresh interval time	t <sub>REFI</sub>		7.8		7.8		7.8	μs
Output DQS valid window	t <sub>QH</sub>	t <sub>HP</sub> -t <sub>QHS</sub>		t <sub>HP</sub> -t <sub>QHS</sub>		t <sub>HP</sub> -t <sub>QHS</sub>		ns
Clock half period	t <sub>HP</sub>	t <sub>CLmin</sub> or t <sub>CHmin</sub>		t <sub>CLmin</sub> or t <sub>CHmin</sub>		t <sub>CLmin</sub> or t <sub>CHmin</sub>		ns
Data hold skew factor	t <sub>QHS</sub>		0.55		0.75		0.75	ns
DQS write postamble	t <sub>WPST</sub>	0.4	0.6	0.4	0.6	0.4	0.6	ns
Active Read with auto precharge command	t <sub>RAP</sub>	18		20		20		ns
Auto precharge Write recovery + Precharge time	t <sub>RAL</sub>	t <sub>WR</sub> /t <sub>CK</sub> + t <sub>RP</sub> /t <sub>CK</sub>		t <sub>WR</sub> /t <sub>CK</sub> + t <sub>RP</sub> /t <sub>CK</sub>		t <sub>WR</sub> /t <sub>CK</sub> + t <sub>RP</sub> /t <sub>CK</sub>		t <sub>CK</sub>

\* AC specification is based on **SAMSUNG** components. Other DRAM manufactures specification may be different.





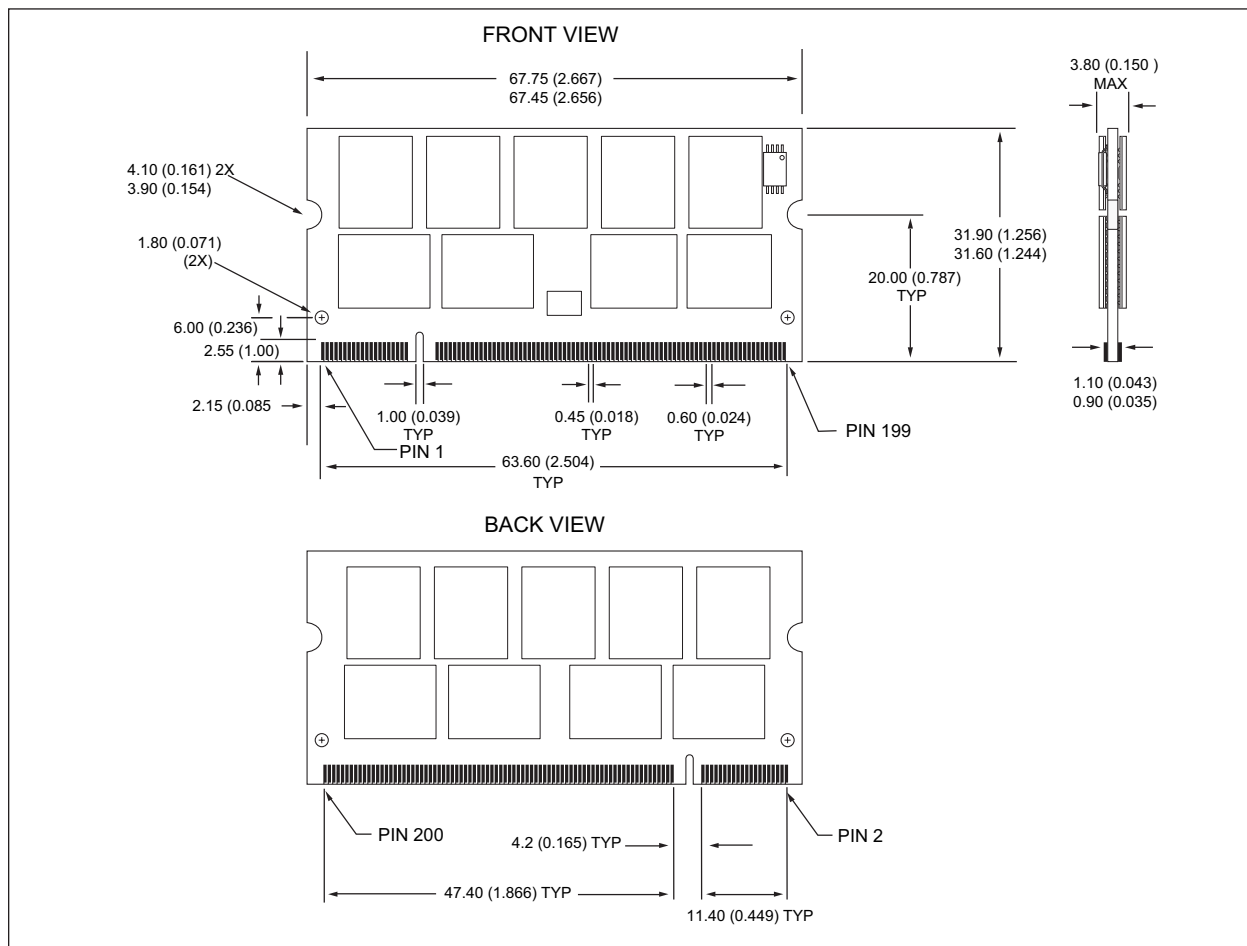
## ORDERING INFORMATION FOR D4

Part Number	Speed	CAS Latency	t <sub>RC</sub> D	t <sub>RP</sub>	Height*
WV3EG265M72EFSU335D4xxx	166MHz/333Mbps	2.5	3	3	31.75 (1.25") MAX
WV3EG265M72EFSU262D4xxx	133MHz/266Mbps	2	2	2	31.75 (1.25") MAX
WV3EG265M72EFSU265D4xxx	133MHz/266Mbps	2.5	3	3	31.75 (1.25") MAX

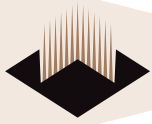
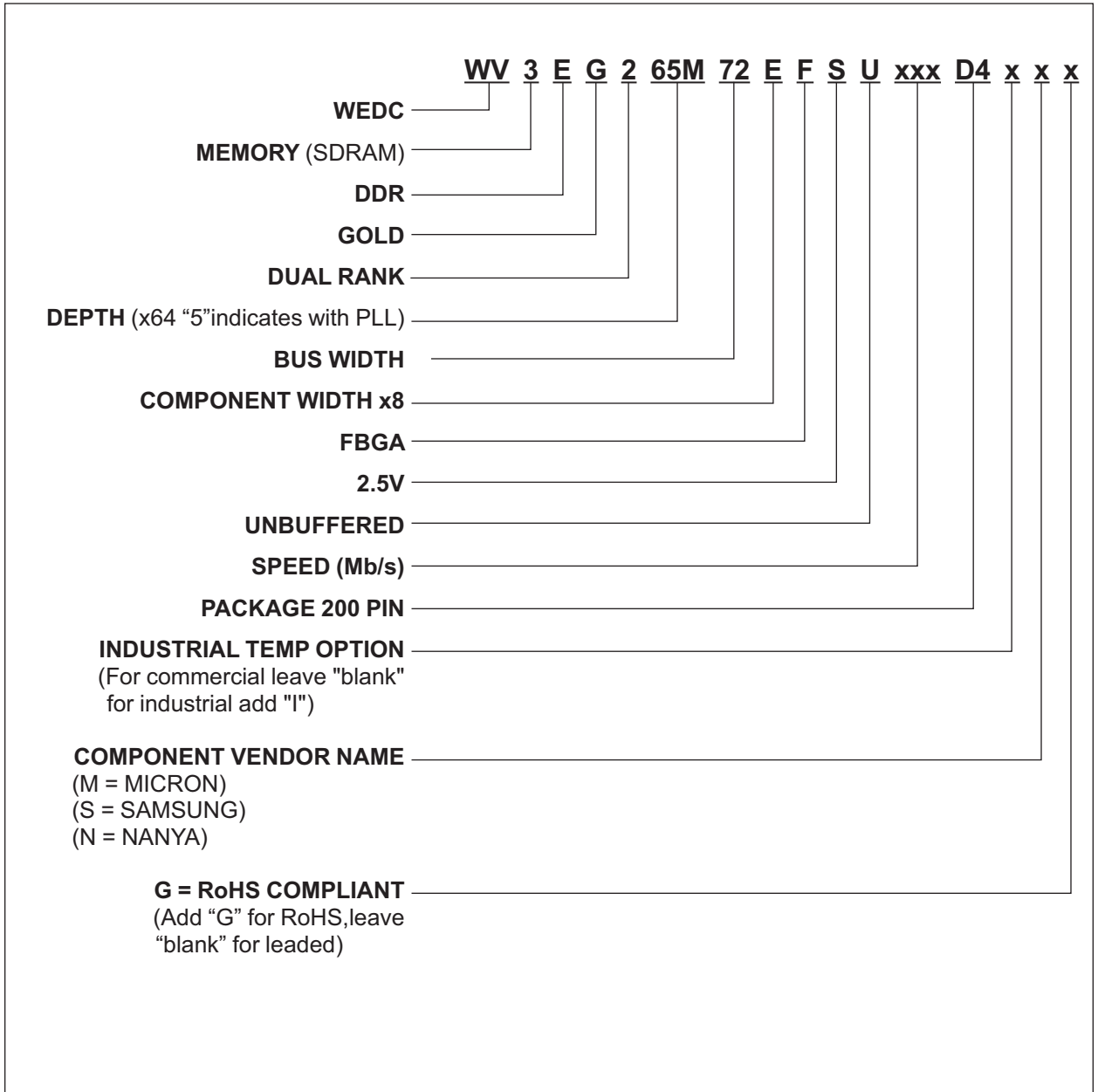
## NOTES:

- Consult Factory for availability of RoHS compliant products. (G = RoHS Compliant)
- Vendor specific part numbers are used to provide memory components source control. The place holder for this is shown as lower case "x" in the part numbers above and is to be replaced with the respective vendors code. Consult factory for qualified sourcing options. (M = Micron, S = Samsung & consult factory for others)
- Consult factory for availability of industrial temperature (-40°C to 85°C) option

## 200-PIN DDR SO-DIMM DIMENSIONS



\* ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)

**PART NUMBERING GUIDE**

**Document Title**

1GB – 2x64Mx72 DDR SDRAM, UNBUFFERED, with PLL, FBGA

**DRAM DIE OPTIONS:**

- SAMSUNG: C-Die
- MICRON: T27Z: D-Die, will move to T37Z:F Q2'06
- NANYA: B-Die

**Revision History**

Rev #	History	Release Date	Status
Rev 0	Created	May 2006	Advanced