



1GB – 2x64Mx72 DDR2 SDRAM UDIMM, SO-DIMM w/PLL

FEATURES

- Unbuffered 200-pin (SO-DIMM) small-outline dual in-line memory module
- Support ECC detection and correction
- Fast data transfer rates: PC2-6400*, PC2-5300*, PC2-4200 and PC2-3200
- $V_{CC} = V_{CCQ} = 1.8V \pm 0.1V$
- $V_{CCSPD} = 1.7V$ to $3.6V$
- JEDEC standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- Differential clock input (CK, CK#)
- Four-bit prefetch architecture
- Multiple internal device banks for concurrent operation
- Programmable CAS# latency (CL): 3 4, 5*, and 6*
- Adjustable data-output drive strength
- 7.8 μ s average periodic refresh interval
- On-die termination (ODT)
- Posted CAS# latency: 0, 1, 2, 3 and 4
- Serial Presence Detect (SPD) with EEPROM
- Auto & self refresh (64ms: 8,192 cycle refresh)
- Gold edge contacts
- Dual Rank
- RoHS compliant
- JEDEC proposed pin-out
- Package option
 - 200 Pin SO-DIMM: 30.00mm (1.181") TYP

DESCRIPTION

The WV3HG264M72EEU is a 2x64Mx72 Double Data Rate DDR2 SDRAM high density module. This memory module consists of eighteen 64Mx8 bit DDR2 Synchronous DRAMs in FBGA packages, mounted on a 200-pin SO-DIMM FR4 substrate.

* This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.

NOTE: Consult factory for availability of:

- Vendor source control options
- Industrial temperature option

OPERATING FREQUENCIES

| | PC2-3200 | PC2-4200 | PC2-5300* | PC2-6400* |
|-------------|----------|----------|-----------|-----------|
| Clock Speed | 200MHz | 266MHz | 333MHz | 400MHz |
| CL-tRCD-tRP | 3-3-3 | 4-4-4 | 5-5-5 | 6-6-6 |

* Consult factory for availability



PIN CONFIGURATION

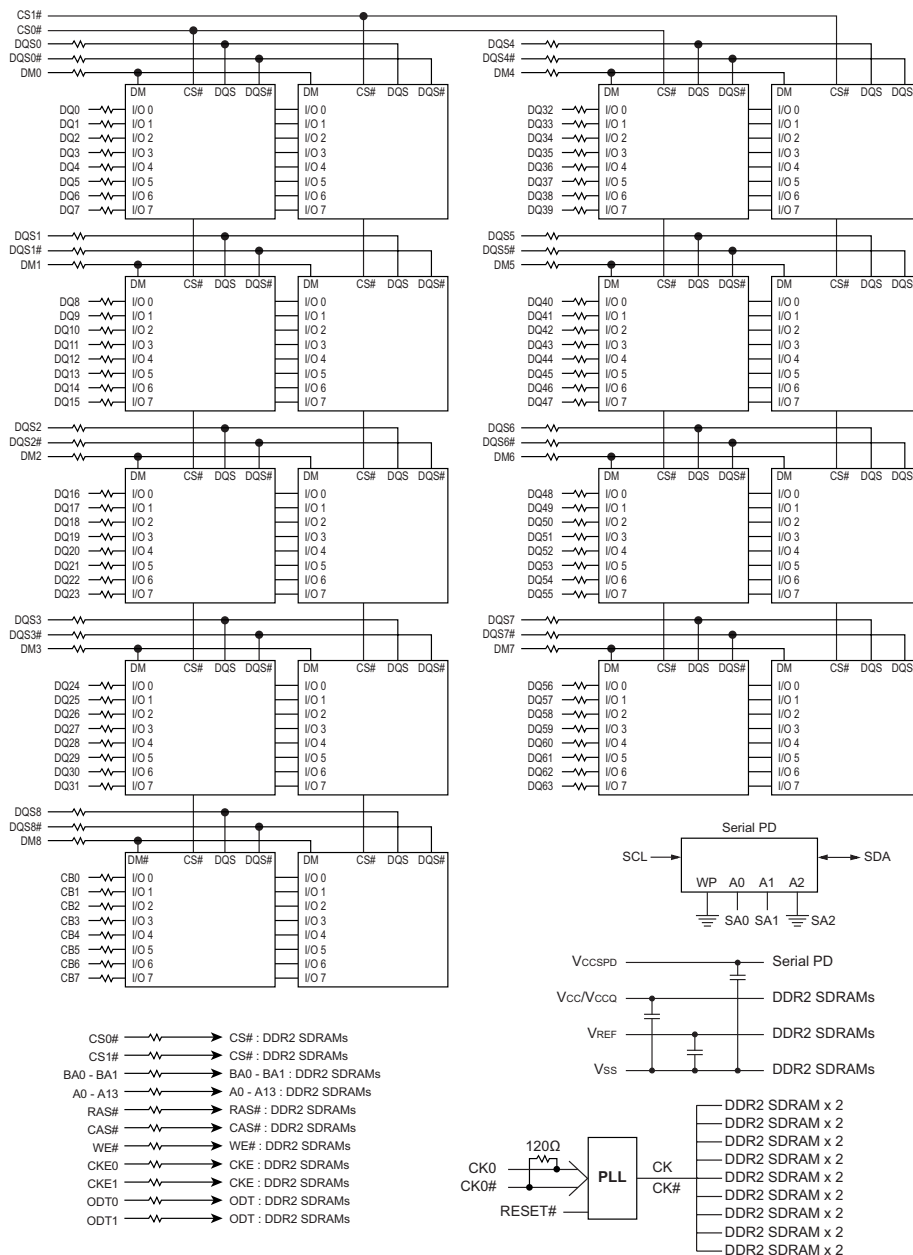
| Pin No. | Symbol | Pin No. | Symbol | Pin No. | Symbol | Pin No. | Symbol |
|---------|------------------|---------|-----------------|---------|-----------------|---------|-----------------|
| 1 | V _{REF} | 51 | DQ18 | 101 | V _{CC} | 151 | V _{SS} |
| 2 | V _{SS} | 52 | V _{SS} | 102 | A6 | 152 | V _{SS} |
| 3 | DQ0 | 53 | DQ19 | 103 | A5 | 153 | DQS5# |
| 4 | DQ4 | 54 | DQ28 | 104 | A4 | 154 | DM5 |
| 5 | V _{SS} | 55 | V _{SS} | 105 | A3 | 155 | DQS5 |
| 6 | DQ5 | 56 | DQ29 | 106 | V _{CC} | 156 | V _{SS} |
| 7 | DQ1 | 57 | DQ24 | 107 | A2 | 157 | V _{SS} |
| 8 | V _{SS} | 58 | V _{SS} | 108 | A1 | 158 | DQ46 |
| 9 | DQS0# | 59 | DQ25 | 109 | V _{CC} | 159 | DQ42 |
| 10 | DM0 | 60 | DM3 | 110 | A0 | 160 | DQ47 |
| 11 | DQS0 | 61 | V _{SS} | 111 | A10/AP | 161 | DQ43 |
| 12 | V _{SS} | 62 | V _{SS} | 112 | BA1 | 162 | V _{SS} |
| 13 | V _{SS} | 63 | DQS3# | 113 | BA0 | 163 | V _{SS} |
| 14 | DQ6 | 64 | DQ30 | 114 | V _{CC} | 164 | DQ52 |
| 15 | DQ2 | 65 | DQS3 | 115 | RAS# | 165 | DQ48 |
| 16 | DQ7 | 66 | DQ31 | 116 | WE# | 166 | DQ53 |
| 17 | DQ3 | 67 | V _{SS} | 117 | V _{CC} | 167 | DQ49 |
| 18 | V _{SS} | 68 | V _{SS} | 118 | CS0# | 168 | V _{SS} |
| 19 | V _{SS} | 69 | DQ26 | 119 | CAS# | 169 | V _{SS} |
| 20 | DQ12 | 70 | CB4 | 120 | ODT0 | 170 | DM6 |
| 21 | DQ8 | 71 | DQ27 | 121 | CS1# | 171 | DQS6# |
| 22 | DQ13 | 72 | CB5 | 122 | A13 | 172 | V _{SS} |
| 23 | DQ9 | 73 | V _{SS} | 123 | V _{CC} | 173 | DQS6 |
| 24 | V _{SS} | 74 | V _{SS} | 124 | V _{CC} | 174 | DQ54 |
| 25 | V _{SS} | 75 | CB0 | 125 | ODT1 | 175 | V _{SS} |
| 26 | DM1 | 76 | DM8 | 126 | CK | 176 | DQ55 |
| 27 | DQS1# | 77 | CB1 | 127 | NC | 177 | DQ50 |
| 28 | V _{SS} | 78 | V _{SS} | 128 | CK# | 178 | V _{SS} |
| 29 | DQS1 | 79 | V _{SS} | 129 | DQ32 | 179 | DQ51 |
| 30 | DQ14 | 80 | CB6 | 130 | V _{SS} | 180 | DQ60 |
| 31 | V _{SS} | 81 | DQS8# | 131 | V _{SS} | 181 | V _{SS} |
| 32 | DQ15 | 82 | CB7 | 132 | DQ36 | 182 | DQ61 |
| 33 | DQ10 | 83 | DQS8 | 133 | DQ33 | 183 | DQ56 |
| 34 | V _{SS} | 84 | V _{SS} | 134 | DQ37 | 184 | V _{SS} |
| 35 | DQ11 | 85 | V _{SS} | 135 | DQS4# | 185 | DQ57 |
| 36 | DQ20 | 86 | CB2 | 136 | V _{SS} | 186 | DM7 |
| 37 | V _{SS} | 87 | CKE0 | 137 | DQS4 | 187 | V _{SS} |
| 38 | DQ21 | 88 | CB3 | 138 | DM4 | 188 | DQ62 |
| 39 | DQ16 | 89 | NC | 139 | V _{SS} | 189 | DQS7# |
| 40 | V _{SS} | 90 | V _{SS} | 140 | V _{SS} | 190 | V _{SS} |
| 41 | DQ17 | 91 | NC | 141 | DQ34 | 191 | DQS7 |
| 42 | RESET# | 92 | NC | 142 | DQ38 | 192 | DQ63 |
| 43 | V _{SS} | 93 | V _{CC} | 143 | DQ35 | 193 | DQ58 |
| 44 | DM2 | 94 | NC | 144 | DQ39 | 194 | SDA |
| 45 | DQS2# | 95 | A12 | 145 | V _{SS} | 195 | V _{SS} |
| 46 | V _{SS} | 96 | A11 | 146 | V _{SS} | 196 | SCL |
| 47 | DQS2 | 97 | A9 | 147 | DQ40 | 197 | DQ59 |
| 48 | DQ22 | 98 | V _{CC} | 148 | DQ44 | 198 | SA1 |
| 49 | V _{SS} | 99 | A7 | 149 | DQ41 | 199 | VCCSPD |
| 50 | DQ23 | 100 | A8 | 150 | DQ45 | 200 | SA0 |

PIN NAMES

| Pin Name | Function |
|--------------------|--------------------------------|
| A0-A13 | Address Inputs |
| BA0, BA1 | SDRAM Bank Address |
| DQ0-DQ63 | Data Input/Output |
| CB0-CB7 | Check Bits |
| DQS0-DQS8 | Data strobes |
| DQS0#-DQS8# | Data strobes complement |
| ODT0, ODT1 | On-die termination controls |
| CK, CK# | Clock inputs |
| CKE0, CKE1 | Clock enable inputs |
| CS0#, CS1# | Chip select inputs |
| RAS# | Row Address Strobe |
| CAS# | Column Address Strobe |
| WE# | Write Enable |
| RESET# | Register reset input |
| V _{CC} | Core Power |
| V _{SS} | Ground |
| SA0-SA1 | SPD address |
| SDA | Serial Data Input/Output |
| V _{REF} | Input/Output Reference Voltage |
| DM0-DM8 | Data-in mask |
| V _{CCSPD} | Serial EEPROM power supply |
| SCL | SPD Clock Input |
| NC | No connect |



FUNCTIONAL BLOCK DIAGRAM



NOTE: All resistor values are 22 ohms unless otherwise specified.

**DC OPERATING CONDITIONS**All voltages referenced to V_{SS}

| Parameter | Symbol | Min | Typical | Max | Unit | Notes |
|-------------------------|--------------------|------------------------|------------------------|------------------------|------|-------|
| Supply Voltage | V _{CC} | 1.7 | 1.8 | 1.9 | V | 3 |
| I/O Reference Voltage | V _{REF} | 0.49 x V _{CC} | 0.50 x V _{CC} | 0.51 x V _{CC} | V | 1 |
| I/O Termination Voltage | V _{TT} | V _{REF} -0.04 | V _{REF} | V _{REF} +0.04 | V | 2 |
| SPD Supply Voltage | V _{CCSPD} | 1.7 | - | 3.6 | V | |

Notes:

- 1 V_{REF} is expected to equal V_{CC}/2 of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed +/-1 percent of the DC value. Peak-to-peak AC noise on V_{REF} may not exceed +/-2 percent of V_{REF}. This measurement is to be taken at the nearest V_{REF} bypass capacitor.
- 2 V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.
- 3 V_{CCQ} of all IC's are tied to V_{CC}.

ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | | Min | Max | Units |
|------------------------------------|---|-----------------------------------|------|-----|-------|
| V _{CC} | Voltage on V _{CC} pin relative to V _{SS} | | -0.5 | 2.3 | V |
| V _{IN} , V _{OUT} | Voltage on any pin relative to V _{SS} | | -0.5 | 2.3 | V |
| I _L | Input leakage current; Any input 0V<V _{IN} <V _{CC} ; V _{REF} input 0V,V _{IN} ,0.95V; Other pins not under test = 0V | Command/Address, RAS#, CAS#, WE#, | -90 | 90 | μA |
| | | CS#, CKE | -45 | 45 | μA |
| | | CK, CK# | -10 | 10 | μA |
| | | DM | -10 | 10 | μA |
| I _{OZ} | Output leakage current; 0V<V _{IN} <V _{CC} ; DQs and ODT are disable | DQ, DQS, DQS# | -10 | 10 | μA |
| I _{VREF} | V _{REF} leakage current; V _{REF} = Valid V _{REF} level | | -36 | 36 | μA |

INPUT/OUTPUT CAPACITANCE

TA=25°C, f=100MHz

| Parameter | Symbol | Min | Max | Unit |
|--|------------------------------|-----|-----|------|
| Input capacitance (0A~A13, BA0~BA1, RAS#, CAS#, WE#) | C _{IN1} | 22 | 40 | pF |
| Input capacitance (CKE0, CKE1), (ODT0, ODT1) | C _{IN2} | 13 | 22 | pF |
| Input capacitance (CS0# - CS1#) | C _{IN3} | 13 | 22 | pF |
| Input capacitance (CK, CK#) | C _{IN4} | 6 | 7 | pF |
| Input capacitance (DM0~DM8), (DQS0~DQS8) | C _{IN5} (665) | 9 | 11 | pF |
| | C _{IN5} (534, 403) | 9 | 12 | pF |
| Input capacitance (DQ0~DQ63), (CB0~CB7) | C _{OUT1} (665) | 9 | 11 | pF |
| | C _{OUT1} (534, 403) | 9 | 12 | pF |

**OPERATING TEMPERATURE CONDITION**

| Parameter | Symbol | Rating | Units | Notes |
|------------------------------------|--------|-----------|-------|-------|
| Operating temperature (Commercial) | TOPER | 0° to 85° | °C | 1, 2 |

Notes:

1. Operating temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JEDEC JESD51.2
2. At 0°C - 85°C, operation temperature range, all DRAM specification will be supported.

INPUT DC LOGIC LEVELAll voltages referenced to V_{SS}

| Parameter | Symbol | Min | Max | Units |
|------------------------------|--------------|-------------------|-------------------|-------|
| Input High (Logic 1) Voltage | $V_{IH}(DC)$ | $V_{REF} + 0.125$ | $V_{CC} + 0.300$ | V |
| Input Low (Logic 0) Voltage | $V_{IL}(DC)$ | -0.300 | $V_{REF} - 0.125$ | V |

INPUT AC LOGIC LEVELAll voltages referenced to V_{SS}

| Parameter | Symbol | Min | Max | Unit |
|--|--------------|-------------------|-------------------|------|
| AC Input High (Logic 1) Voltage DDR2-400 & DDR2-533 | $V_{IH}(AC)$ | $V_{REF} + 0.250$ | - | V |
| AC Input High (Logic 1) Voltage DDR2-667 | $V_{IH}(AC)$ | $V_{REF} + 0.200$ | - | V |
| AC Input High (Logic 0) Voltage DDR2-400 & DDR2-533 | $V_{IL}(AC)$ | - | $V_{REF} - 0.250$ | V |
| AC Input High (Logic 0) Voltage DDR2-667 | $V_{IL}(AC)$ | - | $V_{REF} - 0.200$ | V |

DDR2 I_{cc} SPECIFICATIONS AND CONDITIONS

Includes DDR2 SDRAM components only

V_{CC} = +1.8V ± 0.1V

| Symbol | Proposed Conditions | 806 | 665 | 534 | 403 | Units |
|----------------------|--|---------------------------|-------|-------|-------|-------|
| I _{CC0} * | Operating one bank active-precharge current; t _{CK} = t _{CK} (I _{CC}), t _{RC} = t _{RC} (I _{CC}), t _{RAS} = t _{RASmin} (I _{CC}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING | TBD | 1,137 | 1,092 | 1,092 | mA |
| I _{CC1} * | Operating one bank active-read-precharge current; I _{OUT} = 0mA; BL = 4, CL = CL(I _{CC}), AL = 0; t _{CK} = t _{CK} (I _{CC}), t _{RC} = t _{RC} (I _{CC}), t _{RAS} = t _{RASmin} (I _{CC}), t _{RCD} = t _{RCD} (I _{CC}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as I _{CC4W} | TBD | 1,272 | 1,227 | 1,227 | mA |
| I _{CC2P} * | Precharge power-down current; All banks idle; t _{CK} = t _{CK} (I _{CC}); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING | TBD | 444 | 444 | 444 | mA |
| I _{CC2Q} ** | Precharge quiet standby current; All banks idle; t _{CK} = t _{CK} (I _{CC}); CKE is HIGH, CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING | TBD | 930 | 840 | 840 | mA |
| I _{CC2N} ** | Precharge standby current; All banks idle; t _{CK} = t _{CK} (I _{CC}); CKE is HIGH, CS# is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING | TBD | 1,020 | 930 | 930 | mA |
| I _{CC3P} ** | Active power-down current; All banks open; t _{CK} = t _{CK} (I _{CC}); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING | Fast PDN Exit MRS(12) = 0 | TBD | 840 | 840 | mA |
| | | Slow PDN Exit MRS(12) = 1 | TBD | 516 | 516 | mA |
| I _{CC3N} ** | Active standby current; All banks open; t _{CK} = t _{CK} (I _{CC}), t _{RAS} = t _{RASmax} (I _{CC}), t _{RP} = t _{RP} (I _{CC}); CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING | TBD | 1,290 | 1,200 | 1,200 | mA |
| I _{CC4W} * | Operating burst write current; All banks open, Continuous burst writes; BL = 4, CL = CL(I _{CC}), AL = 0; t _{CK} = t _{CK} (I _{CC}), t _{RAS} = t _{RASmax} (I _{CC}), t _{RP} = t _{RP} (I _{CC}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING | TBD | 1,632 | 1,452 | 1,362 | mA |
| I _{CC4R} * | Operating burst read current; All banks open, Continuous burst reads, I _{OUT} = 0mA; BL = 4, CL = CL(I _{CC}), AL = 0; t _{CK} = t _{CK} (I _{CC}), t _{RAS} = t _{RASmax} (I _{CC}), t _{RP} = t _{RP} (I _{CC}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as I _{CC4W} | TBD | 1,677 | 1,497 | 1,362 | mA |
| I _{CC5B} ** | Burst auto refresh current; t _{CK} = t _{CK} (I _{CC}); Refresh command at every t _{REF} (I _{CC}) interval; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING | TBD | 3,000 | 2,820 | 2,820 | mA |
| I _{CC6} ** | Self refresh current; CK and CK# at 0V; CKE 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING | Normal | TBD | 144 | 144 | mA |
| I _{CC7} * | Operating bank interleave read current; All bank interleaving reads, I _{OUT} = 0mA; BL = 4, CL = CL(I _{CC}), AL = t _{RCD} (I _{CC})-1*t _{CK} (I _{CC}); t _{CK} = t _{CK} (I _{CC}), t _{RC} = t _{RC} (I _{CC}), t _{RRD} = t _{RRD} (I _{CC}), t _{RCD} = 1*t _{CK} (I _{CC}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data bus inputs are SWITCHING. | TBD | 2,352 | 2,352 | 2,352 | mA |

I_{CC} specification is based on **SAMSUNG** components. Other DRAM manufactures specification may be different.

Note:

* Value calculated as one module rank in this operating condition, and all other module ranks in I_{CC2P} (CKE LOW) mode.

** Value calculated reflects all module ranks in this operating condition.



AC TIMING PARAMETERS & SPECIFICATIONS

V_{CC} = +1.8V ± 0.1V

| AC CHARACTERISTICS | | | | 806 | | 665 | | 534 | | 403 | | |
|--------------------|--|--------|---------------------|-----|-----|---|-----------------------|---|-----------------------|---|-----------------------|-----------------|
| PARAMETER | | | SYMBOL | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | UNIT |
| Clock | Clock cycle time | CL = 6 | t _{CK} (6) | TBD | TBD | | | | | | | ps |
| | | CL = 5 | t _{CK} (5) | TBD | TBD | 3,000 | 8,000 | | | | | ps |
| | | CL = 4 | t _{CK} (4) | TBD | TBD | 3,750 | 8,000 | 3,750 | 8,000 | 5,000 | 8,000 | ps |
| | | CL = 3 | t _{CK} (3) | TBD | TBD | 5,000 | 8,000 | 5,000 | 8,000 | 5,000 | 8,000 | ps |
| | CK high-level width | | t _{CH} | TBD | TBD | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | t _{CK} |
| | CK low-level width | | t _{CL} | TBD | TBD | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | t _{CK} |
| | Half clock period | | t _{HP} | TBD | TBD | MIN(t _{CH} , t _{CL}) | | MIN(t _{CH} , t _{CL}) | | MIN(t _{CH} , t _{CL}) | | ps |
| | Clock jitter | | t _{J1T} | TBD | TBD | -125 | 125 | -125 | 125 | -125 | 125 | ps |
| Data | DQ output access time from CK/CK# | | t _{AC} | TBD | TBD | -450 | +450 | -500 | +500 | -600 | +600 | ps |
| | Data-out high-impedance window from CK/CK# | | t _{HZ} | TBD | TBD | | t _{AC} (MAX) | | t _{AC} (MAX) | | t _{AC} (MAX) | ps |
| | Data-out low-impedance window from CK/CK# | | t _{LZ} | TBD | TBD | t _{AC} (MIN) | t _{AC} (MAX) | t _{AC} (MIN) | t _{AC} (MAX) | t _{AC} (MIN) | t _{AC} (MAX) | ps |
| | DQ and DM input setup time relative to DQS | | t _{DS} | TBD | TBD | 100 | | 100 | | 150 | | |
| | DQ and DM input hold time relative to DQS | | t _{DH} | TBD | TBD | 225 | | 225 | | 275 | | |
| | DQ and DM input pulse width (for each input) | | t _{OLPW} | TBD | TBD | 0.35 | | 0.35 | | 0.35 | | t _{CK} |
| | Data hold skew factor | | t _{QHS} | TBD | TBD | | 340 | | 400 | | 450 | ps |
| | DQ...DQS hold, DQS to first DQ to go nonvalid, per access | | t _{QH} | TBD | TBD | t _{HP} - t _{QHS} | | t _{HP} - t _{QHS} | | t _{HP} - t _{QHS} | | ps |
| | Data valid output window (DVW) | | t _{DVW} | TBD | TBD | t _{QH} - t _{DQSQ} | | t _{QH} - t _{DQSQ} | | t _{QH} - t _{DQSQ} | | ns |
| Data Strobe | DQS input high pulse width | | t _{DQSH} | TBD | TBD | 0.35 | | 0.35 | | 0.35 | | t _{CK} |
| | DQS input low pulse width | | t _{DQSL} | TBD | TBD | 0.35 | | 0.35 | | 0.35 | | t _{CK} |
| | DQS output access time from CK/CK# | | t _{DQSCK} | TBD | TBD | -400 | +400 | -450 | +450 | -500 | +500 | ps |
| | DQS falling edge to CK rising ... setup time | | t _{DSS} | TBD | TBD | 0.2 | | 0.2 | | 0.2 | | t _{CK} |
| | DQS falling edge from CK rising ... hold time | | t _{DSH} | TBD | TBD | 0.2 | | 0.2 | | 0.2 | | t _{CK} |
| | DQS...DQ skew, DQS to last DQ valid, per group, per access | | t _{DQSQ} | TBD | TBD | | 240 | | 300 | | 350 | ps |
| | DQS read preamble | | t _{RPRE} | TBD | TBD | 0.9 | 1.1 | 0.9 | 1.1 | 0.9 | 1.1 | t _{CK} |
| | DQS read postamble | | t _{RPST} | TBD | TBD | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | t _{CK} |
| | DQS write preamble setup time | | t _{WPRES} | TBD | TBD | 0 | | 0 | | 0 | | ps |
| | DQS write preamble | | t _{WPRE} | TBD | TBD | 0.35 | | 0.35 | | 0.35 | | t _{CK} |
| | DQS write postamble | | t _{WPST} | TBD | TBD | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | t _{CK} |
| | Write command to first DQS latching transition | | t _{DQSS} | TBD | TBD | WL- 0.25 | WL+ 0.25 | WL- 0.25 | WL+ 0.25 | WL- 0.25 | WL+ 0.25 | t _{CK} |
| | Address and control input pulse width for each input | | t _{IPW} | TBD | TBD | 0.6 | | 0.6 | | 0.6 | | t _{CK} |
| | Address and control input setup time | | t _{IS} | TBD | TBD | 200 | | 250 | | 250 | | ps |
| | Address and control input hold time | | t _{IH} | TBD | TBD | 275 | | 375 | | 475 | | ps |
| | Address and control input hold time | | t _{CCD} | TBD | TBD | 2 | | 2 | | 2 | | t _{CK} |

* AC specification is based on **SAMSUNG** components. Other DRAM manufactures specification may be different.

Continued on next page



AC TIMING PARAMETERS & SPECIFICATIONS (cont'd)

V_{CC} = +1.8V ± 0.1V

| AC CHARACTERISTICS | | | 806 | | 665 | | 534 | | 403 | | |
|---------------------|--|--------------------|-----|-----|---|---|---|---|---|---|-----------------|
| PARAMETER | | SYMBOL | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | UNIT |
| Command and Address | ACTIVE to ACTIVE (same bank) command | t _{RC} | TBD | TBD | 55 | | 55 | | 55 | | ns |
| | ACTIVE bank a to ACTIVE bank b command | t _{RRD} | TBD | TBD | 7.5 | | 7.5 | | 7.5 | | ns |
| | ACTIVE to READ or WRITE delay | t _{RCD} | TBD | TBD | 15 | | 15 | | 15 | | ns |
| | Four Bank Activate period | t _{FAW} | TBD | TBD | 37.5 | 37.5 | 37.5 | 37.5 | 37.5 | 37.5 | ns |
| | ACTIVE to PRECHARGE command | t _{RAS} | TBD | TBD | 45 | 70,000 | 45 | 70,000 | 45 | 70,000 | ns |
| | Internal READ to precharge command delay | t _{RTP} | TBD | TBD | 7.5 | | 7.5 | | 7.5 | | ns |
| | Write recovery time | t _{WR} | TBD | TBD | 15 | | 15 | | 15 | | ns |
| | Auto precharge write recovery + precharge time | t _{DAL} | TBD | TBD | t _{WR} + t _{RP} | | t _{WR} + t _{RP} | | t _{WR} + t _{RP} | | ns |
| | Internal WRITE to READ command delay | t _{WTR} | TBD | TBD | 7.5 | | 7.5 | | 10 | | ns |
| | PRECHARGE command period | t _{RP} | TBD | TBD | 15 | | 15 | | 15 | | ns |
| | PRECHARGE ALL command period | t _{RPA} | TBD | TBD | t _{RP} + t _{CK} | | t _{RP} + t _{CK} | | t _{RP} + t _{CK} | | ns |
| | LOAD MODE command cycle time | t _{MRD} | TBD | TBD | 2 | | 2 | | 2 | | t _{CK} |
| | CKE low to CK,CK# uncertainty | t _{DELAY} | TBD | TBD | t _{IS} + t _{CK} + t _{IH} | | t _{IS} + t _{CK} + t _{IH} | | t _{IS} + t _{CK} + t _{IH} | | ns |
| Self Refresh | REFRESH to Active of Refresh to Refresh command interfal | t _{RFC} | TBD | TBD | 105 | 70,000 | 105 | 70,000 | 105 | 70,000 | ns |
| | Average periodic refresh interval | t _{REFI} | TBD | TBD | | 7.8 | | 7.8 | | 7.8 | μs |
| | Exit self refresh to non-READ command | t _{XSNR} | TBD | TBD | t _{RFC} (MIN) + 10 | | t _{RFC} (MIN) + 10 | | t _{RFC} (MIN) + 10 | | ns |
| | Exit self refresh to READ command | t _{XSRD} | TBD | TBD | 200 | | 200 | | 200 | | t _{CK} |
| | Exit self refresh timing reference | t _{ISXR} | TBD | TBD | t _{IS} | | t _{IS} | | t _{IS} | | ps |
| ODT | ODT turn-on delay | t _{AOND} | TBD | TBD | 2 | 2 | 2 | 2 | 2 | 2 | t _{CK} |
| | ODT turn-on | t _{AON} | TBD | TBD | t _{tAC} (MIN) | t _{tAC} (MAX) + 1000 | t _{tAC} (MIN) | t _{tAC} (MAX) + 1000 | t _{tAC} (MIN) | t _{tAC} (MAX) + 1000 | ps |
| | ODT turn-off delay | t _{AOFD} | TBD | TBD | 2.5 | 2.5 | 2.5 | 2.5 | 2.5 | 2.5 | t _{CK} |
| | ODT turn-off | t _{AOF} | TBD | TBD | t _{tAC} (MIN) | t _{tAC} (MAX) + 600 | t _{tAC} (MIN) | t _{tAC} (MAX) + 600 | t _{tAC} (MIN) | t _{tAC} (MAX) + 600 | ps |
| | ODT turn-on (power-down mode) | t _{AONPD} | TBD | TBD | t _{tAC} (MIN) + 2000 | 2 x t _{CK} + t _{tAC} (MAX) + 1000 | t _{tAC} (MIN) + 2000 | 2 x t _{CK} + t _{tAC} (MAX) + 1000 | t _{tAC} (MIN) + 2000 | 2 x t _{CK} + t _{tAC} (MAX) + 1000 | ps |
| | ODT turn-off (power-down mode) | t _{AOFPD} | TBD | TBD | t _{tAC} (MIN) + 2000 | 2.5 x t _{CK} + t _{tAC} (MAX) + 1000 | t _{tAC} (MIN) + 2000 | 2.5 x t _{CK} + t _{tAC} (MAX) + 1000 | t _{tAC} (MIN) + 2000 | 2.5 x t _{CK} + t _{tAC} (MAX) + 1000 | ps |
| | ODT to power-down entry latency | t _{ANPD} | TBD | TBD | 3 | | 3 | | 3 | | t _{CK} |
| | ODT power-down exit latency | t _{AXPD} | TBD | TBD | 8 | | 8 | | 8 | | t _{CK} |
| | | | | | | | | | | | |
| Power-Down | Exit active power-down to READ command, MR[bit12=0] | t _{XARD} | TBD | TBD | 2 | | 2 | | 2 | | t _{CK} |
| | Exit active power-down to READ command, MR[bit12=1] | t _{XARDS} | TBD | TBD | 7 - AL | | 6 - AL | | 6 - AL | | t _{CK} |
| | A Exit precharge power-down to any non-READ command. | t _{XP} | TBD | TBD | 2 | | 2 | | 2 | | t _{CK} |
| | CKE minimum high/low time | t _{CKE} | TBD | TBD | 3 | | 3 | | 3 | | t _{CK} |

* AC specification is based on **SAMSUNG** components. Other DRAM manufactures specification may be different.

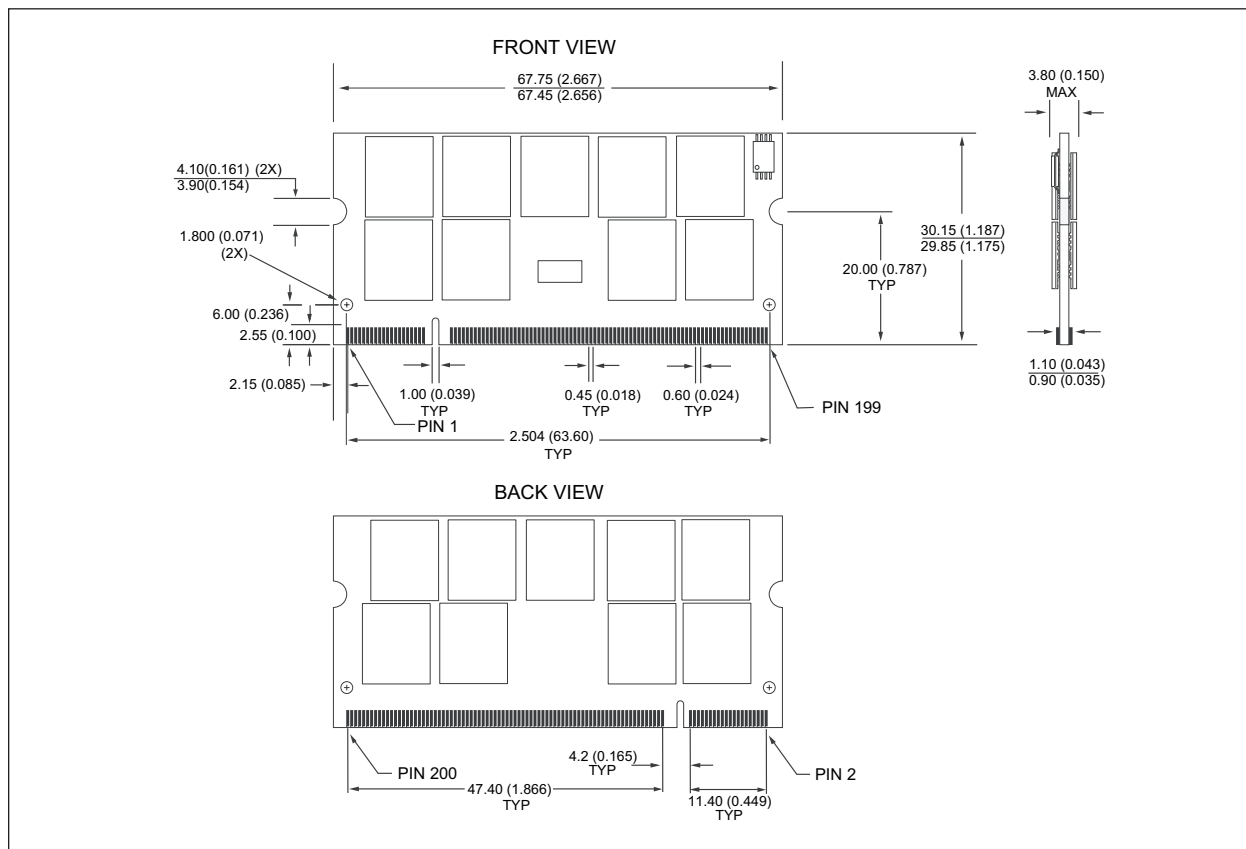
**ORDERING INFORMATION FOR PD4**

| Part Number | Speed/Data Rate | CAS Latency | t _{RCD} | t _{RP} | Height* |
|---------------------------|-----------------|-------------|------------------|-----------------|--------------------|
| WV3HG264M72EEU806PD4xxG** | 400MHz/800Mb/s | 6 | 6 | 6 | 30.00mm (1.81")TYP |
| WV3HG264M72EEU665PD4xxG** | 333MHz/667Mb/s | 5 | 5 | 5 | 30.00mm (1.81")TYP |
| WV3HG264M72EEU534PD4xxG | 266MHz/533Mb/s | 4 | 4 | 4 | 30.00mm (1.81")TYP |
| WV3HG264M72EEU403PD4xxG | 200MHz/400Mb/s | 3 | 3 | 3 | 30.00mm (1.81")TYP |

** Consult factory for availability

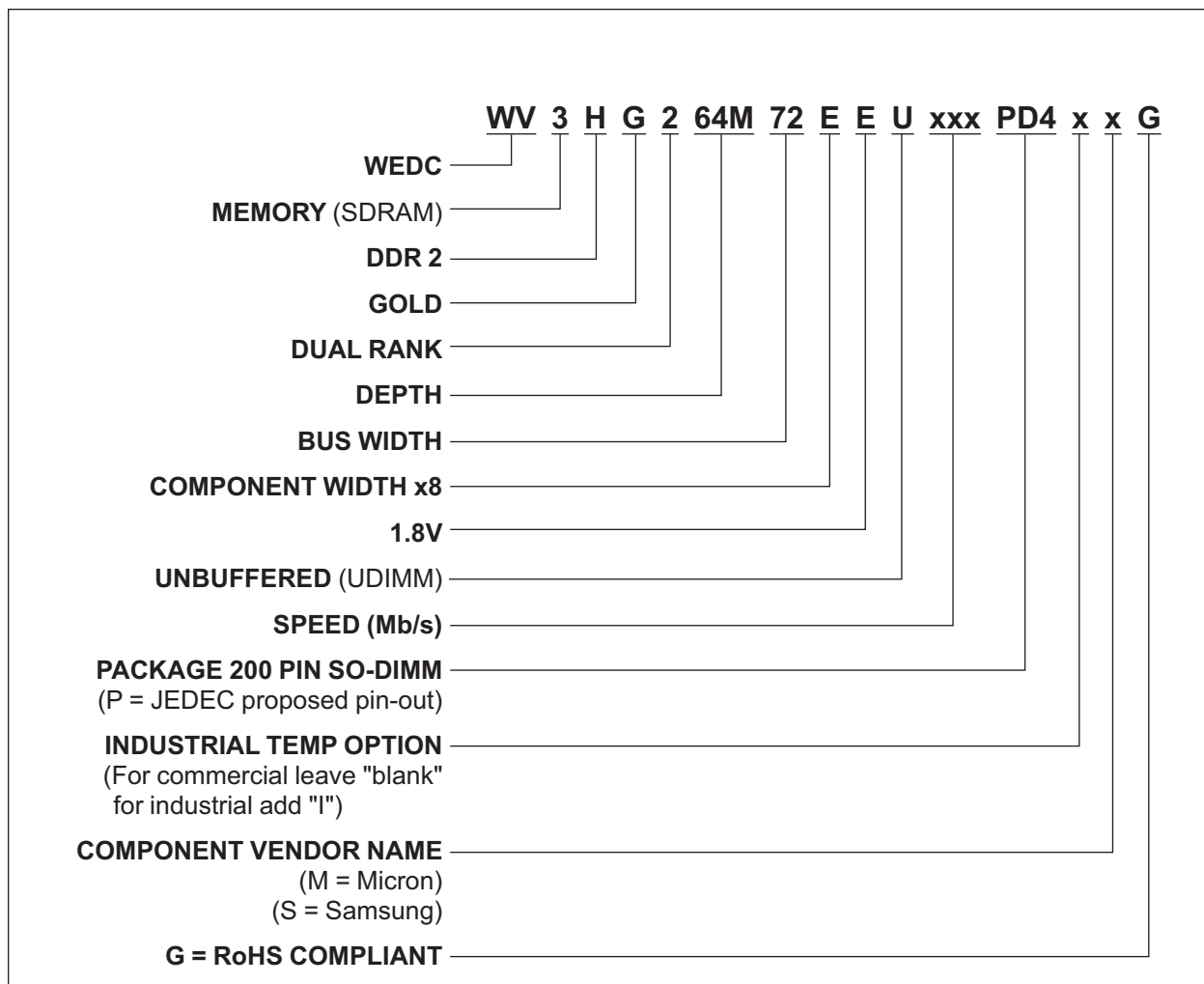
NOTES:

- RoHS product. ("G" = RoHS Compliant)
- Vendor specific part numbers are used to provide memory component source control. The place holder for this is shown as a lower case "x" in the part numbers above and is to be replaced with respective vendors code. Consult factory for qualified sourcing options.
(M = Micron, S = Samsung & consult factory for others)

PACKAGE DIMENSIONS FOR PD4

* ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)

Tolerances: ±0.13 (0.005) unless otherwise specified

**PART NUMBERING GUIDE**

**Document Title**

1GB – 2x64Mx72 DDR2 SDRAM UNBUFFERED, SO-DIMM w/PLL

DRAM DIE OPTIONS:

- SAMSUNG: C-Die, will move to E-Die Q2'06
- MICRON: U37Y: B-Die

Revision History

| Rev # | History | Release Date | Status |
|-------|---|--------------|----------|
| Rev 0 | Created | August 2005 | Concept |
| Rev 1 | 1.0 Updated Icc, CAP & AC specs 1.1 Added industrial temp option to part numbering guide 1.2 Changed from concept to advanced | March 2006 | Advanced |
| Rev 2 | 2.0 Update Icc, CAP & AC specs 2.1 Added "P" for JEDEC proposed pin-out 2.2 Added die Rev info | April 2006 | Advanced |