



512MB – 64Mx72 DDR2 SDRAM REGISTERED, w/PLL, Mini-DIMM

FEATURES

- 244-pin, dual in-line memory module (Mini-DIMM)
- Fast data transfer rates: PC2-6400*, PC2-5300*, PC2-4200 and PC2-3200
- Utilizes 800, 667, 533 and 400 Mb/s DDR2 SDRAM components
- $V_{CC} = V_{CCQ} = 1.8V \pm 0.1V$
- $V_{CCSPD} = 1.7V$ to 3.6V
- Differential data strobe (DQS, DQS#) option
- Four-bit prefetch architecture
- Programmable CAS# latency (CL): 3, 4, 5 and 6
- On-die termination (ODT)
- Serial Presence Detect (SPD) with EEPROM
- Auto and Self Refresh Capability (64ms: 8,192 cycle refresh)
- Gold (Au) edge contacts
- RoHS compliant
- Single Rank
- Package option
 - 244 Pin Mini-DIMM
 - PCB – 30.00mm (1.181") TYP

DESCRIPTION

The WV3HG64M72EER is a 64Mx72 Double Data Rate DDR2 SDRAM high density module. This memory module consists of nine 64Mx8 bit with 4 banks DDR2 Synchronous DRAMs in FBGA packages, mounted on a 244-pin DIMM FR4 substrate.

* This product is under development, is not qualified or characterized and is subject to change without notice.

NOTE: Consult factory for availability of:

- Vendor source control options
- Industrial temperature option

OPERATING FREQUENCIES

	PC2-3200	PC2-4200	PC2-5300*	PC2-6400*
Clock Speed	200MHz	266MHz	333MHz	400MHz
CL-tRCD-tRP	3-3-3	4-4-4	5-5-5	6-6-6

*Consult factory for availability.



PIN CONFIGURATION

Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol
1	VREF	62	A4	123	Vss	184	Vccq
2	Vss	63	Vccq	124	DQ4	185	A3
3	DQ0	64	A2	125	DQ5	186	A1
4	DQ1	65	Vcc	126	Vss	187	Vcc
5	Vss	66	Vss	127	DM0	188	CK0
6	DQS0#	67	Vss	128	NC	189	CK0#
7	DQS0	68	NC	129	Vss	190	Vcc
8	Vss	69	Vcc	130	DQ6	191	A0
9	DQ2	70	A10/AP	131	DQ7	192	BA1
10	DQ3	71	BA0	132	Vss	193	Vcc
11	Vss	72	Vcc	133	DQ12	194	RAS#
12	DQ8	73	WE#	134	DQ13	195	Vccq
13	DQ9	74	Vccq	135	Vss	196	CS0#
14	Vss	75	CAS#	136	DM1	197	Vccq
15	DQS1#	76	Vccq	137	NC	198	ODT0
16	DQS1	77	NC	138	Vss	199	A13
17	Vss	78	NC	139	NC	200	Vcc
18	RESET#	79	Vccq	140	NC	201	NC
19	NC	80	NC	141	Vss	202	Vss
20	Vss	81	Vss	142	DQ14	203	DQ36
21	DQ10	82	DQ32	143	DQ15	204	DQ37
22	DQ11	83	DQ33	144	Vss	205	Vss
23	Vss	84	Vss	145	DQ20	206	DM4
24	DQ16	85	DQS4#	146	DQ21	207	NC
25	DQ17	86	DQS4	147	Vss	208	Vss
26	Vss	87	Vss	148	DM2	209	DQ38
27	DQS2#	88	DQ34	149	NC	210	DQ39
28	DQS2	89	DQ35	150	Vss	211	Vss
29	Vss	90	Vss	151	DQ22	212	DQ44
30	DQ18	91	DQ40	152	DQ23	213	DQ45
31	DQ19	92	DQ41	153	Vss	214	Vss
32	Vss	93	Vss	154	DQ28	215	DM5
33	DQ24	94	DQS5#	155	DQ29	216	NC
34	DQ25	95	DQS5	156	Vss	217	Vss
35	Vss	96	Vss	157	DM3	218	DQ46
36	DQS3#	97	DQ42	158	NC	219	DQ47
37	DQS3	98	DQ43	159	Vss	220	Vss
38	Vss	99	Vss	160	DQ30	221	DQ52
39	DQ26	100	DQ48	161	DQ31	222	DQ53
40	DQ27	101	DQ49	162	Vss	223	Vss
41	Vss	102	Vss	163	CB4	224	NC
42	CB0	103	SA2	164	CB5	225	NC
43	CB1	104	NC	165	Vss	226	Vss
44	Vss	105	Vss	166	DM8	227	DM6
45	DQS8#	106	DQS6#	167	NC	228	NC
46	DQS8	107	DQS6	168	Vss	229	Vss
47	Vss	108	Vss	169	CB6	230	DQ54
48	CB2	109	DQ50	170	CB7	231	DQ55
49	CB3	110	DQ51	171	Vss	232	Vss
50	Vss	111	Vss	172	NC	233	DQ60
51	NC	112	DQ56	173	Vccq	234	DQ61
52	Vccq	113	DQ57	174	*CKE1	235	Vss
53	CKE0	114	Vss	175	Vcc	236	DM7
54	Vcc	115	DQS7#	176	NC	237	NC
55	NC	116	DQS7	177	NC	238	Vss
56	NC	117	Vss	178	Vccq	239	DQ62
57	Vccq	118	DQ58	179	A12	240	DQ63
58	A11	119	DQ59	180	A9	241	Vss
59	A7	120	Vss	181	Vcc	242	SDA
60	Vcc	121	SA0	182	A8	243	SCL
61	A5	122	SA1	183	A6	244	VccSPD

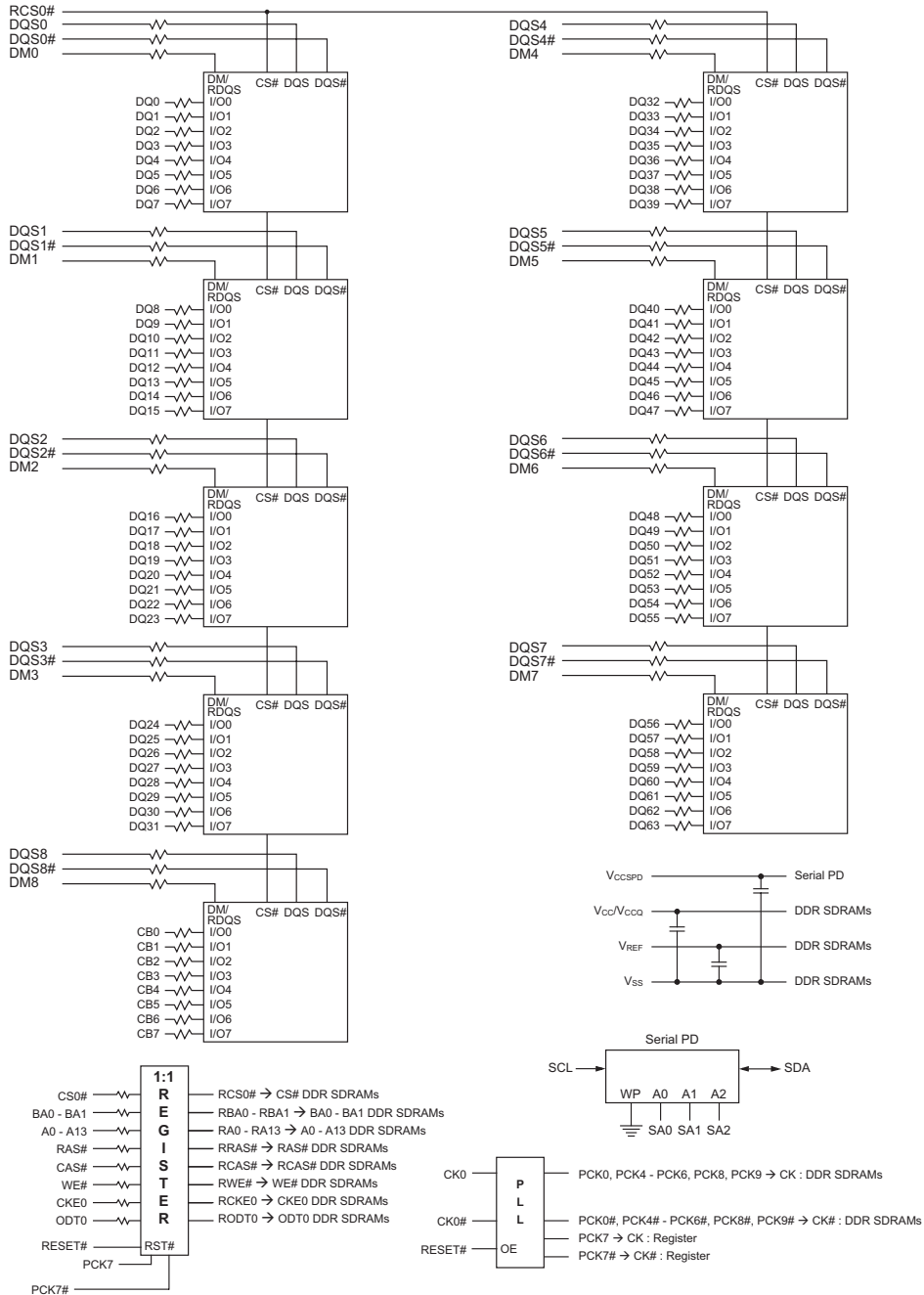
RESET (pin 18) is connected to both OE of the PLL and Reset# of the register .

PIN NAMES

Pin Name	Function
A0-A13	Address Inputs
BA0,BA1	SDRAM Bank Address
DQ0-DQ63	Data Input/Output
CB0-CB7	Check Bits
DQS0-DQS8	Data strobes
DQS0#-DQS8#	Data strobes complement
ODT0	On-die termination control
CK0,CK0#	Clock Inputs, positive line
CKE0	Clock Enables
CS0#	Chip Selects
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
RESET#	Register Reset Input
DM (0-8)	Data Masks
VCCSPD	SPD Power
Vcc	Core and I/O Power (1.8V)
Vccq	I/O Power (1.8V)
A10/AP	Address Input/Auto Precharge
Vss	Ground
SA0-SA2	SPD address
SDA	SPD Data Input/Output
SCL	Serial Presence Detect (SPD) Clock Input
NC	Spare pins, No connect
VREF	Input/Output Reference



FUNCTIONAL BLOCK DIAGRAM



NOTE: All resistor values are 22 ohms $\pm 5\%$ unless otherwise specified.



DC OPERATING CONDITIONS

All voltages referenced to V_{SS}

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Supply voltage	V _{CC}	1.7	1.8	1.9	V	1
I/O Supply voltage	V _{CCQ}	1.7	1.8	1.9	V	4
V _{CCL} Supply voltage	V _{CCL}	1.7	1.8	1.9	V	4
I/O Reference voltage	V _{REF}	0.49 x V _{CCQ}	0.50 x V _{CCQ}	0.51 x V _{CCQ}	V	2
I/O Termination voltage	V _{TT}	V _{REF} -0.04	V _{REF}	V _{REF} + 0.04	V	3

Notes:

- V_{CC} V_{CCQ} must track each other. V_{CCQ} must be less than or equal to V_{CC}.
- V_{REF} is expected to equal V_{CCQ}/2 of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed ±1 percent of the DC value. Peak-to-peak AC noise on V_{REF} may not exceed ±2 percent of V_{REF}. This measurement is to be taken at the nearest V_{REF} bypass capacitor.
- V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.
- V_{CCQ} tracks with V_{CC}; V_{CCL} track with V_{CC}.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		MIN	MAX	Unit
V _{CC}	Voltage on V _{CC} pin relative to V _{SS}		-1.0	2.3	V
V _{CCQ}	Voltage on V _{CCQ} pin relative to V _{SS}		-0.5	2.3	V
V _{CCL}	Voltage on V _{CCL} pin relative to V _{SS}		-0.5	2.3	V
V _{IN} , V _{OUT}	Voltage on any pin relative to V _{SS}		-0.5	2.3	V
T _{STG}	Storage temperature		-55	100	°C
T _{CASE}	Device operating temperature		0	85	°C
I _L	Input leakage current; Any input 0V<V _{IN} <V _{CC} ; V _{REF} input 0V<V _{IN} <0.95V; Other pins not under test = 0V	Command/Address, RAS#, CAS#, WE#, CS#, CKE	-5	5	μA
		CK, CK#	-10	10	μA
		DM	-5	5	μA
I _{OZ}	Output leakage current; 0V<V _{OUT} <V _{CCQ} ; DQs and ODT are disable	DQ, DQS, DQS#	-5	5	μA
I _{VREF}	V _{REF} leakage current; V _{REF} = Valid V _{REF} level		-18	18	μA

INPUT/OUTPUT CAPACITANCE

T_A=25 0 C, f=1 00MHz

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0 - A13, BA0 - BA1 ,RAS#,CAS#,WE#)	C _{IN1}	6.5	7.5	pF
Input capacitance (CKE0), (ODT0)	C _{IN2}	6.5	7.5	pF
Input capacitance (CS0#)	C _{IN3}	6.5	7.5	pF
Input capacitance (CK0, CK0#)	C _{IN4}	6	7	pF
Input capacitance (DM0 - DM8), (DQS0 - DQS8)	C _{IN5}	6.5	8	pF
Input capacitance (DQ0 - DQ63), (CB0 - CB7)	C _{OUT1}	6.5	8	pF

**OPERATING TEMPERATURE CONDITION**

Parameter	Symbol	Rating	Units	Notes
Operating temperature	T _{OPER}	0 to 85	°C	1, 2

Notes:

1. Operating temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JEDEC JESD51 .2
2. At 0 - 85°C, operation temperature range, all DRAM specification will be supported.

INPUT DC LOGIC LEVELAll voltages referenced to V_{SS}

Parameter	Symbol	Min	Max	Unit
Input High (Logic 1) Voltage	V _{IH} (DC)	V _{REF} + 0.1 25	V _{REF} + 0.300	V
Input Low (Logic 0) Voltage	V _{IL} (DC)	-0.300	V _{REF} - 0.125	V

INPUT AC LOGIC LEVELAll voltages referenced to V_{SS}

Parameter	Symbol	Min	Max	Unit
AC Input High (Logic 1) Voltage	V _{IH} (AC)	V _{REF} + 0.250	—	V
AC Input Low (Logic 0) Voltage DDR2-400 & DDR2-533 (DDR2-667 & DDR2-806) TBD	V _{IL} (AC)	—	V _{REF} - 0.250	V



DDR2 I_{CC} SPECIFICATIONS AND CONDITIONS

Includes DDR2 SDRAM components only; T_A = 0°C, V_{CC} = 1.9V

Symbol	Parameter	Condition	806	665	534	403	Unit	
I _{CC0} *	Operating one bank active-precharge;	t _{CK} = t _{CK(DD)} ; t _{RC} = t _{RC(I_{CC})} ; t _{RAS} = t _{RAS MIN(I_{CC})} ; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	TBD	TBD	1120	1120	mA	
I _{CC1} *	Operating one bank active-read-precharge;	I _{OUT} = 0mA; BL = 4; CL = CL(I _{CC}); t _{CK} = t _{CK(I_{CC})} ; t _{RC} = t _{RC(I_{CC})} ; t _{RAS} = t _{RAS MIN(I_{CC})} ; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING; Data pattern is same as I _{CC4W} .	TBD	TBD	1255	1255	mA	
I _{CC2P} **	Precharge power-down current;	All banks idle; t _{CK} = t _{CK(I_{CC})} ; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	TBD	TBD	472	472	mA	
I _{CC2Q} **	Precharge quite standby current;	All banks idle; t _{CK} = t _{CK(I_{CC})} ; CKE is HIGH; CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	TBD	TBD	670	670	mA	
I _{CC2N} **	Precharge standby current;	All banks idle; t _{CK} = t _{CK(I_{CC})} ; CKE is HIGH; CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are SWITCHING	TBD	TBD	715	715	mA	
I _{CC3P} **	Active power-down current;	All banks open; t _{CK} = t _{CK(I_{CC})} , CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast PDN Exit MRS(12) = 0	TBD	TBD	670	670	mA
			Slow PDN Exit MRS(12) = 1	TBD	TBD	508	508	mA
I _{CC3N} **	Active standby current;	All banks open; t _{CK} = t _{CK(I_{CC})} ; t _{RC} = t _{RC(I_{CC})} ; t _{RAS} = t _{RAS MIN(I_{CC})} ; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	TBD	TBD	850	850	mA	
I _{CC4W} *	Operating burst write current;	All banks open; Continuous burst writes; BL = 4; CL = CL(ICC); AL = 0; t _{CK} = t _{CK(I_{CC})} ; t _{RC} = t _{RC(I_{CC})} ; t _{RAS} = t _{RAS MIN(I_{CC})} ; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	TBD	TBD	1480	1390	mA	
I _{CC4R} *	Operating burst read current;	All banks open; Continuous burst reads; TOUT = 0mA; BL = 4; CL = CL(ICC); AL = 0; t _{CK} = t _{CK(I_{CC})} ; t _{RC} = t _{RC(I_{CC})} ; t _{RAS} = t _{RAS MIN(I_{CC})} ; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as I _{CC4W} .	TBD	TBD	1525	1390	mA	
I _{CC5} **	Burst auto refresh current;	t _{CK} = t _{CK(I_{CC})} ; Refresh command at every t _{RC(I_{CC})} interval; CKE is HIGH; CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	TBD	TBD	1660	1660	mA	
I _{CC6} **	Self refresh current;	CK and CK# at 0V; CKE < 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	Normal	TBD	TBD	472	472	mA
I _{CC7} *	Operating bank interleave read current;	All bank interleaving reads; IOUT = 0mA; BL = 4; CL = CL(ICC); AL = t _{RC(D)(I_{CC})} - 1*t _{CK(I_{CC})} ; t _{CK} = t _{CK(I_{CC})} ; t _{RC} = t _{RC(I_{CC})} ; t _{RRD} = t _{RRD MIN(I_{CC})} = 1*t _{CK(I_{CC})} ; CKE is HIGH; CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data bus inputs are SWITCHING	TBD	TBD	2380	2380	mA	

Notes:

I_{CC} specification is based on **SAMSUNG** components. Other DRAM manufacturers specification may be different.

* Value calculated as one module rank in this operating condition, and all other module ranks in I_{CC2P} (CKE LOW) mode.

** Value calculated reflects all module ranks in this operating condition.



AC TIMING PARAMETERS

0°C ≤ T_{case} < +70°C; V_{CCQ} = + 1.8V ± 0.1V, V_{CC} = +1.8V ± 0.1V

Parameter			Symbol	806		665		534		403		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
Clock	Clock cycle time	CL=6	t _{CK(6)}	TBD	TBD	TBD	TBD					ps
		CL=5	t _{CK(5)}	TBD	TBD	TBD	TBD					ps
		CL=4	t _{CK(4)}	TBD	TBD	TBD	TBD	3,750	8,000	5,000	8,000	ps
		CL=3	t _{CK(3)}	TBD	TBD	TBD	TBD	5,000	8,000	5,000	8,000	ps
	CK high-level width		t _{CH}	TBD	TBD	TBD	TBD	0.45	0.55	0.45	0.55	t _{CK}
	CK low-level width		t _{CL}	TBD	TBD	TBD	TBD	0.45	0.55	0.45	0.55	t _{CK}
	Half clock period		t _{HP}	TBD	TBD	TBD	TBD	MIN (t _{CH} , t _{CL})		MIN (t _{CH} , t _{CL})		ps
	Clock jitter		t _{JIT}	TBD	TBD	TBD	TBD	TBD		TBD		ps
Data	DQ output access time from CK/CK#		t _{AC}	TBD	TBD	TBD	TBD	-500	+500	-600	+600	ps
	Data-out high impedance window from CK/CK#		t _{HZ}	TBD	TBD	TBD	TBD		t _{AC(MAX)}		t _{AC(MAX)}	ps
	Data-out low-impedance window from CK/CK#		t _{LZ}	TBD	TBD	TBD	TBD	t _{AC(MN)}	t _{AC(MAX)}	t _{AC(MN)}	t _{AC(MAX)}	ps
	DQ and DM input setup time relative to DQS		t _{DS}	TBD	TBD	TBD	TBD	100		150		
	DQ and DM input hold time relative to DQS		t _{QH}	TBD	TBD	TBD	TBD	225		275		
	DQ and DM input pulse width (for each input)		t _{DIPW}	TBD	TBD	TBD	TBD	0.35		0.35		t _{CK}
	Data hold skew factor		t _{QHS}	TBD	TBD	TBD	TBD		400		450	ps
	DQ-DQS hold, DQS to first DQ to go nonvalid, per access		t _{HQ}	TBD	TBD	TBD	TBD	t _{HP} - t _{QHS}		t _{HP} - t _{QHS}		ps
	Data valid output window (DVW)		t _{DVW}	TBD	TBD	TBD	TBD	t _{QH} - t _{DQSQ}		t _{QH} - t _{DQSQ}		ns
Data Strobe	DQS input high pulse width		t _{DQSH}	TBD	TBD	TBD	TBD	0.35		0.35		t _{CK}
	DQS input low pulse width		t _{DQSL}	TBD	TBD	TBD	TBD	0.35		0.35		t _{CK}
	DQS output access time from CK/CK#		t _{DQSCK}	TBD	TBD	TBD	TBD	-450	+450	-500	+500	Ps
	DQS falling edge to CK rising - setup time		t _{DSS}	TBD	TBD	TBD	TBD	0.2		0.2		t _{CK}
	DQS falling edge from CK rising - hold time		t _{DSH}	TBD	TBD	TBD	TBD	0.2		0.2		t _{CK}
	O DQS-DQ skew, DOS to last DQ valid, per group, per access		t _{DQSQ}	TBD	TBD	TBD	TBD		300		350	ps
	DQS read preamble		t _{RPRE}	TBD	TBD	TBD	TBD	0.9	1.1	0.9	1.1	t _{CK}
	DQS read postamble		t _{RPST}	TBD	TBD	TBD	TBD	0.4	0.6	0.4	0.6	t _{CK}
	DQS write preamble setup time		t _{WPRES}	TBD	TBD	TBD	TBD	0		0		ps
	DQS write preamble		t _{WPRE}	TBD	TBD	TBD	TBD	0.35		0.35		t _{CK}
	DQS write postamble		t _{WPST}	TBD	TBD	TBD	TBD	0.4	0.6	0.4	0.6	t _{CK}
	Write command to first DQS latching transition		t _{DQSS}	TBD	TBD	TBD	TBD	WL-0.25	WL+0.25	WL-0.25	WL+0.25	t _{CK}

AC specification is based on **SAMSUNG** components. Other DRAM manufacturers specification may be different.

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AC TIMING PARAMETERS (continued)

0°C ≤ T_{case} < +70°C; V_{CCQ} = + 1.8V ± 0.1V, V_{CC} = +1.8V ± 0.1V

	Parameter	Symbol	806		665		534		403		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Command and Address	Address and control input pulse width for each input	t _{IPW}	TBD	TBD	TBD	TBD	0.6		0.6		t _{CK}
	Address and control input setup time	t _{IS}	TBD	TBD	TBD	TBD	250		250		ps
	Address and control input hold time	t _{IH}	TBD	TBD	TBD	TBD	375		475		ps
	CAS# to CAS# command delay	t _{CCD}	TBD	TBD	TBD	TBD	2		2		ps
	ACTIVE to ACTIVE (same bank) command	t _{RC}	TBD	TBD	TBD	TBD	60		65		ns
	ACTIVE bank a to ACTIVE bank b command	t _{RRD}	TBD	TBD	TBD	TBD	7.5		7.5		ns
	ACTIVE to READ or WRITE delay	t _{RCD}	TBD	TBD	TBD	TBD	15		15		ns
	Four Bank Activate period	t _{FAW}	TBD	TBD	TBD	TBD	37.5	37.5	37.5	37.5	ns
	ACTIVE to PRECHARGE command	t _{RAS}	TBD	TBD	TBD	TBD	45	70,000	45	70,000	ns
	Internal READ to precharge command delay	t _{RTP}	TBD	TBD	TBD	TBD	7.5		7.5		ns
	Write recovery time	t _{WR}	TBD	TBD	TBD	TBD	15		15		ns
	Auto precharge write recovery + precharge time	t _{DAL}	TBD	TBD	TBD	TBD	t _{WR} + t _{RP}		t _{WR} + t _{RP}		ns
	Internal WRITE to READ command delay	t _{WTR}	TBD	TBD	TBD	TBD	7.5		10		ns
	PRECHARGE command period	t _{RP}	TBD	TBD	TBD	TBD	15		15		ns
	PRECHARGE ALL command period	t _{RPA}	TBD	TBD	TBD	TBD	t _{RP} + t _{CK}		t _{RP} + t _{CK}		ns
	LOAD MODE command cycle time	t _{MRD}	TBD	TBD	TBD	TBD	2		2		t _{CK}
	CKE low to CK, CK# uncertainty	t _{DELAY}	TBD	TBD	TBD	TBD	4.375		4.375		ns
Self Refresh	REFRESH to Active or Refresh to Refresh command interval	t _{RFC}	TBD	TBD	TBD	TBD	127.5	70,000	127.5	70,000	ns
	Average periodic refresh interval	t _{REFI}	TBD	TBD	TBD	TBD		7.8		7.8	ns
	Exit self refresh to non-READ command	t _{XS_{NR}}	TBD	TBD	TBD	TBD	t _{RPC(MIN)} + 10		t _{RFC(MIN)} + 10		ns
	Exit self refresh to READ	t _{XS_{RD}}	TBD	TBD	TBD	TBD	200		200		t _{CK}
	Exit self refresh timing reference	t _{IS_{XR}}	TBD	TBD	TBD	TBD	t _{IS}		t _{IS}		ps
ODT	ODT turn-on delay	t _{AOND}	TBD	TBD	TBD	TBD	2	2	2	2	t _{CK}
	ODT turn-on	t _{ACN}	TBD	TBD	TBD	TBD	t _{AC(MIN)}	t _{AC(MAX)} + 1000	t _{AC(MIN)}	t _{AC(MAX)} + 1000	ps
	ODT turn-off delay	t _{AOFD}	TBD	TBD	TBD	TBD	2.5	2.5	2.5	2.5	t _{CK}
	ODT turn-off	t _{AOF}	TBD	TBD	TBD	TBD	t _{AC(MIN)}	t _{AC(MAX)} + 600	t _{AC(MIN)}	t _{AC(MAX)} + 600	ps
	ODT turn-on (power-down mode)	t _{AONPD}	TBD	TBD	TBD	TBD	t _{AC(MIN)} + 2000	2 x t _{CK} + t _{AC(MAX)} + 1000 +1000	t _{AC(MIN)} + 2000	2 x t _{CK} + t _{AC(MAX)} + 1000	ps
	ODT turn-off (power-down mode)	t _{AOFPD}	TBD	TBD	TBD	TBD	t _{AC(MIN)} + 2000	2 x t _{CK} + t _{AC(MAX)} + 1000 +1000	t _{AC(MIN)} + 2000	2 x t _{CK} + t _{AC(MAX)} + 1000	ps
	ODT to power-down entry latency	t _{ANPD}	TBD	TBD	TBD	TBD	3		3		t _{CK}
	ODT power-down exit latency	t _{AXPD}					8		8		t _{CK}
Power-Down	Exit active power-down to READ command, MR[bit12=0]	t _{XARD}					2		2		t _{CK}
	Exit active power-down to READ command, MR[bit12=1]	t _{XARDS}					6-AL		6-AL		t _{CK}
	Exit precharge power-down to any non-READ command	t _{XP}					2		2		t _{CK}
	CKE minimum high/low time	t _{CKE}					3		3		t _{CK}

AC specification is based on **SAMSUNG** components. Other DRAM manufacturers specification may be different.



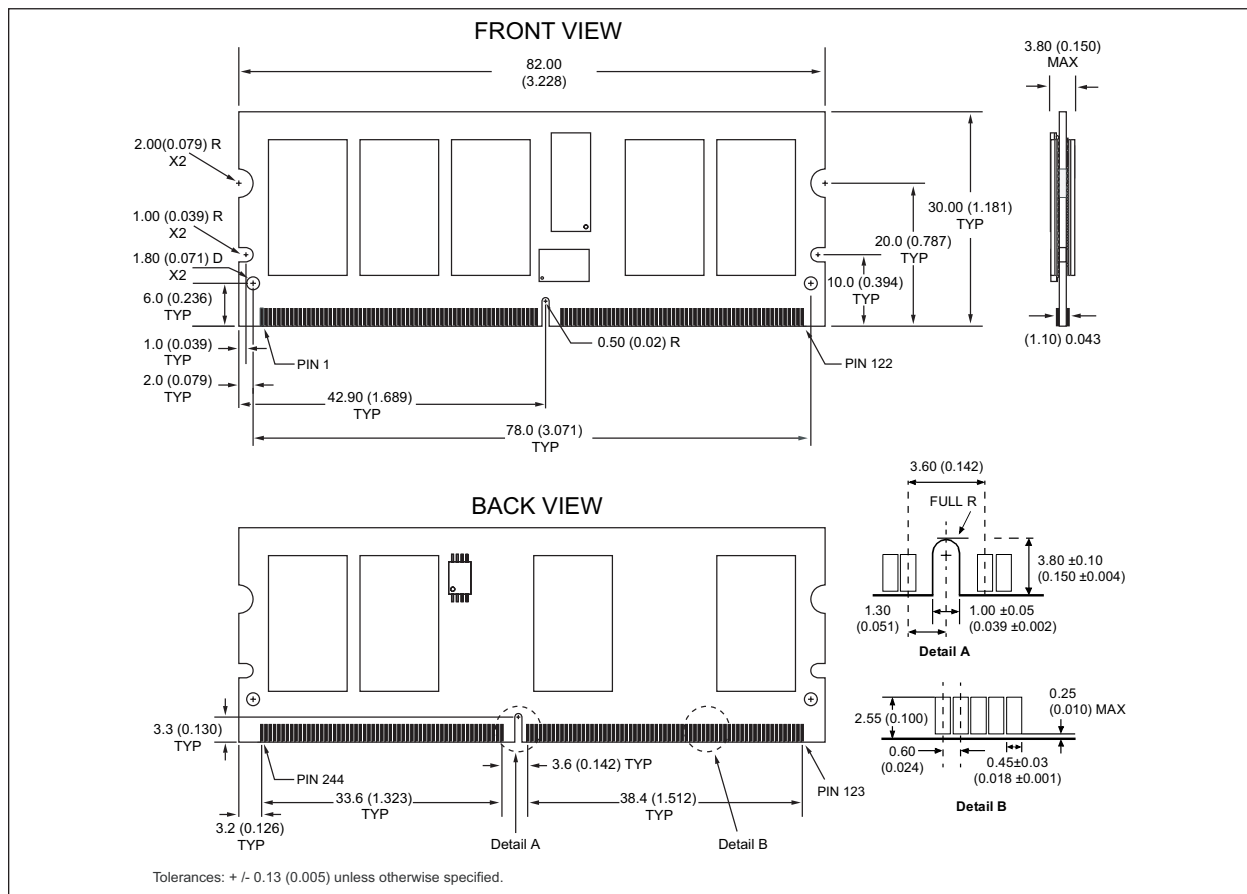
ORDERING INFORMATION FOR D7

Part Number	Clock Speed/ Data Rate	CAS Latency	t _{RC} D	t _{RP}	Height*
WV3HG64M72EER806D7xG	400MHz/800Mb/s	6	6	6	30.00mm (1.181") TYP
WV3HG64M72EER665D7xG	333MHz/667Mb/s	5	5	5	30.00mm (1.181") TYP
WV3HG64M72EER534D7xG	266MHz/533Mb/s	4	4	4	30.00mm (1.181") TYP
WV3HG64M72EER403D7xG	200MHz/400Mb/s	3	3	3	30.00mm (1.181") TYP

NOTES:

- Consult Factory for availability of RoHS products. (G = RoHS Compliant)
- Vendor specific part numbers are used to provide memory component source control. The place holder for this is shown as a lower case "x" in the part numbers above and is to be replaced with respective vendors code. Consult factory for qualified sourcing options.
(M = Micron, S = Samsung & consult factory for others)
- Consult factory for availability of industrial temperature (-40°C to 85°C) option

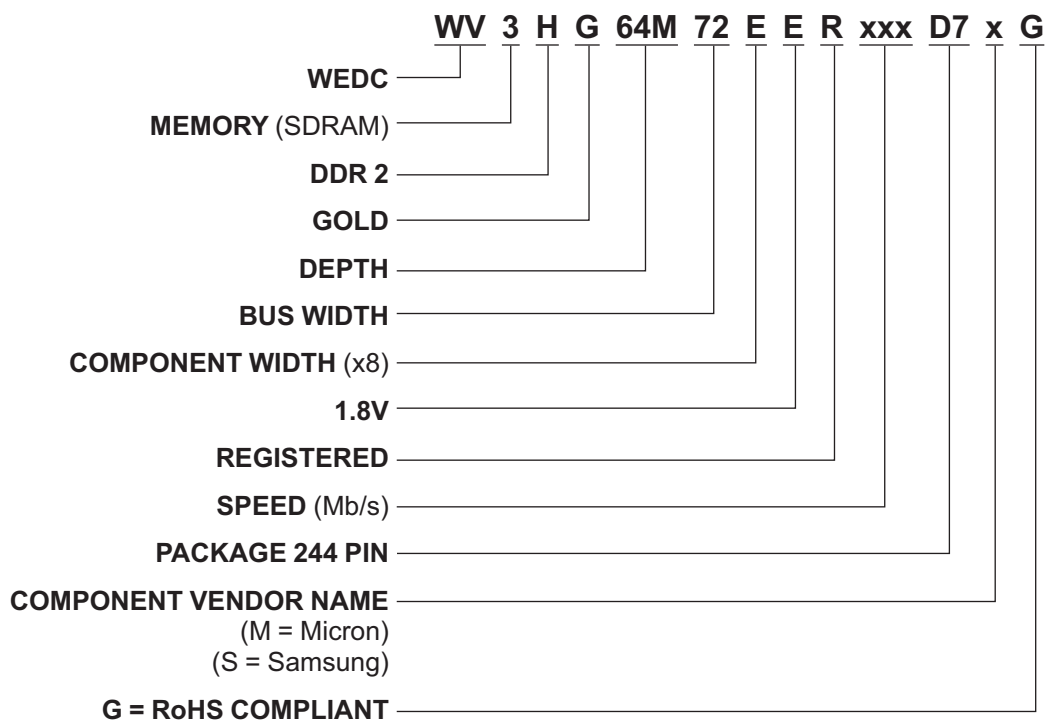
PACKAGE DIMENSIONS FOR D7



* ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)



PART NUMBERING GUIDE





Document Title

512MB – 64Mx72 DDR2 SDRAM REGISTERED, w/PLL, Mini-DIMM

Revision History

Rev #	History	Release Date	Status
Rev 0	Created	August 2005	Advanced
Rev 1	1.0 Updated CAP, Icc and AC specs. 1.1 Changed from Advanced to Preliminary	September 2005	Preliminary
Rev 2	2.0 Update Icc specs 2.1 Added DDR2-667 & DDR2-800 as TBD	February 2006	Preliminary