

## Surface Mount N-Channel Enhancement Mode MOSFET

**Pb** Lead(Pb)-Free

### Features:

\*Super high dense cell design for low  $R_{DS(ON)}$

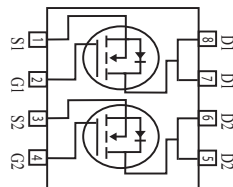
$$R_{DS(ON)} < 35m\Omega @ V_{GS} = 10V$$

$$R_{DS(ON)} < 62m\Omega @ V_{GS} = 4.5V$$

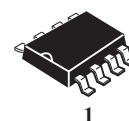
\*Simple Drive Requirement

\*Dual N MOSFET Package

\*SO-8 Package



**DRAIN CURRENT**  
**5 AMPERES**  
**DRAIN SOURCE VOLTAGE**  
**40 VOLTAGE**



**SO-8**

## Maximum Ratings (TA=25°C Unless Otherwise Specified)

Rating	Symbol	Value	Unite
Drain-Source Voltage	$V_{DS}$	40	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current <sup>(1)</sup> ( $T_A = 25^\circ C$ ) ( $T_A = 70^\circ C$ )	$I_D$	5	A
		4.2	
Pulsed Drain Current <sup>(2)</sup>	$I_{DM}$	20	A
Drain-Source Diode Forward Current <sup>(1)</sup>	$I_S$	1.7	A
Power Dissipation <sup>(1)</sup> ( $T_A = 25^\circ C$ ) ( $T_A = 70^\circ C$ )	$P_D$	2	W
		1.44	
Maximax Junction-to-Ambient <sup>(1)</sup>	$R_{\theta JA}$	62.5	$^\circ C/W$
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to 150	$^\circ C$

## Device Marking

WT6920AM=STM6920A

**Electrical Characteristics** (T<sub>A</sub>=25 °C Unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

**Static (2)**

Drain-Source Breakdown Voltage V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	V <sub>(BR)DSS</sub>	40	-	-	V
Gate-Source Threshold Voltage V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	V <sub>GS(th)</sub>	1	1.8	3	V
Gate-Source Leakage Current V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V	I <sub>GSS</sub>	-	-	±100	nA
Zero Gate Voltage Drain Current V <sub>DS</sub> =32V, V <sub>GS</sub> =0V	I <sub>DSS</sub>	-	-	1	uA
Drain-Source On-Resistance V <sub>GS</sub> =10V, I <sub>D</sub> =6A V <sub>GS</sub> =4.5V, I <sub>D</sub> =5A	r <sub>DS(on)</sub>	- -	24 45	35 62	mΩ
On-State Drain Current V <sub>DS</sub> =5V, V <sub>GS</sub> =10V	I <sub>D(on)</sub>	15	-	-	A
Forward Transconductance V <sub>DS</sub> =5V, I <sub>D</sub> =6A	g <sub>fs</sub>	-	10	-	S

**Dynamic(3)**

Input Capacitance V <sub>DS</sub> =25V, V <sub>GS</sub> =0V, f=1MHZ	C <sub>iss</sub>	-	759	-	pF
Output Capacitance V <sub>DS</sub> =25V, V <sub>GS</sub> =0V, f=1MHZ	C <sub>oss</sub>	-	92	-	
Reverse Transfer Capacitance V <sub>DS</sub> =25V, V <sub>GS</sub> =0V, f=1MHZ	C <sub>rss</sub>	-	70	-	

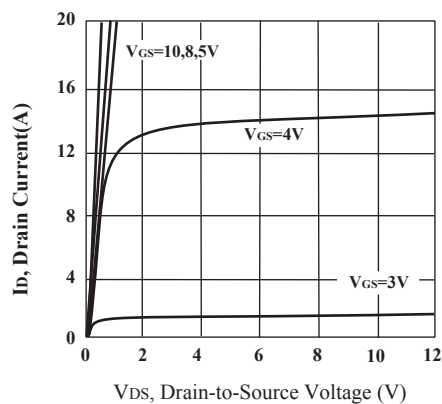
**Switching (3)**

Turn-On Delay Time V <sub>GS</sub> =10V, V <sub>DD</sub> =20V, I <sub>D</sub> =1A, R <sub>GEN</sub> =3.3Ω	t <sub>d(on)</sub>	-	9.2	-	nS
Rise Time V <sub>GS</sub> =10V, V <sub>DD</sub> =20V, I <sub>D</sub> =1A, R <sub>GEN</sub> =3.3Ω	t <sub>r</sub>	-	21	-	
Turn-Off Time V <sub>GS</sub> =10V, V <sub>DD</sub> =20V, I <sub>D</sub> =1A, R <sub>GEN</sub> =3.3Ω	t <sub>d(off)</sub>	-	15.5	-	
Fall Time V <sub>GS</sub> =10V, V <sub>DD</sub> =20V, I <sub>D</sub> =1A, R <sub>GEN</sub> =3.3Ω	t <sub>f</sub>	-	4.4	-	
Total Gate Charge V <sub>DS</sub> =20V, I <sub>D</sub> =6A, V <sub>GS</sub> =10V V <sub>DS</sub> =20V, I <sub>D</sub> =6A, V <sub>GS</sub> =4.5V	Q <sub>g</sub>	- -	15.9 7.6	- -	nC
Gate-Source Charge V <sub>DS</sub> =20V, V <sub>GS</sub> =10V, I <sub>D</sub> =6A	Q <sub>gs</sub>	-	2.2	-	
Gate-Drain Charge V <sub>DS</sub> =20V, V <sub>GS</sub> =10V, I <sub>D</sub> =6A	Q <sub>gd</sub>	-	4.8	-	
Drain-Source Diode Forward Voltage V <sub>GS</sub> =0V, I <sub>S</sub> =1.7A	V <sub>SD</sub>	-	0.8	1.2	V

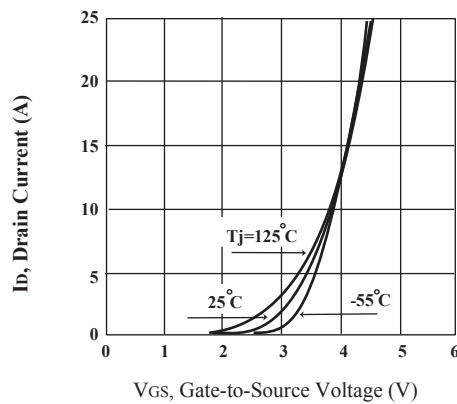
Note: 1. Surface Mounted on FR4 Board t ≤ 10sec.

2. Pulse Test : PW ≤ 300us, Duty Cycle ≤ 2%.

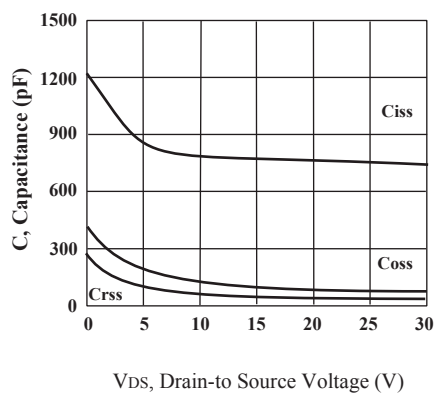
3. Guaranteed by Design, not Subject to Production Testing.



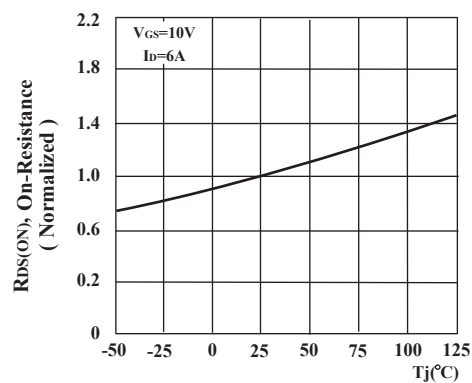
**Fig.1 Output Characteristics**



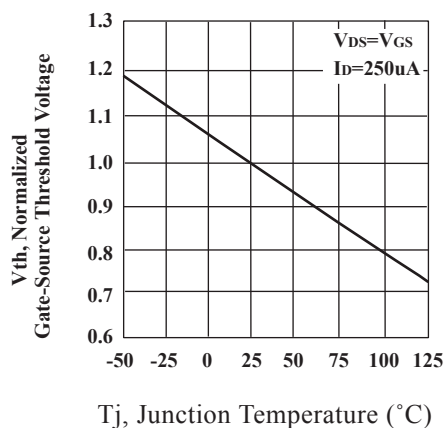
**Fig.2 Transfer Characteristics**



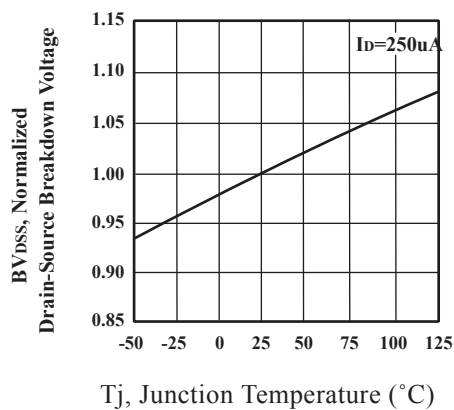
**Figure 3. Capacitance**



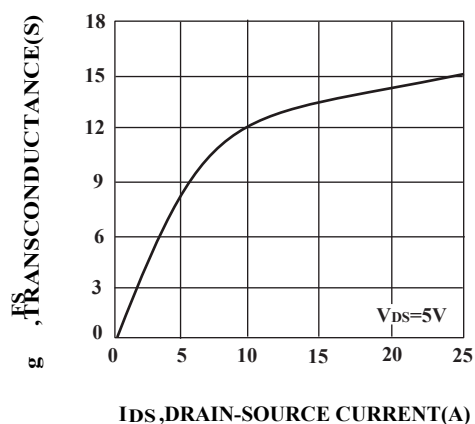
**Fig.4 On-Resistance Variation with Temperature**



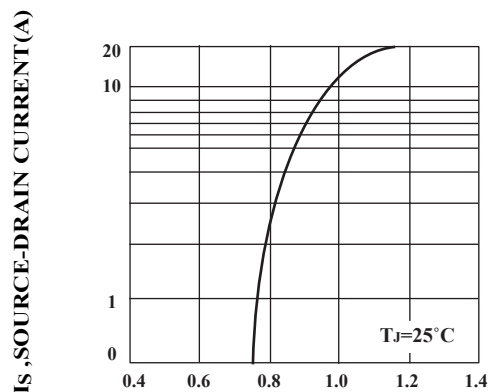
**Fig.5 Gate Threshold Variation with Temperature**



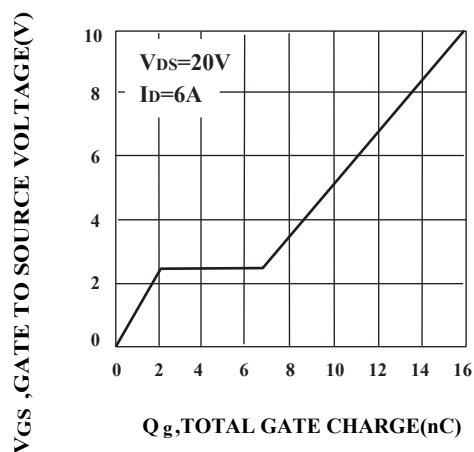
**Fig.6 Breakdown Voltage Variation with Temperature**



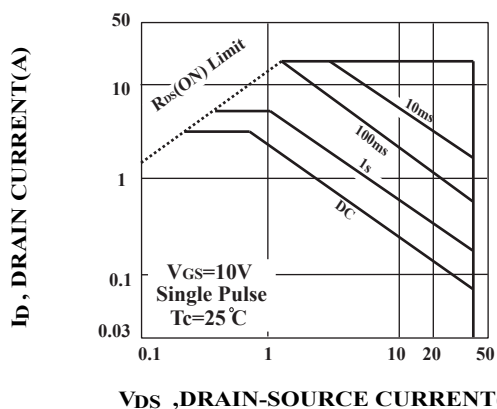
**FIG.7 Transconductance Variation with Drain Current**



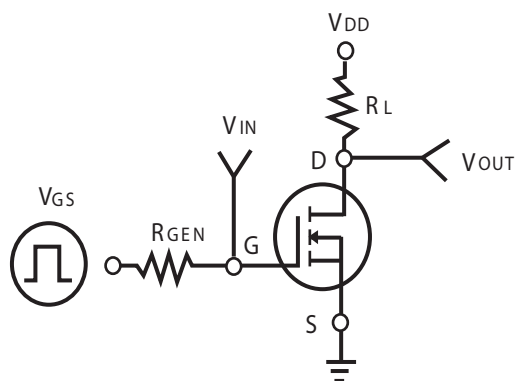
**FIG.8 Body Diode Forward Voltage Variation with Source Current**



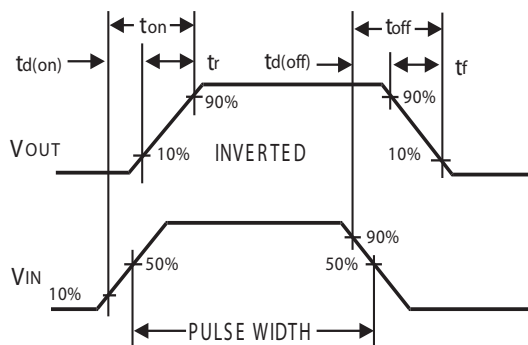
**FIG.9 Gate Charge**



**FIG.10 Maximum Safe Operating Area**



**FIG.11 Switching Test Circuit**



**FIG.12 Switching Waveforms**

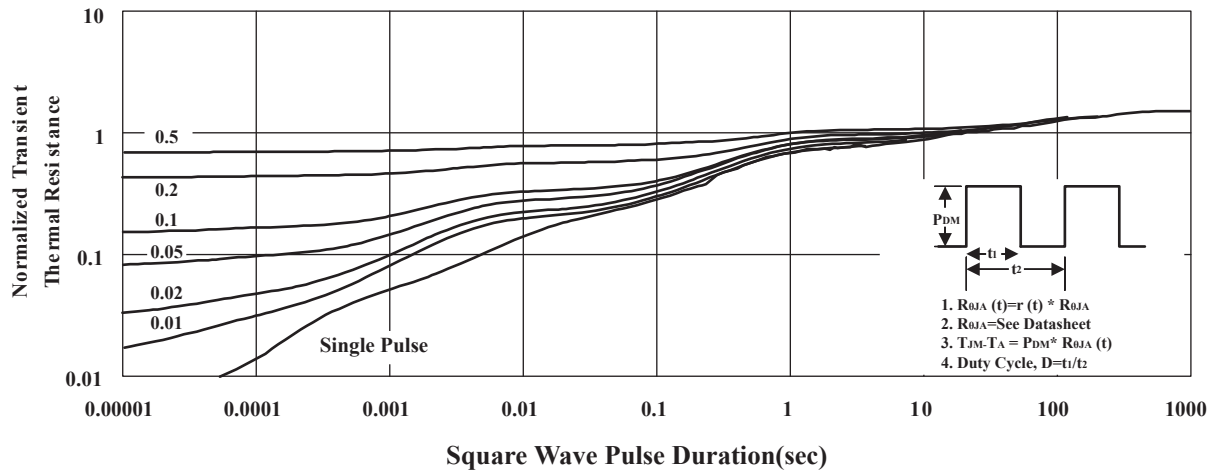
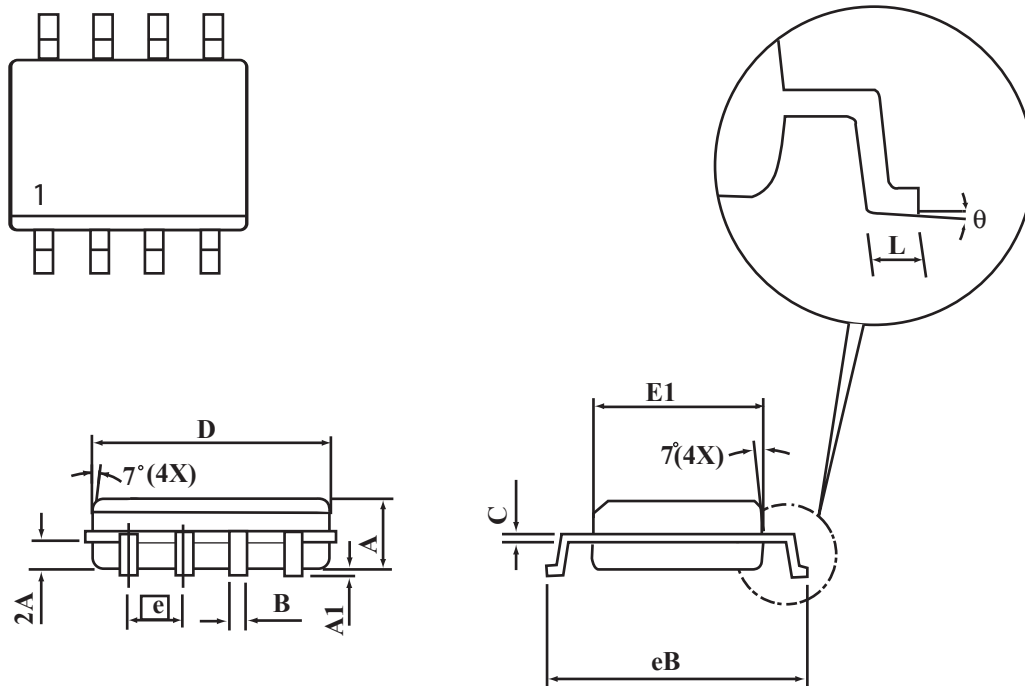


FIG.13 NORMALIZED THERMAL TRANSIENT IMPEDANCE CUREVE

## SO-8 Package Outline Dimensions

Unit:mm



SYMBOLS	MILLIMETERS	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.20
B	0.35	0.45
C	0.18	0.23
D	4.69	4.98
E1	3.56	4.06
eB	5.70	6.30
e	1.27 BSC	
L	0.60	0.80
$\theta$	0°	8°