

W24L011A



128K ´ 8 HIGH SPEED CMOS STATIC RAM

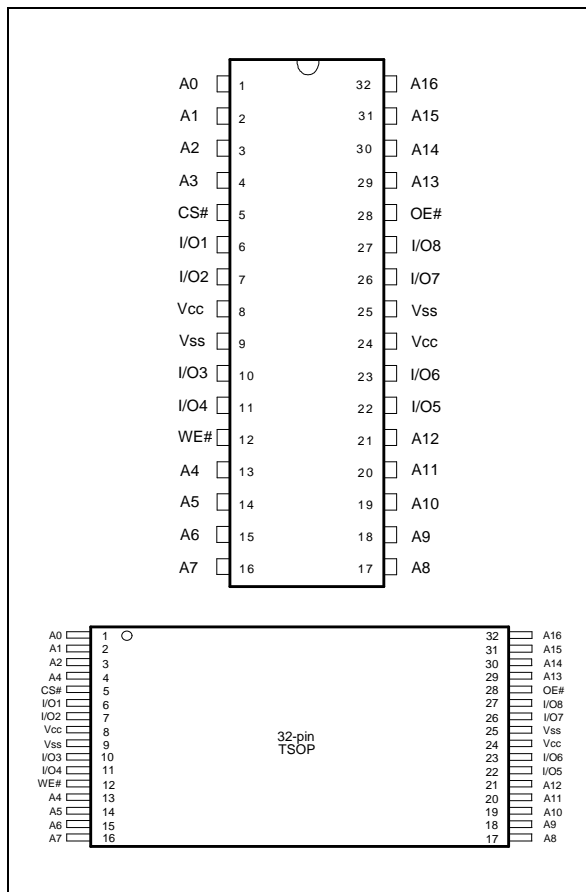
GENERAL DESCRIPTION

The W24L011A is a high speed, low power CMOS static RAM organized as 131072 x 8 bits that operates on a single 3.3-volt power supply. This device is manufactured using Winbond's high performance CMOS technology.

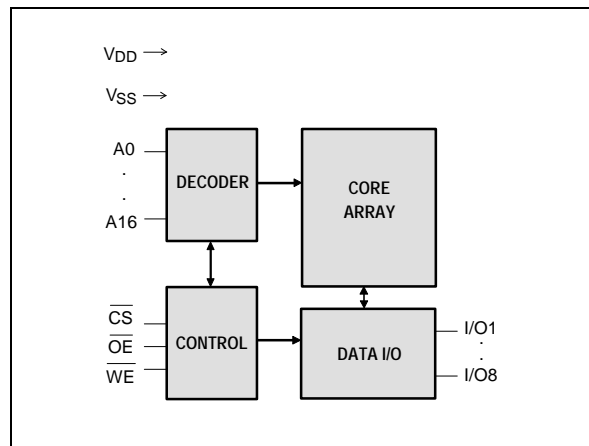
FEATURES

- High speed access time: 10/12/15 nS
- Single +3.3V power supply
- Center power/ground pin configuration
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three-state outputs
- Available packages: 32-pin 300 mil SOJ, Small TSOP-I (8 x 13.4 mm), TSOP-I (8 x 20 mm) and 400 mil SOJ

PIN CONFIGURATIONS



BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 – A16	Address Inputs
I/O1 – I/O8	Data Inputs/Outputs
CS	Chip Select Inputs
WE	Write Enable Input
OE	Output Enable Input
VDD	Power Supply
VSS	Ground

TRUTH TABLE

CS	OE	WE	MODE	I/O1 - I/O8	V _{DD} CURRENT
H	X	X	Not Selected	High Z	I _{SB} , I _{SB1}
L	H	H	Output Disable	High Z	I _{DD}
L	L	H	Read	Data Out	I _{DD}
L	X	L	Write	Data In	I _{DD}

DC CHARACTERISTICS

Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Supply Voltage to V _{SS} Potential	-0.5 to +4.6	V
Input/Output to V _{SS} Potential	-0.5 to V _{DD} +0.5	V
Allowable Power Dissipation	1.0	W
Storage Temperature	-65 to +150	°C
Operating Temperature	0 to +70	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

Operating Characteristics

(V_{DD} = 3.3V ±5%, V_{SS} = 0V, T_A = 0 to 70° C)

PARAMETER	SYM.	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Input Low Voltage	V _{IL}	-		-0.5	-	0.8	V
Input High Voltage	V _{IH}	-		+2.0	-	V _{DD} +0.5	V
Input Leakage Current	I _{LI}	V _{IN} = V _{SS} to V _{DD}		-10	-	+10	μA
Output Leakage Current	I _{LO}	V _{I/O} = V _{SS} to V _{DD} , $\overline{\text{CS}}$ = V _{IH} (min.) or $\overline{\text{OE}}$ = V _{IH} (min.) or $\overline{\text{WE}}$ = V _{IL} (max.)		-10	-	+10	μA
Output Low Voltage	V _{OL}	I _{OL} = +8.0 mA		-	-	0.4	V
Output High Voltage	V _{OH}	I _{OH} = -4.0 mA		2.4	-	-	V
Operating Power Supply Current	I _{DD}	$\overline{\text{CS}}$ = V _{IL} (max.), I/O = 0 mA Cycle = min., Duty = 100%	10	-	-	130	mA
			12	-	-	120	
			15	-	-	100	
Standby Power Supply Current	I _{SB}	$\overline{\text{CS}}$ = V _{IH} (min.)		-	-	15	mA
Supply Current	I _{SB1}	$\overline{\text{CS}}$ ≥ V _{DD} -0.2V		-	-	5	mA

Note: Typical characteristics are at V_{DD} = 3.3V, T_A = 25° C.

CAPACITANCE

(V_{DD} = 3.3V, T_A = 25° C, f = 1 MHz)

PARAMETER	SYM.	CONDITIONS	MAX.	UNIT
Input Capacitance	C _{IN}	V _{IN} = 0V	8	pF
Input/Output Capacitance	C _{I/O}	V _{OUT} = 0V	10	pF

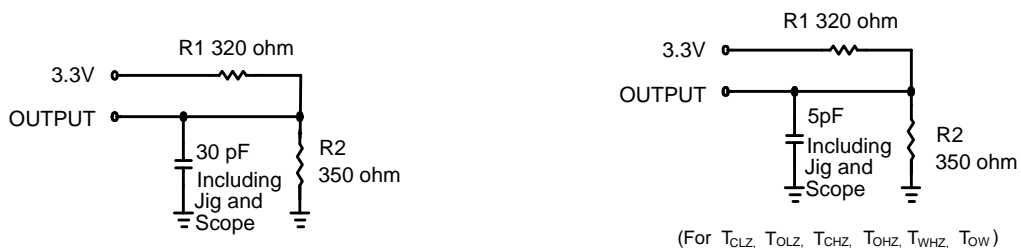
Note: These parameters are sampled but not 100% tested.

AC CHARACTERISTICS

AC Test Conditions

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3 nS
Input and Output Timing Reference Level	1.5V
Output Load	C _L = 30 pF, I _{OH} /I _{OL} = -4 mA/8 mA

AC Test Loads and Waveform



AC Characteristics, continued

(V_{DD} = 3.3V ±5%, V_{SS} = 0V, T_A = 0 to 70°)

Read Cycle

PARAMETER	SYM.	W24L011A-10		W24L011A-12		W24L011A-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	TRC	10	-	12	-	15	-	nS
Address Access Time	TAA	-	10	-	12	-	15	nS
Chip Select Access Time	TACS	-	10	-	12	-	15	nS
Output Enable to Output Valid	TAOE	-	5	-	6	-	8	nS
Chip Selection to Output in Low Z	TCLZ	3	-	3	-	-	3	nS
Output Enable to Output in Low Z	TOLZ*	0	-	0	-	-	-	nS
Chip Deselection to Output in High Z	TCHZ	-	5	-	6	-	8	nS
Output Disable to Output in High Z	TOHZ*	-	5	-	6	-	8	nS
Output Hold from Address Change	TOH	3	-	3	-	3	-	nS

* These parameters are sampled but not 100% tested.

Write Cycle

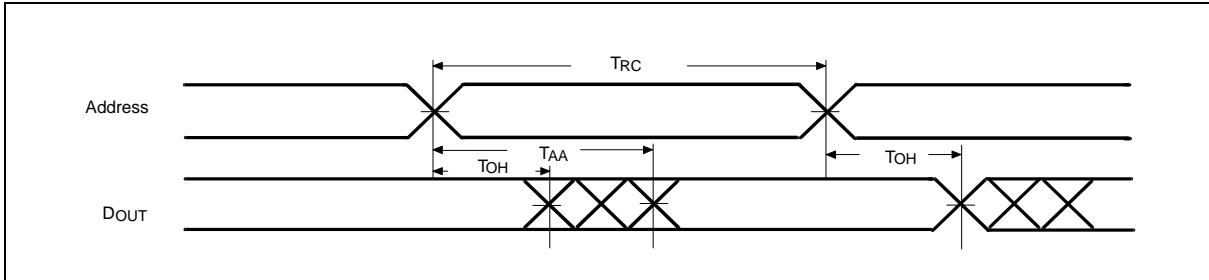
PARAMETER		SYM.	W24L011A-10		W24L011A-12		W24L011A-15		UNIT
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time		TWC	10	-	12	-	15	-	nS
Chip Selection to End of Write		TCW	9	-	10	-	12	-	nS
Address Valid to End of Write		TAW	9	-	10	-	12	-	nS
Address Setup Time		TAS	0	-	0	-	0	-	nS
Write Pulse Width		TWP	9	-	10	-	12	-	nS
Write Recovery Time	$\overline{\text{CS}}, \overline{\text{WE}}$	TWR	0	-	0	-	0	-	nS
Data Valid to End of Write		TDW	5	-	7	-	9	-	nS
Data Hold from End of Write		TDH	0	-	0	-	0	-	nS
Write to Output in High Z		TWHZ*	-	5	-	6	-	8	nS
Output Disable to Output in High Z		TOHZ*	-	5	-	6	-	8	nS
Output Active from End of Write		TOW	0	-	0	-	0	-	nS

* These parameters are sampled but not 100% tested.

TIMING WAVEFORMS

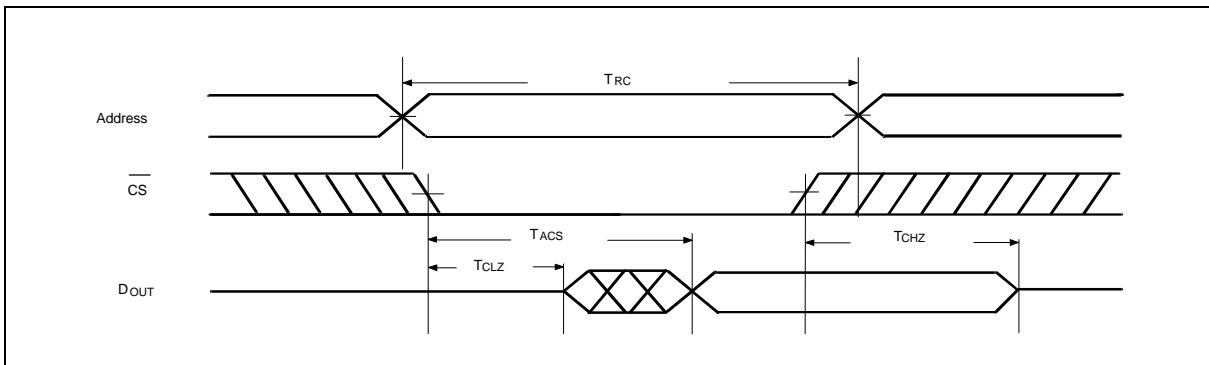
Read Cycle 1

(Address Controlled, $\overline{CS} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$)



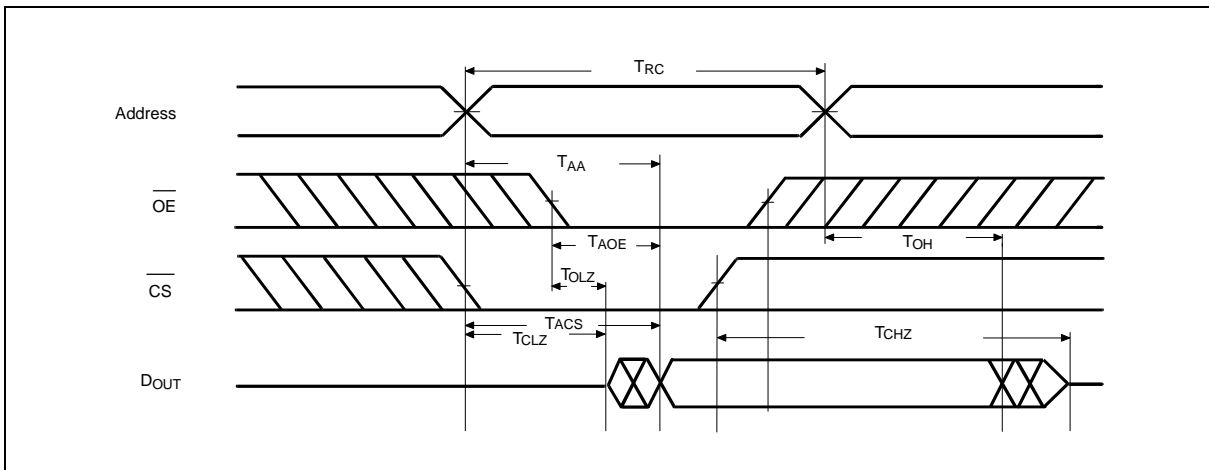
Read Cycle 2

(Chip Select Controlled)



Read Cycle 3

(Output Enable Controlled)



Write Cycle 1

The diagram illustrates the timing relationships for a memory access cycle. The signals and their timing parameters are as follows:

- Address:** The address bus signal. T_{WC} is the total width of the address signal during the access cycle.
- CS (Chip Select):** The chip select signal, shown as a pulse. T_{CW} is the pulse width, and T_{WR} is the time from the falling edge of CS to the start of the data output.
- WE (Write Enable):** The write enable signal, shown as a pulse. T_{AW} is the pulse width, and T_{AS} is the time from the falling edge of WE to the start of the data output.
- DOUT (Data Output):** The data output signal. T_{WP} is the pulse width of the data output. T_{WHZ} (1, 4) is the time from the end of the data output pulse to the start of the high-impedance state. T_{OW} is the time from the start of the high-impedance state to the start of the next data output pulse. The high-impedance state is labeled (2) and the next data output pulse is labeled (3).
- DIN (Data Input):** The data input signal. T_{DW} is the time from the start of the data input pulse to the start of the data output pulse. T_{DH} is the time from the end of the data input pulse to the end of the data output pulse.

1. During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.
2. The data output from DOUT are the same as the data written to DIN during the write cycle.
3. DOUT provides the read data for the next address.
4. Transition is measured ± 200 mV from steady state with $C_L = 5$ pF. This parameter is guaranteed but not 100% tested.

ORDERING INFORMATION

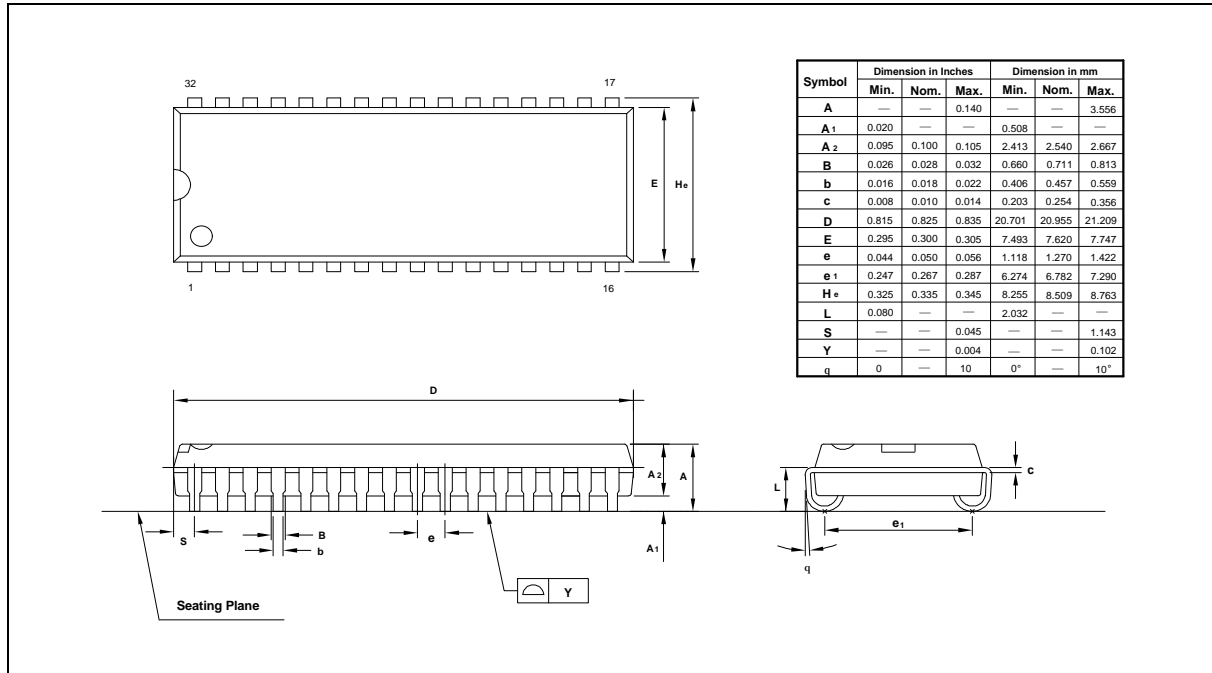
PART NO.	ACCESS TIME (nS)	OPERATING CURRENT MAX. (mA)	STANDBY CURRENT MAX. (mA)	OPERATION TEMPERATURE (°C)	PACKAGE
W24L011AJ-10	10	130	10	0 to +70	300 mil SOJ
W24L011AJ-12	12	120	10	0 to +70	300 mil SOJ
W24L011AJ-15	15	110	10	0 to +70	300 mil SOJ
W24L011AI-10	10	130	10	0 to +70	400 mil SOJ
W24L011AI-12	12	120	10	0 to +70	400 mil SOJ
W24L011AI-15	15	110	10	0 to +70	400 mil SOJ
W24L010AT-10	10	130	10	0 to +70	TSOP (8 x 20 mm)
W24L010AT-12	12	120	10	0 to +70	TSOP (8 x 20 mm)
W24L010AT-15	15	110	10	0 to +70	TSOP (8 x 20 mm)
W24L010AQ-10	10	130	10	0 to +70	TSOP (8 x 13.4 mm)
W24L010AQ-12	12	120	10	0 to +70	TSOP (8 x 13.4 mm)
W24L010AQ-15	15	110	10	0 to +70	TSOP (8 x 13.4 mm)

Notes:

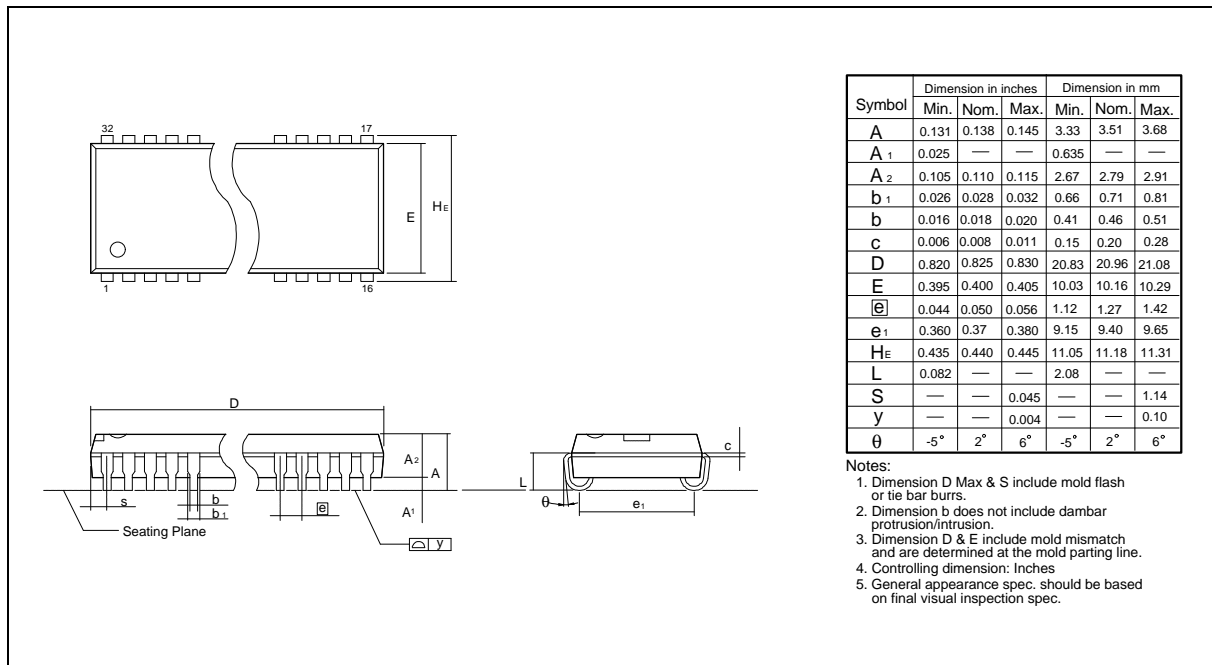
1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

PACKAGE DIMENSIONS

32-pin SOJ (300 mil)

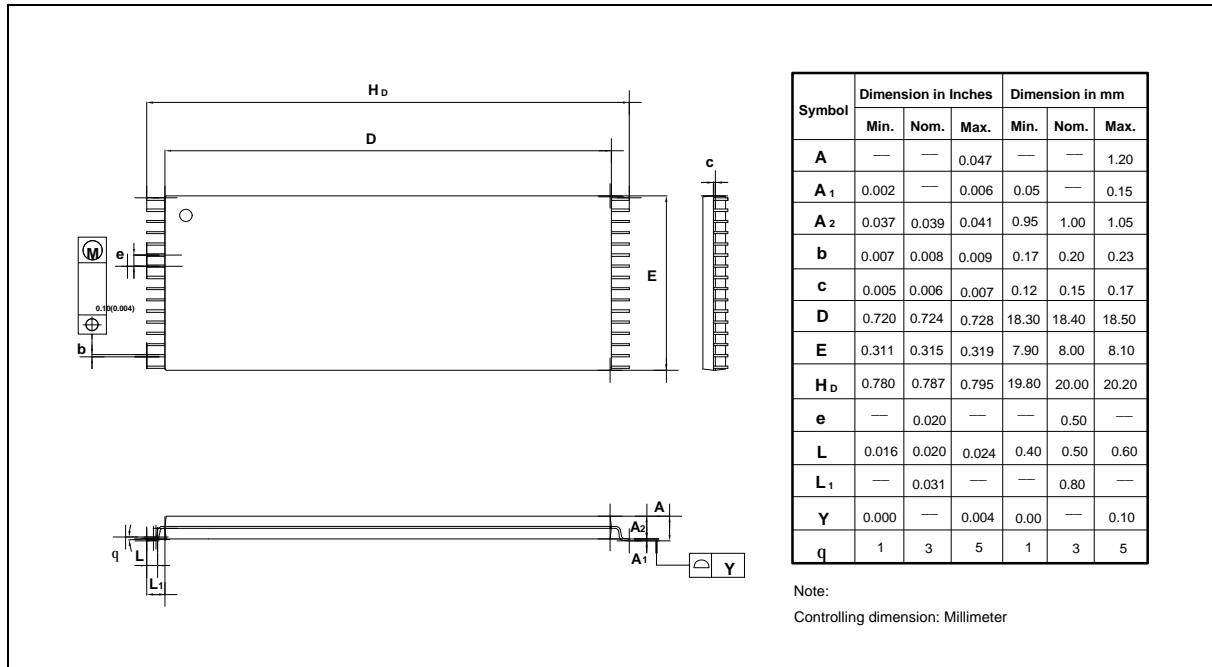


32-pin SOJ (400 mil)

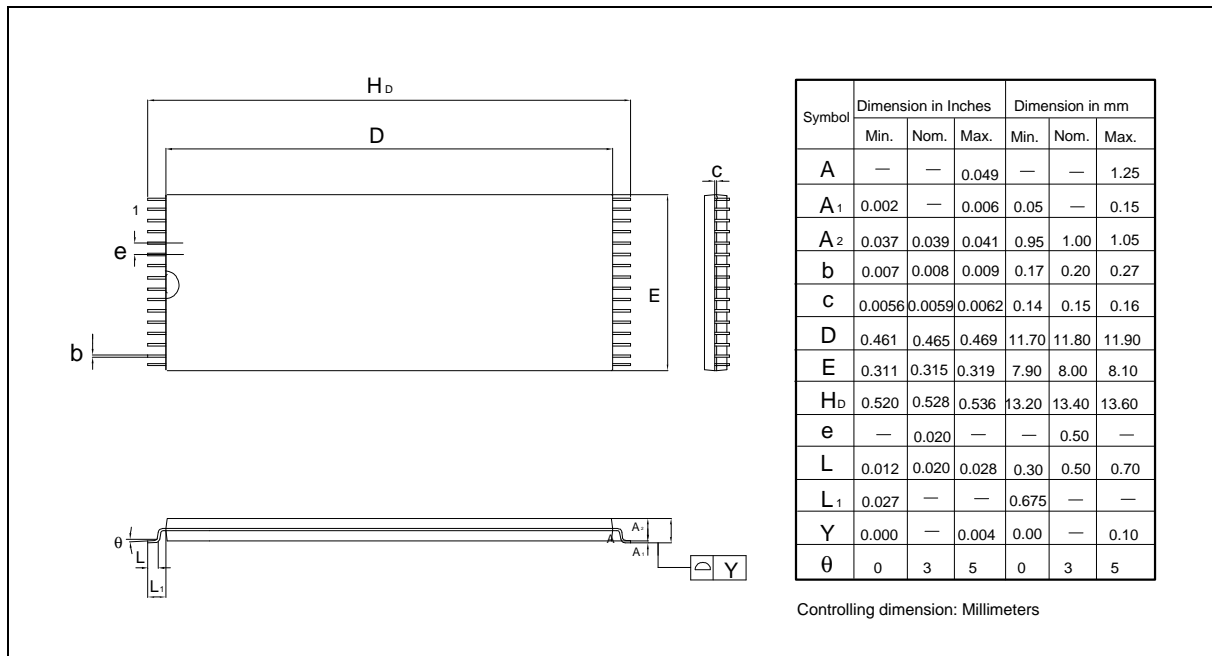


Package Dimensions, continued

32-pin TSOP



32-Lead Small Type One TSOP (8 x 13.4)





VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	Aug. 1997	-	Initial Issued
A2	Aug. 1999	1, 2, 4, 7	Add 15 nS specification
A3	Apr. 26, 2002	1, 2, 7, 9	Add TSOP package and change (IDD, ISB & ISBC) current



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