

Preliminary W27L520



64K \times 8 ELECTRICALLY ERASABLE EPROM

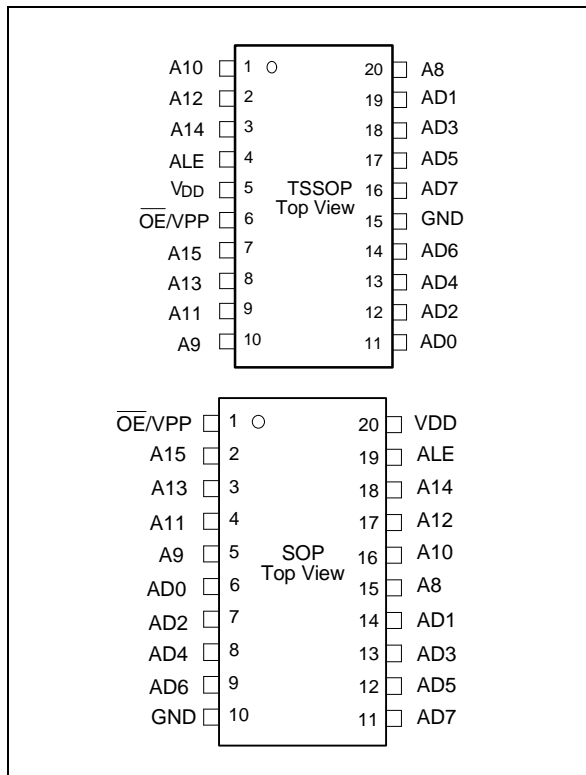
GENERAL DESCRIPTION

The W27L520 is a high speed, low power Electrically Erasable and Programmable Read Only Memory organized as $65,536 \times 8$ bits. It includes latches for the lower 8 address lines to multiplex with the 8 data lines. To cooperate with the MCU, this device could save the external TTL component, also cost and space. It requires only one supply in the range of 3.0V in normal read mode. The W27L520 provides an electrical chip erase function. It will be a great convenient when you need to change/update the contents in the device.

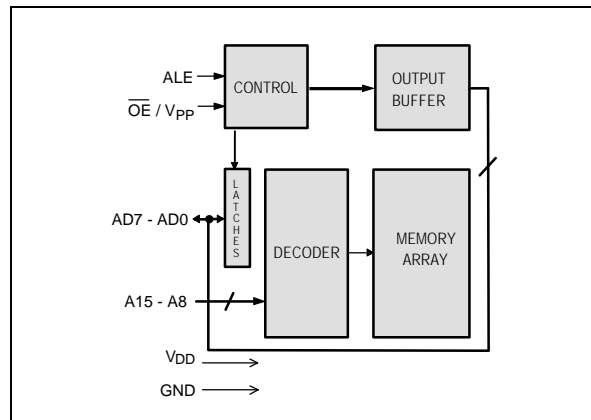
FEATURES

- High speed access time: 70/90 nS (max.)
- Read operating current: 8 mA (max.)
- Erase/Programming operating current 30 mA (max.)
- Standby current: 20 μ A (max.)
- Unregulated battery power supply range, 3.0V to 3.6V
- +13V erase and programming voltage
- High Reliability CMOS Technology
 - 2K V ESD Protection
 - 200 mA Latchup Immunity
- Fully static operation
- All inputs and outputs directly LVTTTL/CMOS compatible
- Three-state outputs
- Available packages: 20-pin TSSOP and 20-pin SOP

PIN CONFIGURATIONS



BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
AD0-AD7	Address/Data Inputs/Outputs
A8-A15	Address Inputs
ALE	Address Latch Enable
OE/VPP	Output Enable, Program/Erase Supply Voltage
VDD	Power Supply
GND	Ground



FUNCTIONAL DESCRIPTION

Read Mode

Unlike conventional UVEPROMs, which has \overline{CE} and \overline{OE} two control functions, the W27L520 has one \overline{OE}/V_{PP} and one ALE (address_latch_enable) control functions. The ALE makes lower address A[7:0] to be latched in the chip when it goes from high to low, so that the same bus can be used to output data during read mode. i.e. lower address A[7:0] and data bus DQ[7:0] are multiplexed. \overline{OE}/V_{PP} controls the output buffer to gate data to the output pins. When addresses are stable, the address access time (TACC) is equal to the delay from ALE to output (TCE), and data are available at the outputs TOE after the falling edge of \overline{OE}/V_{PP} , if TACC and TCE timings are met.

Erase Mode

The erase operation is the only way to change data from "0" to "1." Unlike conventional UVEPROMs, which use ultraviolet light to erase the contents of the entire chip (a procedure that requires up to half an hour), the W27L520 uses electrical erasure. Generally, the chip can be erased within 100 mS by using an EPROM writer with a special erase algorithm.

There are two ways to enter Erase mode. One is to raise \overline{OE}/V_{PP} to VPE (13V), $V_{DD} = V_{DE}$ (6.5V), A9 = VHH (13V), A10 = high A8&A11 = low, and all other address pins include AD[7:0] keep at fixed low or high. Pulsing ALE high starts the erase operation. The other way is somewhat like flash, by programming two consecutive commands into the device and then enter Erase mode. The two commands are loading Data = AA(hex) to Addr. = 5555(hex) and Data = 10(hex) to Addr. = 2AAA(hex). Be careful to note that the ALE pulse widths of these two commands are different: One is 50uS, while the other is 100mS. Please refer to the Smart Erase Algorithm 1 & 2.

Erase Verify Mode

The device will enter the Erase Verify Mode automatically after Erase Mode. Only power down the device can force the device enter Normal Read Mode again.

Program Mode

Programming is the only way to change cell data from "1" to "0." The program mode is entered when \overline{OE}/V_{PP} is raised to VPP (13V), $V_{DD} = V_{DP}$ (6.5V), the address pins equal the desired addresses, and the input pins equal the desired inputs. Pulsing ALE high starts the programming operation.

Program Verify Mode

The device will enter the Program Verify Mode automatically after Program Mode. Only power down the device can force the device enter Normal Read Mode again.

Erase/Program Inhibit

Erase or program inhibit mode allows parallel erasing or programming of multiple chips with different data. When ALE low, erasing or programming of non-target chips is inhibited, so that except for the ALE and \overline{OE}/V_{PP} pins, the W27L520 may have common inputs.

Standby Mode

The standby mode significantly reduces V_{DD} current. This mode is entered when ALE and \overline{OE}/V_{PP} keep high. In standby mode, all outputs are in a high impedance state.

System Considerations

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An EPROM's power switching characteristics require careful device decoupling. System designers are interested in three supply current issues: standby current levels (ISB), active current levels (IDD), and transient current peaks produced by the falling and rising edges of ALE. Transient current magnitudes depend on the device output's capacitive and inductive loading. Proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a

0.1 μ F ceramic capacitor connected between its VDD and GND. This high frequency, low inherent-inductance capacitor should be placed as close as possible to the device. Additionally, for every eight devices, a 4.7 μ F electrolytic capacitor should be placed at the array's power supply connection between VDD and GND. The bulk capacitor will overcome voltage slumps caused by PC board trace inductances.

TABLE OF OPERATING MODES

(VPP = 13V, VPE = 13V, VHH = 12V, VDP = 6.5V, VDE = 6.5V, VDD = 3.3V, VDI = 5.0V, X = VIH or VIL)

MODE	PIN				
	ALE	\overline{OE}/V_{PP}	OTHER ADDRESS	VDD	AD[7:0]
Address Latch Enable	VIH	VIH	X	VDD	A[7:0]
Read	VIL	VIL	AIN	VDD	DOUT
Output Disable	VIL	VIH	X	VDD	High Z
Standby	VIH	VIH	AIN	VDD	A[7:0]
Program	VIH	VPP	AIN	VDP	DIN
Erase 1	VIH	VPE	A8&A11 = VIL, A9 = VPE, A10 = VIH, Others = X	VDE	X
Erase 2	VIH	VPE	First command: Addr. = 5555 (hex)	VDE	AA(hex)
			Secon command: Addr. = 2AAA (hex)	VDE	10(hex)
Product Identifier- manufacturer	VIL	VIL	A8 = VIL, A9 = VHH, Others = X	VDI	DA(Hex)
Product Identifier-device	VIL	VIL	A8 = VIH, A9 = VHH, Others = X	VDI	1F(Hex)

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DC CHARACTERISTICS

Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Ambient Temperature with Power Applied	-55 to +125	°C
Storage Temperature	-65 to +150	°C
Voltage on all Pins with Respect to Ground Except OE/VPP, A9 and VDD Pins	-2.0 to +7.0	V
Voltage on OE/VPP Pin with Respect to Ground	-2.0 to +7.0	V
Voltage on A9 Pin with Respect to Ground	-2.0 to +7.0	V
Voltage VDD Pin with Respect to Ground	-2.0 to +14.0	V

Note: 1. Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

2. Minimum voltage is -0.6V DC which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is VDD+0.75V DC which may overshoot to +7.0V for pulses of less than 20ns.

DC Erase Characteristics

(TA = 25° C ±5° C, VDD = 6.5V ±0.25V)

PARAMETER	SYM.	CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Input Load Current	ILI	VIN = VIL or VIH	-10	-	10	μA
VDD Erase Current	ICP	ALE = VIH, OE/VPP = VPE A8&A11 = VIL, A9 = VPE, A10 = VIH, Others = X	-	-	30	mA
VPP Erase Current	IPP	ALE = VIH, OE/VPP = VPE A8&A11 = VIL, A9 = VPE, A10 = VIH, Others = X	-	-	30	mA
Input Low Voltage	VIL	-	-0.3	-	0.8	V
Input High Voltage	VIH	-	2.4	-	VDD+0.3	V
Output Low Voltage (Verify)	VOL	IOL = 2.1 mA	-	-	0.45	V
Output High Voltage (Verify)	VOH	IOH = -0.4 mA	2.4	-	-	-
A9 SID Voltage	VHH	VDD = 5V ± 10%	11.5	12	12.5	V
A9 Erase Voltage	VPE	-	12.75	13	13.25	V
VPP Erase Voltage	VPE	-	12.75	13	13.25	V
VDD Supply Voltage (Erase & Erase Verify)	VDE	-	6.25	6.5	6.75	V

Note: VDD must be applied simultaneously or before VPP and removed simultaneously or after VPP.

CAPACITANCE

(VDD = 3.0V to 3.6V, TA = 25° C, f = 1 MHz)

PARAMETER	SYMBOL		MAX.	UNIT
Input Capacitance	CIN	VIN = 0V	6	pF
Output Capacitance	COUT	VOUT = 0V	12	pF

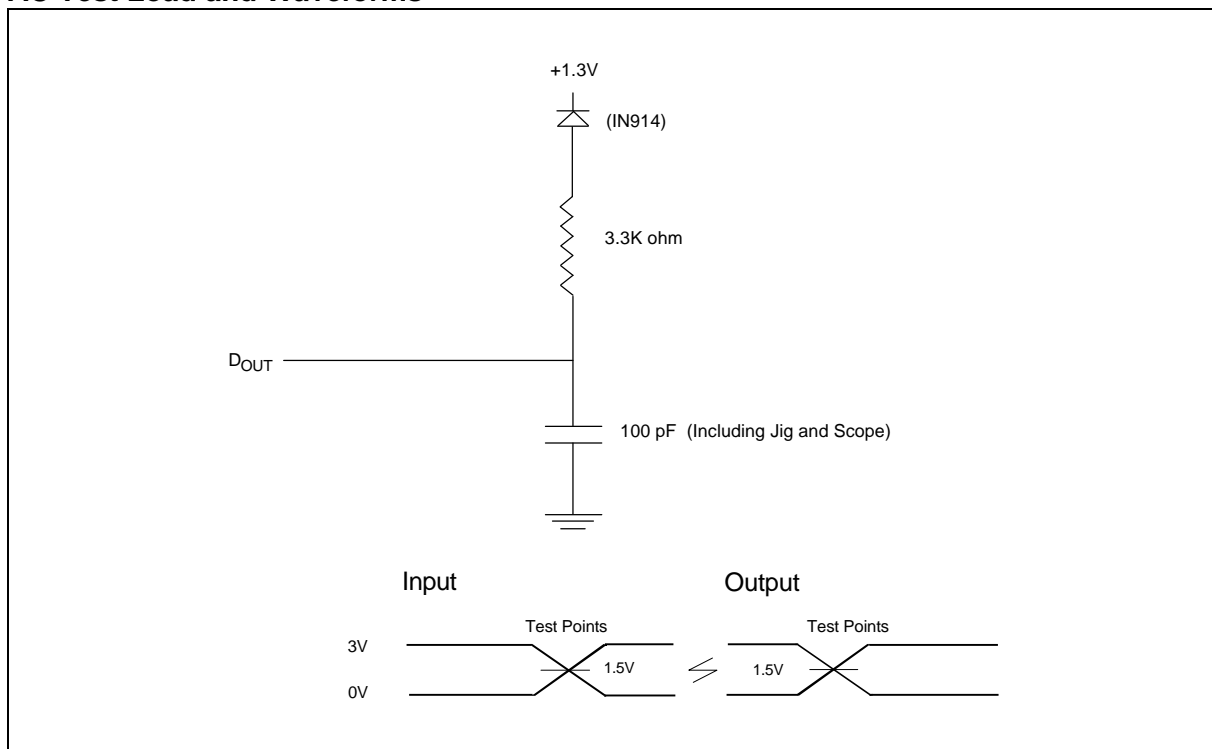


AC CHARACTERISTICS

AC Test Conditions

PARAMETER	CONDITIONS
Input Pulse Levels	0V/3V
Input Rise and Fall Times	10 nS
Input and Output Timing Reference Level	1.5V/1.5V
Output Load	CL = 100 pF, IOH/IO L = -0.4 mA/2.1 mA

AC Test Load and Waveforms



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READ OPERATION DC CHARACTERISTICS

(V_{DD} = 3.0V to 3.6V, T_A = 0 to 70° C)

PARAMETER	SYM.	CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Input Load Current	I _{LI}	V _{IN} = 0V to V _{DD}	-5	-	5	μA
Output Leakage Current	I _{LO}	V _{OUT} = 0V to V _{DD}	-5	-	5	μA
Standby V _{DD} Current (CMOS input)	I _{SB}	ALE = V _{DD} ±0.3V, \overline{OE}/V_{PP} = V _{DD} ±0.3V All others inputs = GND/ V _{DD} ±0.3V	-	-	20	μA
V _{DD} Operating Current	I _{DD}	ALE = V _{IL} , I _{OUT} = 0 mA f = 5 MHz	-	-	8	mA
Input Low Voltage	V _{IL}	-	-0.6	-	0.8	V
Input High Voltage	V _{IH}	-	2.0	-	V _{DD} +0.3	V
Output Low Voltage	V _{OL}	I _{OL} = 2.1 mA	-	-	0.4	V
Output High Voltage	V _{OH}	I _{OH} = -0.4 mA	2.4	-	-	V

READ OPERATION AC CHARACTERISTICS

(V_{DD} = 3.0V to 3.6V, T_A = 0 to 70° C)

PARAMETER	SYM.	W27L520-70		W27L520-90		UNIT
		MIN.	MAX.	MIN.	MAX.	
Address Latch Enable Access Time	T _{CE}	-	70	-	90	nS
Address Latch Enable Width	T _{ALE}	45	-	45	-	nS
Address Access Time	T _{ACC}	-	70	-	90	nS
Address Setup Time	T _{AS}	15	-	15	-	nS
Address Hold Time	T _{AH}	15	-	15	-	nS
Output Enable Access Time	T _{OE}	-	35	-	35	nS
\overline{OE} /V _{PP} High to High-Z Output	T _{DF}	-	25	-	25	nS
Output Hold from Address Change	T _{OH}	0	-	0	-	nS

Note: V_{DD} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

DC PROGRAMMING CHARACTERISTICS

(V_{DD} = 6.5V ±0.25V, T_A = 25° C ±5° C)

PARAMETER	SYM.	CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Input Load Current	I _{LI}	V _{IN} = V _{IL} or V _{IH}	-10	-	10	μA
V _{DD} Program Current	I _{CP}	ALE = V _{IH} , OE /V _{PP} = V _{PP}	-	-	30	mA
V _{PP} Program Current	I _{PP}	ALE = V _{IH} , OE /V _{PP} = V _{PP}	-	-	30	mA
Input Low Voltage	V _{IL}	-	-0.3	-	0.8	V
Input High Voltage	V _{IH}	-	2.4	-	V _{DD} +0.5	V
Output Low Voltage (Verify)	V _{OL}	I _{OL} = 2.1 mA	-	-	0.45	V
Output High Voltage (Verify)	V _{OH}	I _{OH} = -0.4 mA	2.4	-	-	V
A9 Silicon I.D. Voltage	V _{HH}	V _{DD} = 5V ± 10%	11.5	12.0	12.5	V
V _{PP} Program Voltage	V _{PP}	-	12.75	13.0	13.25	V
V _{DD} Supply Voltage (Program)	V _{DP}	-	6.25	6.5	6.75	V

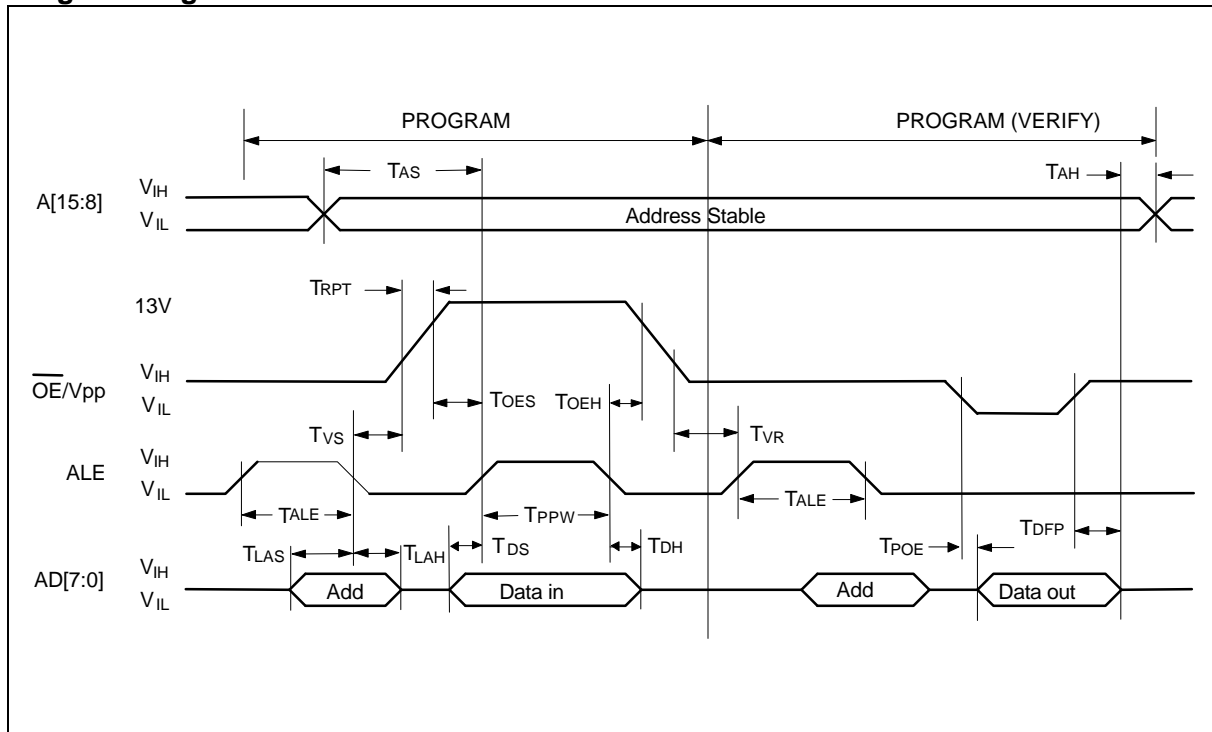
AC PROGRAMMING/ERASE CHARACTERISTICS

(V_{DD} = 6.5V ±0.25V, T_A = 25° C ±5° C)

PARAMETER	SYM.	LIMITS			UNIT
		MIN.	TYP.	MAX.	
OE /V _{PP} Pulse Rise Time	T _{PRT}	50	-	-	nS
Address Latch Enable Width	T _{ALE}	500	-	-	nS
ALE Program Pulse Width	T _{PPW}	47.5	50	52.5	μS
ALE Erase Pulse Width	T _{EPW}	95	100	105	mS
ALE Erase Pulse Width 1	T _{EPW1}	47.5	50	52.5	μS
ALE Erase Pulse Width 2	T _{EPW2}	95	100	105	mS
Latched Address Setup Time	T _{LAS}	100	-	-	nS
Latched Address Hold Time	T _{LAH}	100	-	-	nS
Address Setup Time	T _{AS}	2.0	-	-	μS
Address Hold Time	T _{AH}	0	-	-	μS
OE /V _{PP} Setup Time	T _{OES}	2.0	-	-	μS
OE /V _{PP} Hold Time	T _{OEH}	2.0	-	-	μS
Data Setup Time	T _{DS}	2.0	-	-	μS
Data Hold Time	T _{DH}	2.0	-	-	μS
Data Valid from OE /V _{PP} Low during Erase Verify	T _{EOE}	-	-	150	nS
Data Valid from OE /V _{PP} Low during Program Verify	T _{POE}	-	-	150	nS
OE /V _{PP} High to Output High Z	T _{DFP}	0	-	130	nS
OE /V _{PP} High Voltage Delay After ALE Low	T _{Vs}	2.0	-	-	μS
OE /V _{PP} Recovery Time	T _{VR}	2.0	-	-	μS

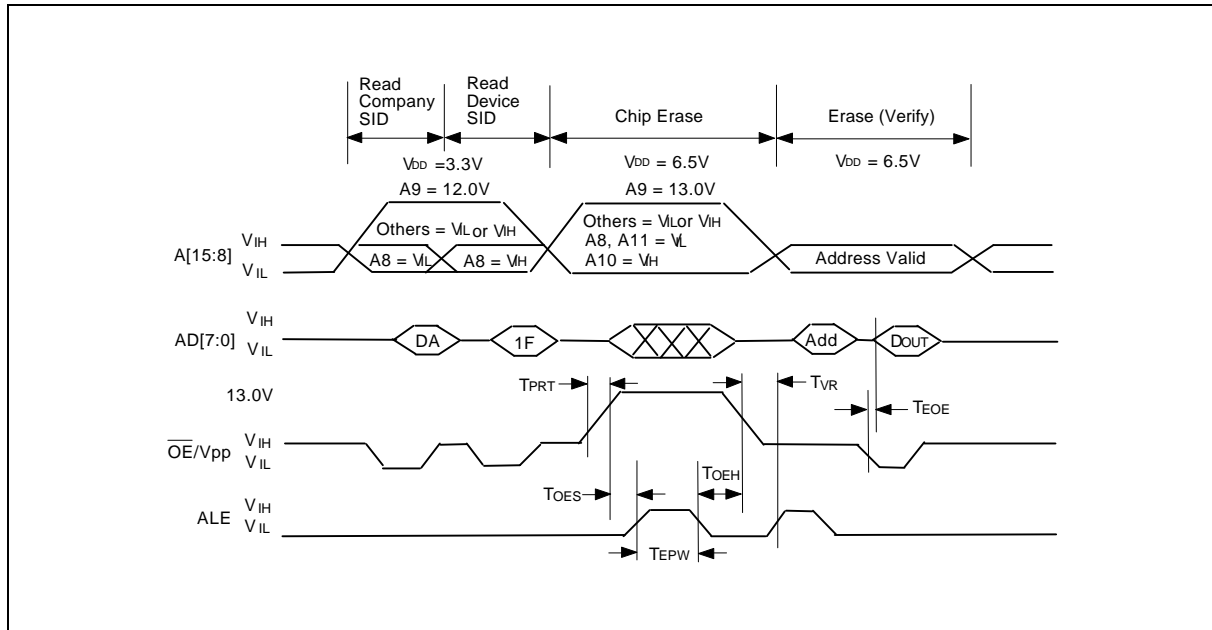
Note: V_{DD} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

AC Read Waveform

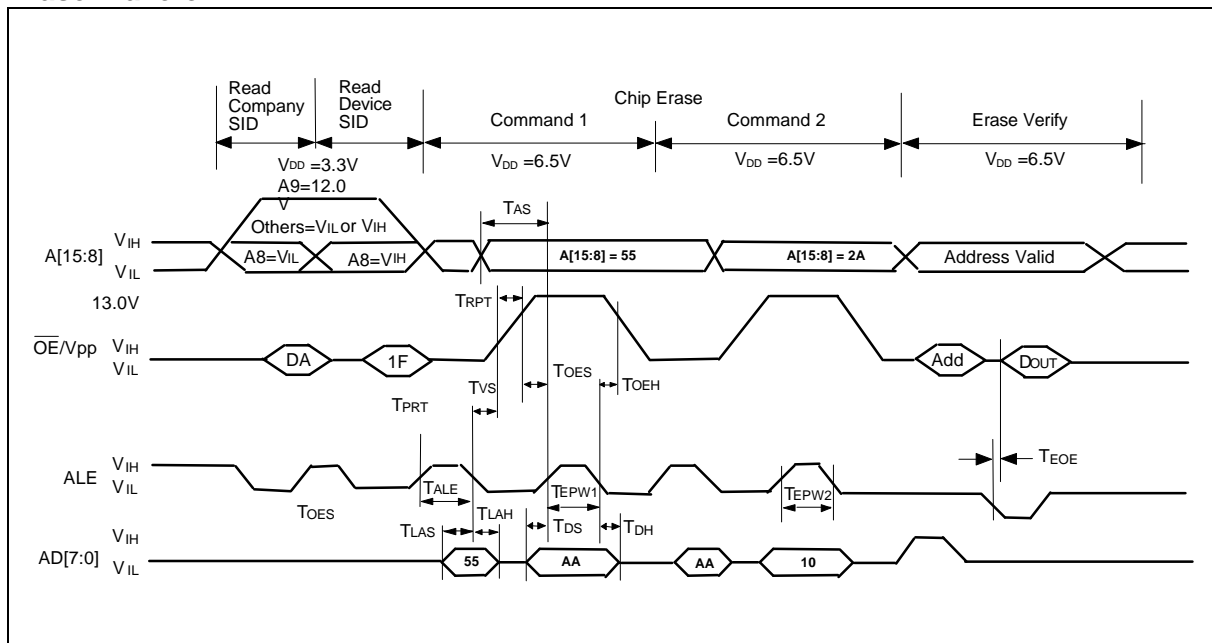


Timing Waveforms, continued

Erase Waveform 1

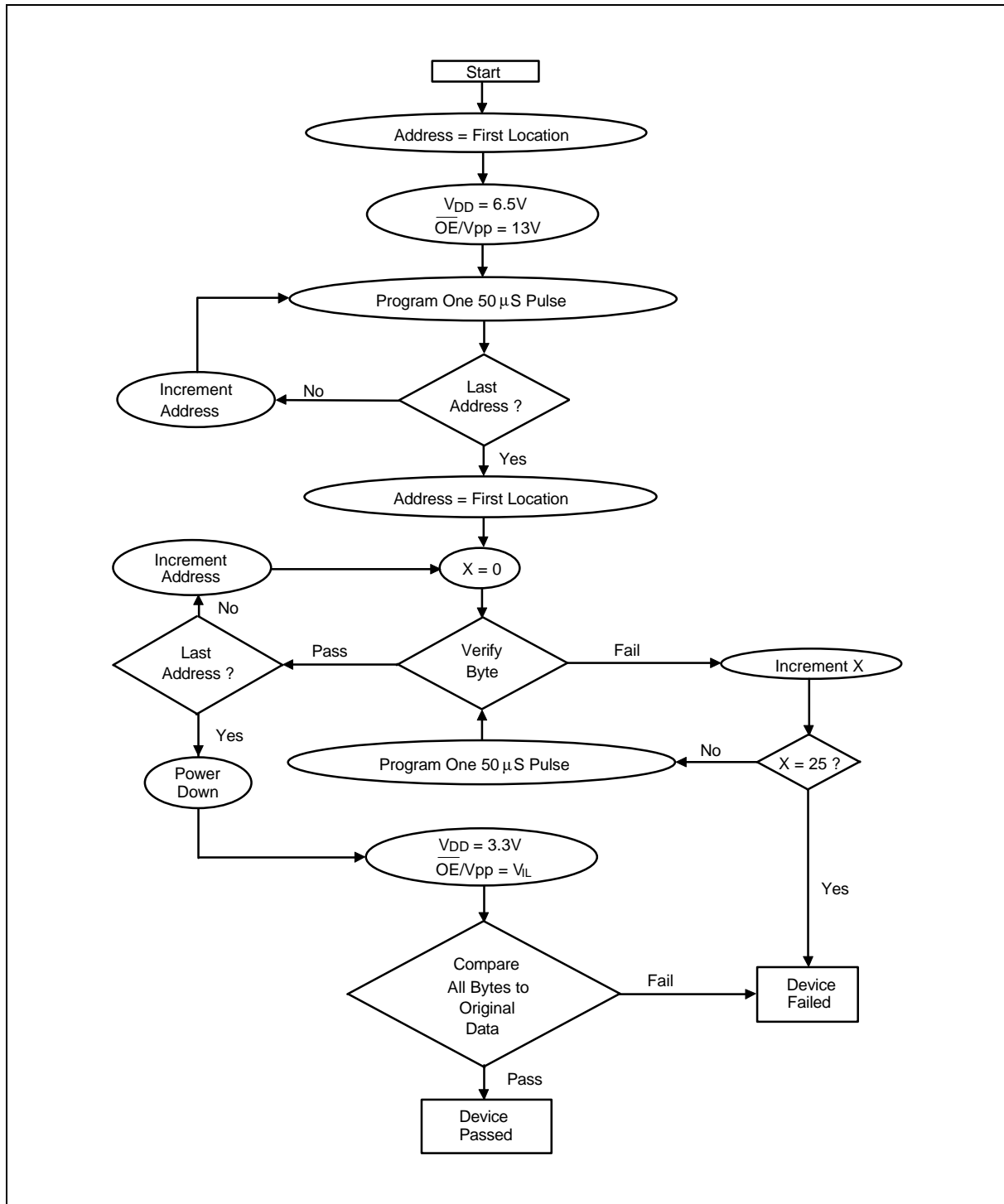


Erase Waveform 2

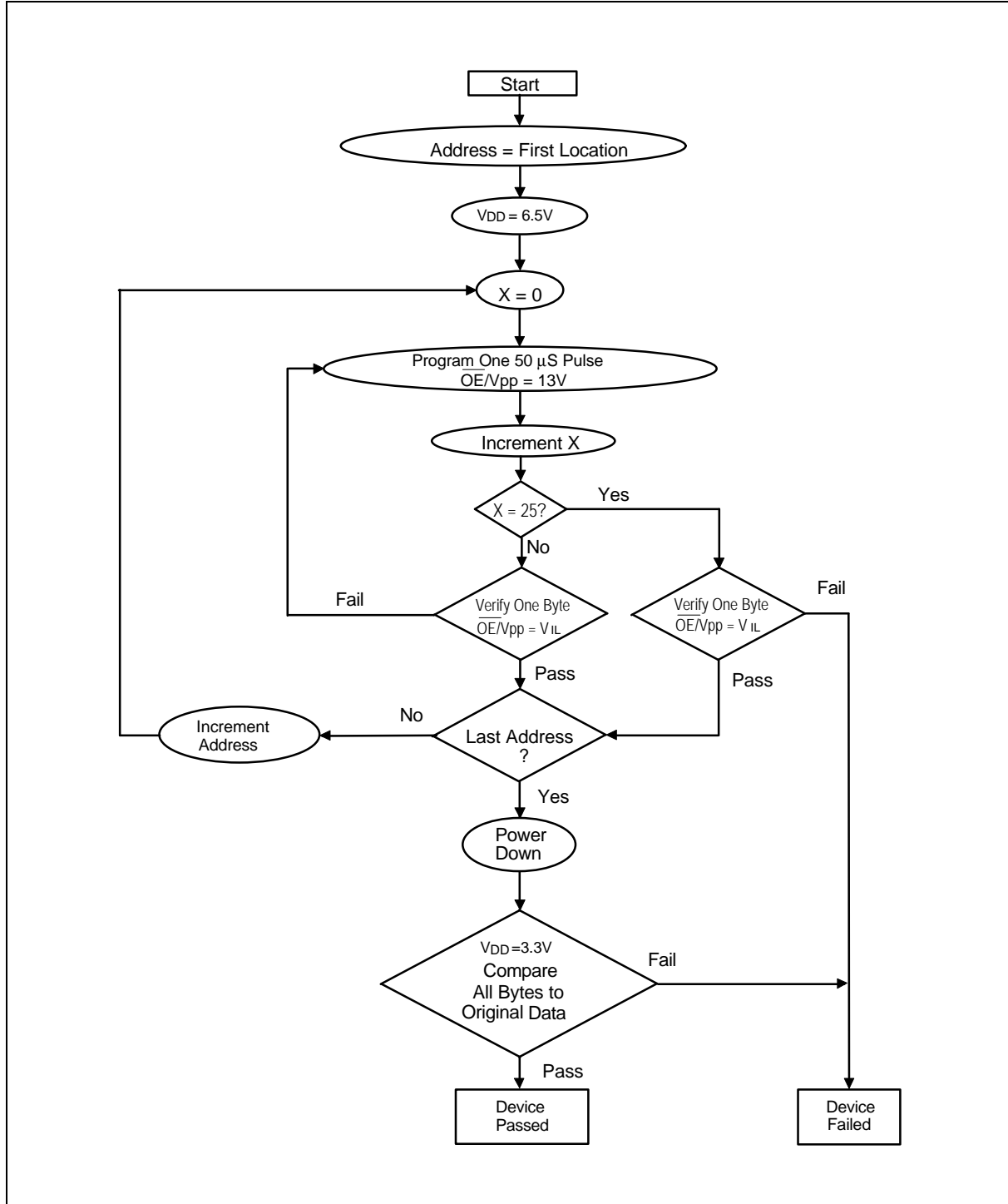


Note: First command Address = 5555(hex) with Data = AA(hex)
Second command Address = 2AAA(hex) with Data = 10(hex)

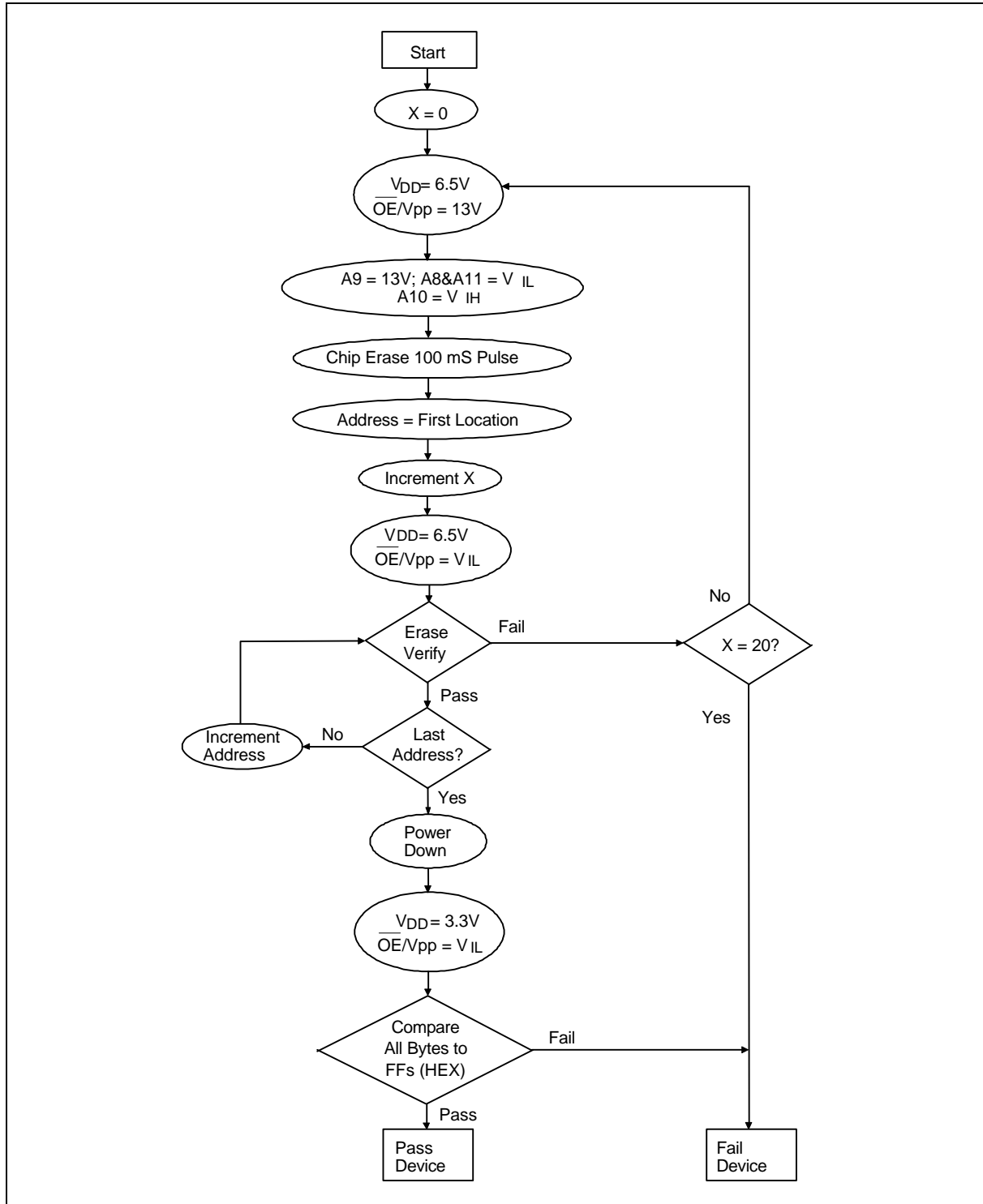
SMART PROGRAMMING ALGORITHM 1



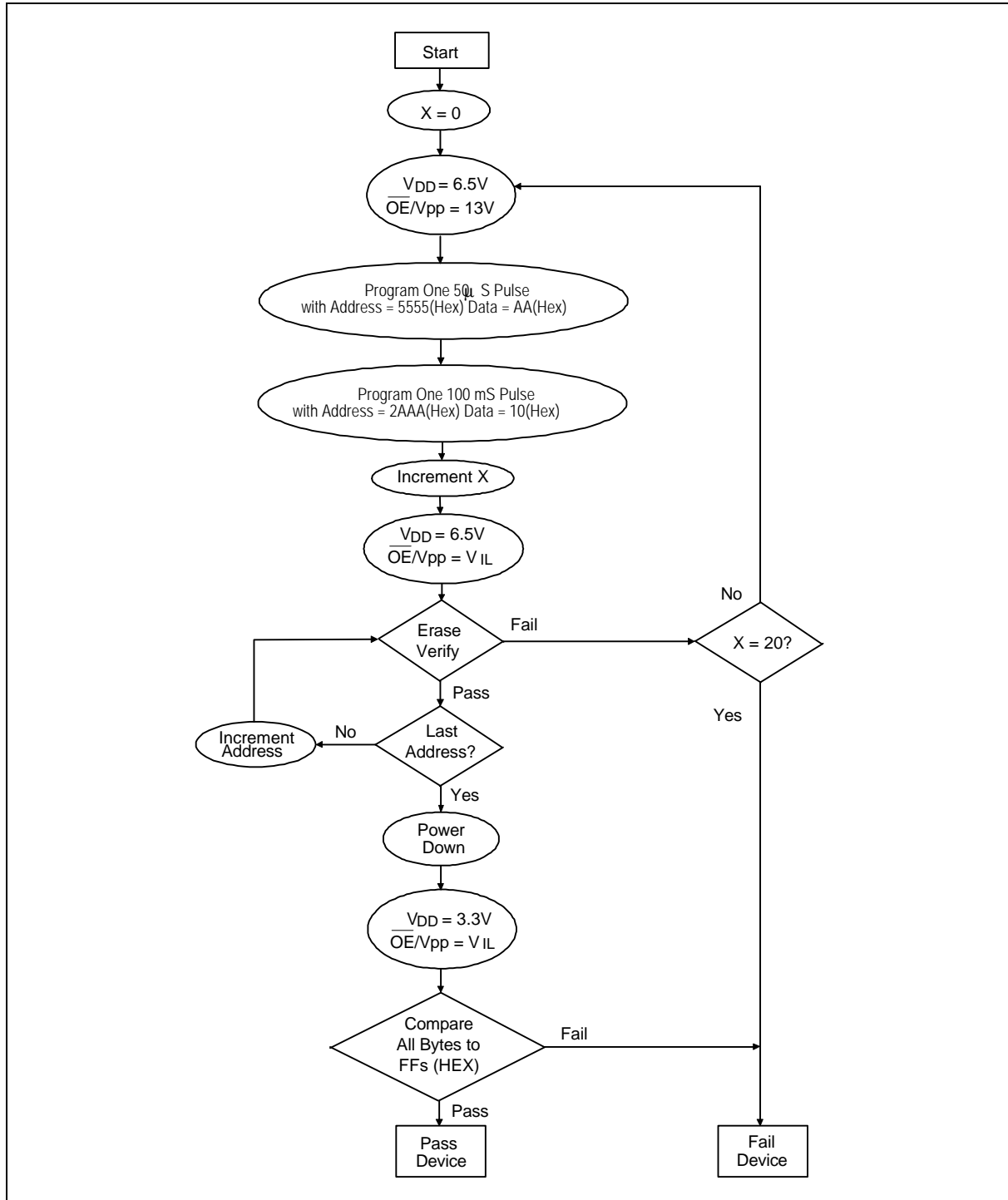
SMART PROGRAMMING ALGORITHM 2



SMART ERASE ALGORITHM 1



SMART ERASE ALGORITHM 2



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ORDERING INFORMATION

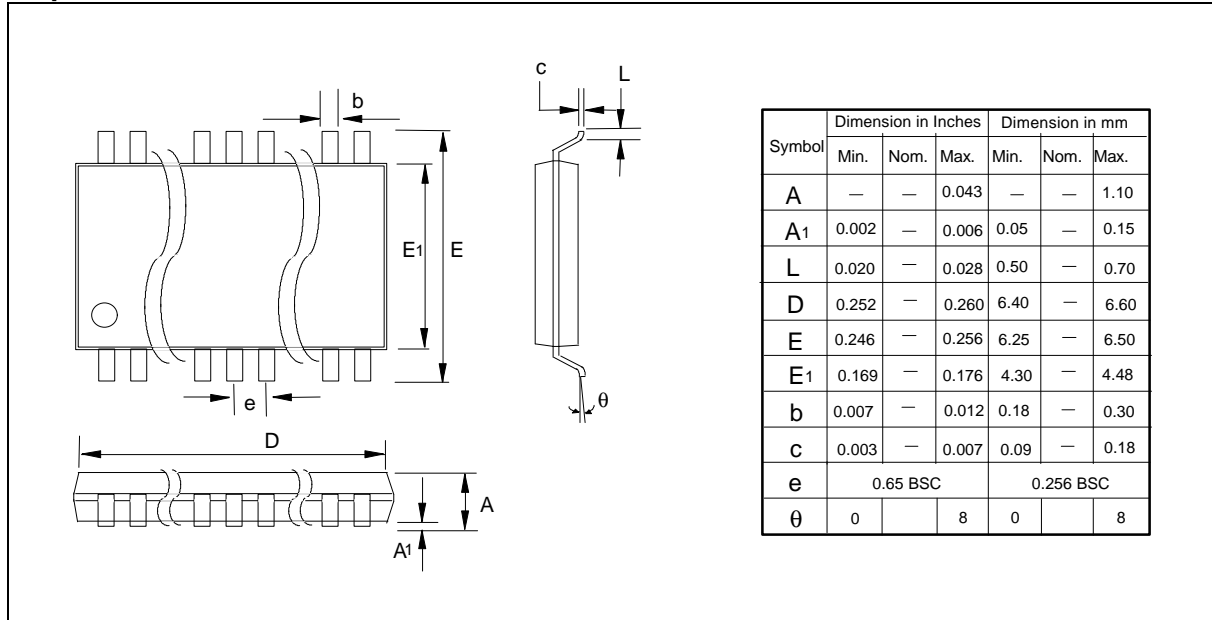
PART NO.	ACCESS TIME (nS)	OPERATING CURRENT MAX. (mA)	STANDBY CURRENT MAX. (μA)	PACKAGE
W27L520W-70*	70	8	20	173mil TSSOP
W27L520W-90*	90	8	20	173mil TSSOP
W27L520S-70*	70	8	20	300mil SOP
W27L520S-90*	90	8	20	300mil SOP

Notes:

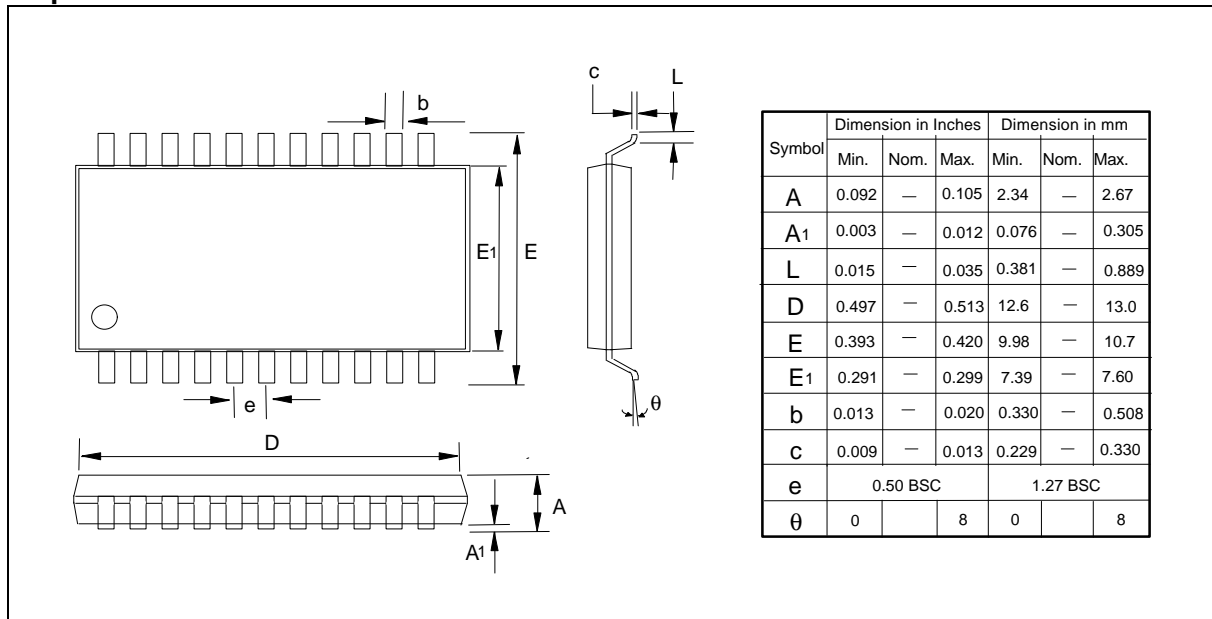
1. The Part No is preliminary and might be changed after project is consold.
2. Winbond reserves the right to make changes to its products without prior notice.
3. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

PACKAGE DIMENSIONS

20-pin TSSOP



20-pin SOP



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VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	Sep. 1999	-	Initial Issued
A2	Feb. 2000	3, 4, 9, 11	Specify VDD, VID, VCE, and VHH description
		1	Change VCC as VDD
		4	Change VCE as VDE
		6, 7, 8, 9, 10	Change VCE as VDE, VCP as VDP, VID as VHH, ICC as IDD
		1,6,14	Add 90nS bin
		1,3,6	Add in power supply range: 4.5V to 5.5V
		5	AC Test Condition: Change Input pulse level to 0V/3V; Input and Output Timing Reference Level to 1.5V/1.5V
	3/14/2000	3	Delete Two-line Output Control section
		4	Modify Storage Temperature Rating from -65 to +125°C to -65 to +150°C
		6	Modify Output Leakage Current from $\pm 10\mu\text{A}$ to $\pm 5\mu\text{A}$
	4/26/2000	1,3,6	Delete power supply range: 4.5V to 5.5V
		1	Add in ESD/Latchup information
		4	Modify DC Characteristics



Headquarters

No. 4, Creation Rd. III,
Science-Based Industrial Park,
Hsinchu, Taiwan

TEL: 886-3-5770066

FAX: 886-3-5796096

<http://www.winbond.com.tw/>

Voice & Fax-on-demand: 886-2-7197006

Taipei Office

11F, No. 115, Sec. 3, Min-Sheng East Rd.,
Taipei, Taiwan

TEL: 886-2-7190505

FAX: 886-2-7197502

Winbond Electronics (H.K.) Ltd.

Rm. 803, World Trade Square, Tower II,
123 Hoi Bun Rd., Kwun Tong,
Kowloon, Hong Kong

TEL: 852-27513100

FAX: 852-27552064

Winbond Electronics North America Corp.

Winbond Memory Lab.

Winbond Microelectronics Corp.

Winbond Systems Lab.

2727 N. First Street, San Jose,
CA 95134, U.S.A.

TEL: 408-9436666

FAX: 408-5441798

Note: All data and specifications are subject to change without notice.