



## WM2626

# Low Power Dual 8-bit Serial Input DAC with Internal Reference

Production Data, Rev. 1.0, April 2001

## FEATURES

- Dual 8-bit voltage output DAC
- Single supply from 2.7V to 5.5V
- Low power consumption:
  - 1.7mW typical (3V supply, slow mode)
  - 3.7mW typical (3V supply, fast mode)
- DNL  $\pm 0.1$  LSB, INL  $\pm 0.4$  LSB (typical)
- Monotonic over temperature
- Microprocessor and DSP compatible serial interface
- Programmable settling time of 0.8 $\mu$ s or 2.8 $\mu$ s typical
- High impedance reference input buffer

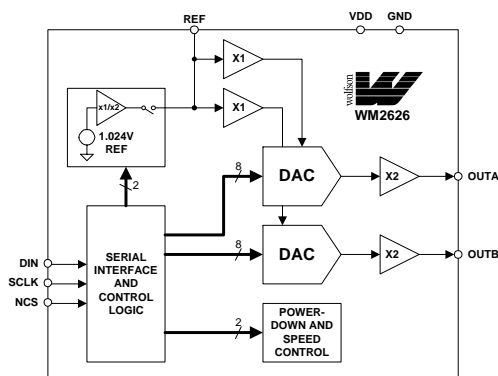
## APPLICATIONS

- Digital servo control loops
- Industrial process control
- Battery powered instruments and controls
- Machine and motion control devices
- Digital offset and gain adjustment

## ORDERING INFORMATION

DEVICE	TEMP. RANGE	PACKAGE
WM2626CD	0° to 70°C	8-pin SOIC
WM2626ID	-40° to 85°C	8-pin SOIC

## BLOCK DIAGRAM



## DESCRIPTION

The WM2626 is a dual 8-bit voltage output, resistor string digital-to-analogue converter. It can operate with supply voltages between 2.7V and 5.5V and can be powered down under software control. Power down reduces current consumption to 1 $\mu$ A.

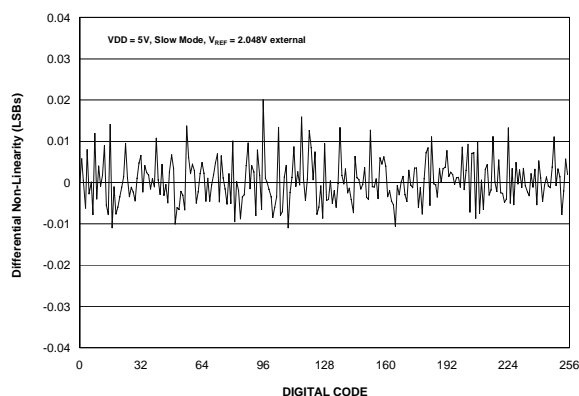
The device has been designed for glueless interface to industry standard microprocessors and DSPs. It is programmed with a 16-bit serial word including 4 control bits and 8 data bits.

Excellent performance is delivered with a typical DNL of 0.2LSBs. Monotonicity is guaranteed over the operating temperature range. The settling time of the DAC is programmable to allow for optimisation of speed versus power dissipation. The analogue output is buffered by a rail-to-rail amplifier with a gain of two and a Class AB output stage.

The on-chip voltage reference is available to external circuitry through the REF pin. It is buffered and can supply up to 1mA. Alternatively, an external reference can be used. A high impedance reference input buffer eliminates the need to keep the reference source impedance low.

The WM2626 is available in an 8-pin SOIC package. Commercial (0° to 70°C) and Industrial (-40° to 85°C) temperature range variants are available.

## TYPICAL PERFORMANCE



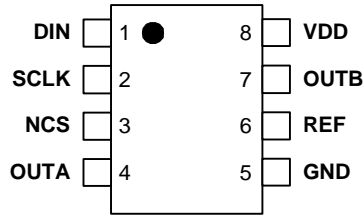
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## PIN CONFIGURATION



## PIN DESCRIPTION

PIN NO	NAME	TYPE	DESCRIPTION
1	DIN	Digital input	Serial data input
2	SCLK	Digital input	Serial clock input
3	NCS	Digital input	Chip select. This pin is active low.
4	OUTA	Digital input	DAC A analogue voltage output
5	GND	Supply	Ground
6	REF	Analogue in/out	Voltage reference
7	OUT	Analogue output	DAC B analogue voltage output
8	VDD	Supply	Positive power supply

## ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.



ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

CONDITION		MIN	MAX
Supply voltage, VDD to GND			7V
Digital input voltage		-0.3V	VDD + 0.3V
Reference input voltage		-0.3V	VDD + 0.3V
Operating temperature range, T <sub>A</sub>	WM2626CD	0°C	70°C
	WM2626ID	-40°C	85°C
Storage temperature		-65°C	150°C
Soldering lead temperature, 1.6mm (1/16 inch) from package body for 10 seconds			260°C

## RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply voltage	VDD		2.7		5.5	V
High-level digital input voltage	V <sub>IH</sub>	VDD = 2.7V to 5.5V	2			V
Low-level digital input voltage	V <sub>IL</sub>	VDD = 2.7V to 5.5V			0.8	V
Reference voltage to REF pin	V <sub>REF</sub>	See Note	GND		VDD - 1.5	V
Load resistance	R <sub>L</sub>		2			kΩ
Load capacitance	C <sub>L</sub>				100	pF
Serial clock frequency	f <sub>SCLK</sub>				20	MHz
Operating free-air temperature	T <sub>A</sub>	WM2626CD	0		70	°C
		WM2626ID	-40		85	°C

**Note:** Reference input voltages greater than VDD/2 will cause clipping for large DAC codes.

## ELECTRICAL CHARACTERISTICS

### Test Conditions:

$R_L = 10k\Omega$ ,  $C_L = 100pF$ .  $V_{DD} = 5V \pm 10\%$ ,  $V_{REF} = 2.048V$  and  $V_{DD} = 3V \pm 10\%$ ,  $V_{REF} = 1.024V$  over recommended operating free-air temperature range (unless noted otherwise).

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT		
Static DAC Specifications								
Resolution			8			bits		
Integral non-linearity	INL	End point adjusted See Note 1		±0.4	±1	LSB		
Differential non-linearity	DNL	See Note 2		±0.1	±0.5	LSB		
Zero code error	ZCE	See Note 3			±24	mV		
Gain error	GE	See Note 4			±0.6	% FSR		
D.C. power supply rejection ratio	D.C. PSRR	See Note 5		65		dB		
Zero code error temperature coefficient		See Note 6		10		ppm/°C		
Gain error temperature coefficient		See Note 6		10		ppm/°C		
DAC Output Specifications								
Output voltage range			0		VDD - 0.4	V		
Output load regulation		2kΩ to 10kΩ load See Note 7			0.25	% FS		
Power Supplies								
No load, DAC value = 128, all digital inputs 0V or VDD								
Active supply current	I <sub>DD</sub>	Internal Reference	VDD=5V	Fast		4.2	7	mA
				Slow		2	3.6	
			VDD=3V	Fast		3.7	6.3	
				Slow		1.7	3.0	
		External Reference	VDD=5V	Fast		3.8	6.3	
				Slow		1.7	3.0	
			VDD=3V	Fast		3.4	5.7	
				Slow		1.4	2.6	
Power down supply current					1		μA	
Dynamic DAC Specifications								
Slew rate	SR	R <sub>L</sub> = 10kΩ, C <sub>L</sub> = 100pF Slow Fast See Note 9			12 1.8		V/μs V/μs	
Settling time	t <sub>s</sub>	R <sub>L</sub> = 10kΩ, C <sub>L</sub> = 100pF Slow Fast See Note 10			2.8 0.8	5.5 2.4	μs μs	
Glitch energy		DIN = 0 to 1, f <sub>CLK</sub> = 100kHz, NCS = VDD			5		nV-s	
Signal to noise ratio	SNR	f <sub>s</sub> = 480kSPS, f <sub>OUT</sub> = 1kHz, R <sub>L</sub> = 10kΩ, C <sub>L</sub> = 100pF See Note 11		53	57		dB	
Signal to noise and distortion ratio	SINAD			47	48		dB	
Total harmonic distortion	THD				-50	-48	dB	
Spurious free dynamic range	SFDR			50	62		dB	

**Test Conditions:**

$R_L = 10k\Omega$ ,  $C_L = 100pF$ .  $V_{DD} = 5V \pm 10\%$ ,  $V_{REF} = 2.048V$  and  $V_{DD} = 3V \pm 10\%$ ,  $V_{REF} = 1.024V$  over recommended operating free-air temperature range (unless noted otherwise).

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Reference Output (Internal reference)</b>						
Low reference voltage	$V_{REFL}$		1.003	1.024	1.045	V
High reference voltage	$V_{REFH}$		2.027	2.048	2.069	V
Output Current	$I_{REF}$				$\pm 1$	mA
Load capacitance					100	pF
<b>Reference Input (External reference)</b>						
Reference input resistance	$R_{REFIN}$			10		M $\Omega$
Reference input capacitance	$C_{REFIN}$			5		pF
Reference feedthrough		$V_{REF} = 1V_{PP}$ at 1kHz + 1.024V dc, DAC code 0		-80		dB
Reference input bandwidth		$V_{REF} = 0.2V_{PP} + 1.024V$ dc DAC code 128 Slow Fast		0.525 1.3		MHz MHz
<b>Digital Inputs</b>						
High level input current	$I_{IH}$	Input voltage = $V_{DD}$			1	$\mu A$
Low level input current	$I_{IL}$	Input voltage = 0V	-1			$\mu A$
Input capacitance	$C_i$			8		pF

**Notes:**

1. **Integral non-linearity (INL)** is the maximum deviation of the output from the line between zero and full scale (excluding the effects of zero code and full scale errors).
2. **Differential non-linearity (DNL)** is the difference between the measured and ideal 1LSB amplitude change of any adjacent two codes. A guarantee of monotonicity means the output voltage always changes in the same direction (or remains constant) as the digital input code.
3. **Zero code error** is the voltage output when the DAC input code is zero.
4. **Gain error** is the deviation from the ideal full-scale output excluding the effects of zero code error.
5. **Power supply rejection ratio** is measured by varying  $V_{DD}$  from 4.5V to 5.5V and measuring the proportion of this signal imposed on the zero code error and the gain error.
6. **Zero code error** and **Gain error** temperature coefficients are normalised to full-scale voltage.
7. **Output load regulation** is the difference between the output voltage at full scale with a 10k $\Omega$  load and 2k $\Omega$  load. It is expressed as a percentage of the full scale output voltage with a 10k $\Omega$  load.
8.  **$I_{DD}$**  is measured while continuously writing code 128 to the DAC. For  $V_{IH} < V_{DD} - 0.7V$  and  $V_{IL} > 0.7V$  supply current will increase.
9. **Slew rate** is for an output change from 10% to 90% of full-scale output voltage, or vice versa. The results are for the lower value of the rising and falling edge slew rates.
10. **Settling time** is the time taken for the signal to settle to within 0.5LSB of the final measured value for both rising and falling edges. Limits are ensured by design and characterisation, but are not production tested.
11. **SNR**, **SNRD**, **THD** and **SPFDR** are measured on a synthesised sine wave at frequency  $f_{OUT}$  generated with a sampling frequency  $f_s$ .

## SERIAL INTERFACE

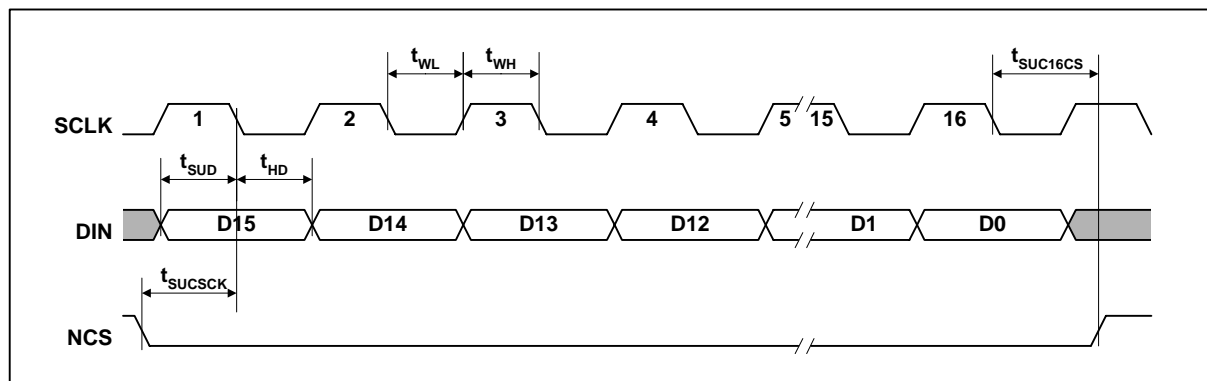


Figure 1 Timing Diagram

### Test Conditions:

$R_L = 10k\Omega$ ,  $C_L = 100pF$ .  $V_{DD} = 5V \pm 10\%$ ,  $V_{REF} = 2.048V$  and  $V_{DD} = 3V \pm 10\%$ ,  $V_{REF} = 1.024V$  over recommended operating free-air temperature range (unless noted otherwise).

SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{SUCSCK}$	Setup time, NCS low before first falling SCLK edge	10			ns
$t_{SUC16CS}$	Setup time, 16 <sup>th</sup> falling SCLK edge (when data bit D0 is sampled) before NCS rising edge.	10			ns
$t_{WH}$	Pulse duration, SCLK high.	25			ns
$t_{WL}$	Pulse duration, SCLK low.	25			ns
$t_{SUD}$	Setup time, data ready before SCLK falling edge.	10			ns
$t_{HD}$	Hold time, data held valid after SCLK falling edge.	5			ns

## TYPICAL PERFORMANCE GRAPHS

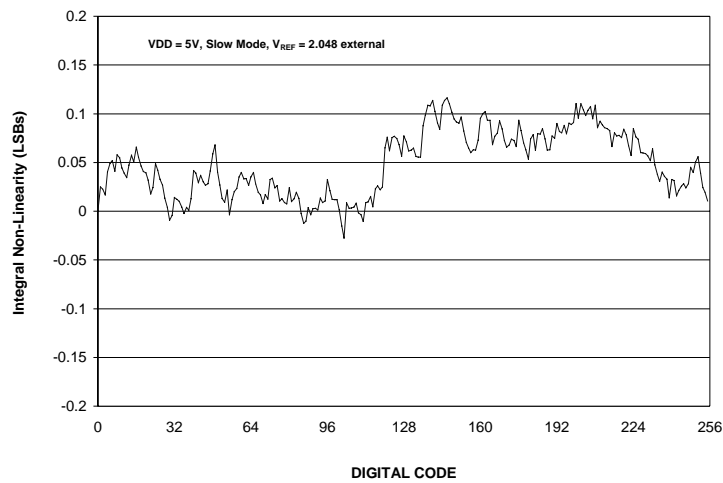


Figure 2 Integral Non-Linearity

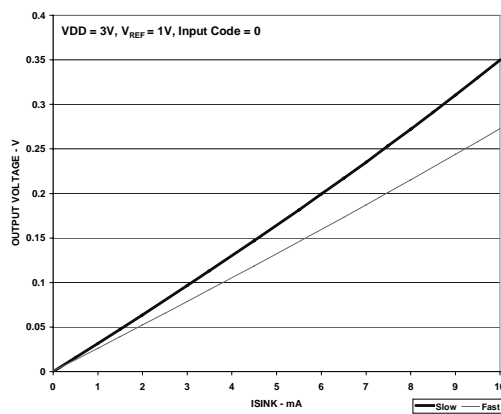


Figure 3 Sink Current VDD = 3V

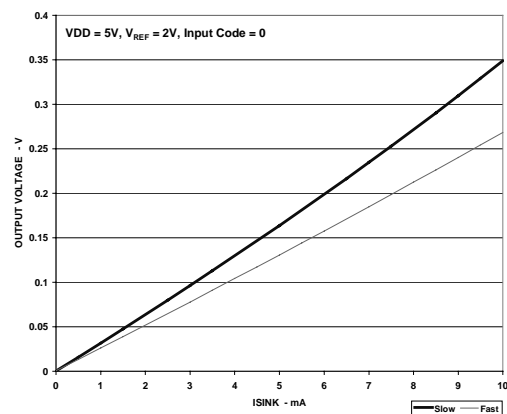


Figure 4 Sink Current VDD = 5V

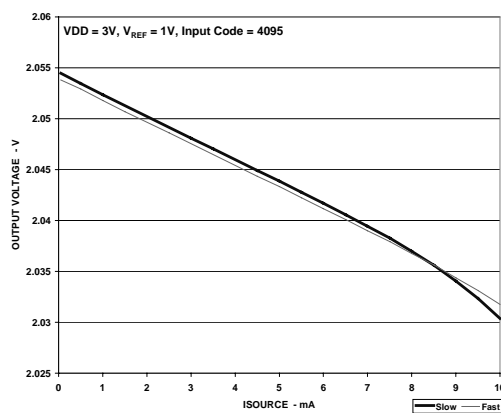


Figure 5 Source Current VDD = 3V

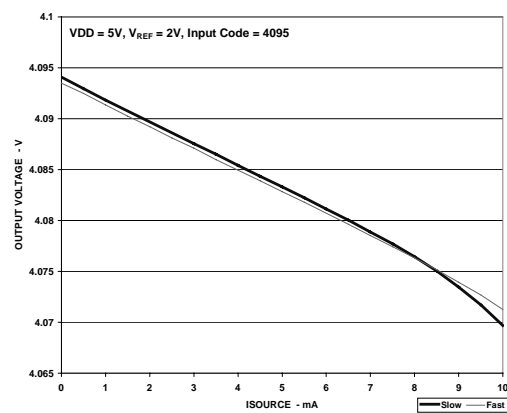


Figure 6 Source Current VDD = 5V

## DEVICE DESCRIPTION

### GENERAL FUNCTION

The WM2626 is a dual 8-bit, voltage output DAC with an on-chip voltage reference. It uses a resistor string network buffered with an op amp to convert 8-bit digital data to analogue voltage levels (see Block Diagram). The output voltage is determined by the reference voltage and the input code according to the following relationship:

$$V_{out} = 2(V_{REFIN}) \frac{CODE}{256}$$

INPUT		OUTPUT
1111	1111	$2(V_{REF}) \frac{255}{256}$
:		:
1000	0001	$2(V_{REF}) \frac{129}{256}$
1000	0000	$2(V_{REF}) \frac{128}{256} = V_{REF}$
0111	1111	$2(V_{REF}) \frac{127}{256}$
:		:
0000	0001	$2(V_{REF}) \frac{1}{256}$
0000	0000	0V

**Table 1 Binary Code Table (0V to 2V<sub>REF</sub> Output), Gain = 2**

### POWER ON RESET

An internal power-on-reset circuit resets the DAC register to all 0s on power-up.

### BUFFER AMPLIFIER

The output buffer has a near rail-to-rail output with short circuit protection and can reliably drive a 2kΩ load with a 100pF load capacitance.

## SERIAL INTERFACE

Before writing any data to the WM2626, the interface must be enabled by setting NCS to low. Incoming data on DIN (starting with the MSB) is then shifted bit-per-bit into the internal register on the falling edges of SCLK. From there data is loaded into the target latch after 16 bits have been transferred, or when NCS rises. Four internal latches can be addressed: DAC A, DAC B, the buffer latch or the control register. Their function is explained below (see 'Register Addressing').

### SERIAL CLOCK AND UPDATE RATE

Figure 1 shows the device timing. The maximum serial rate is:

$$f_{SCLK\ max} = \frac{1}{t_{WH\ min} + t_{WL\ min}} = 20MHz$$

Since a data word contains 16 bits, the sample rate for one channel is limited to

$$f_{s\ max} = \frac{1}{16 \times (t_{WH\ min} + t_{WL\ min})} = 1.25MHz$$

For full two-channel operation, where two data words need to be transmitted per sample, this figure is halved to 625kHz. However, the DAC settling time to 8-bit accuracy limits the response time of the analogue output for large input step transitions.

## SOFTWARE CONFIGURATION OPTIONS

Table 2 shows the composition of a 16-bit data word. D11-D4 contains the 8-bit data word, and D14-D13 hold the programmable options. Bits D15 and D12 are used for addressing the different latches. D3 to D0 are unused and should be set to ZERO.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R1	SPD	PWR	R0	New DAC value (8 bits)								0	0	0	0

**Table 2 Register Map**

### PROGRAMMABLE CONVERTER SPEED

SPD (Bit 14) allows for software control of the converter speed. A ONE selects the fast mode, where typical settling time to within  $\pm 0.5\text{LSB}$  of the final value is  $0.8\mu\text{s}$ . a ZERO puts the device into the slow mode, where typical settling time is  $2.8\mu\text{s}$ .

### PROGRAMMABLE POWER DOWN

The power down function is controlled by PWR (Bit 13). A ZERO configures the device as active, or fully powered up, a ONE configures the device into power down mode. When the power down function is released the device reverts to the DAC code set prior to power down.

### REGISTER ADDRESSING

Data received on the serial interface is routed according to the values of bits R1 and R0, as shown in Table 3.

R1 (BIT D15)	R0 (BIT D12)	REGISTER
0	0	Write data to DAC B and buffer
0	1	Write data to buffer
1	0	Write data to DAC A and update DAC B with buffer content
1	1	Write data to control register

**Table 3 Latch Addressing**

To update both DACs simultaneously, the data intended for DAC B should first be stored in the buffer. Subsequently, writing data to DAC A will automatically update the DAC B latch from the buffer, so that the analogue output of both DACs will change at the same time.

When updating the two channels independently, all data written to the DAC B latch (R1 and R0 set to ZERO) is also copied to the buffer. Thus the automatic update of DAC B when writing to DAC A latch (R1=1, R0=0) does not change the DAC B data. Data should not be written only to the buffer when operating in this mode.

The contents of the control register, shown below in Table 4, are used to program the internal reference function.

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
x	x	x	x	x	x	x	x	x	x	REF1	REF0

**Table 4 Control Register Contents**

### PROGRAMMABLE INTERNAL OR EXTERNAL REFERENCE

The reference can be sourced internally or externally under software control, as detailed in Table 5. If an external reference voltage is applied to the REF pin, the device must be configured to accept this. This will activate the reference input buffer, whose input resistance of  $10\text{M}\Omega$  (typical) makes the reference input resistance independent of code.

REF1	REF0	FUNCTION
0	0	Use external reference
0	1	Use internal 1.024V reference
1	0	Use internal 2.048V reference
1	1	Use external reference

**Table 5 Programmable Internal Reference**

When using the on-chip reference, voltages of 1.024V or 2.048V are available. The internal reference can source up to 1mA on the REF pin and can therefore be used as a system reference for external components.



**EXAMPLES OF OPERATION*****Simultaneous operation, slow mode:***

1. Write data for DAC B to buffer

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	New DAC B value								0	0	0	0

2. Write new DAC A value and update DAC B from buffer simultaneously

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	New DAC A value								0	0	0	0

***Independent operation, fast mode:***

Set DAC B output (fast mode):

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	New DAC B value								0	0	0	0

Set DAC A output (fast mode):

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	New DAC A value								0	0	0	0

***Select internal 2.048V reference:***

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	1	0	0	0	0	0	0	0	0	0	0	1	0

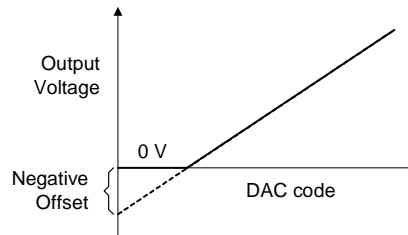
***Select external reference:***

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0

## APPLICATIONS INFORMATION

### LINEARITY, OFFSET, AND GAIN ERROR

Amplifiers operating from a single supply can have positive or negative voltage offsets. With a positive offset, the output voltage changes on the first code transition. However, if the offset is negative, the output voltage may not change with the first code, depending on the magnitude of the offset voltage. This is because with the most negative supply rail being ground, any attempt to drive the output amplifier below ground will clamp the output at 0 V. The output voltage then remains at zero until the input code is sufficiently high to overcome the negative offset voltage, resulting in the transfer function shown in Figure 7



**Figure 7 Effect of Negative Offset**

This offset error, not the linearity error, produces the breakpoint. The transfer function would follow the dotted line if the output buffer could drive below the ground rail.

DAC linearity is measured between zero-input code (all input bits at 0) and full-scale code (all inputs at 1), disregarding offset and full-scale errors. However, due to the breakpoint in the transfer function, single supply operation does not allow for adjustment when the offset is negative. In such cases, the linearity is therefore measured between full-scale and the lowest code that produces a positive (non-zero) output voltage.

### POWER SUPPLY DECOUPLING AND GROUNDING

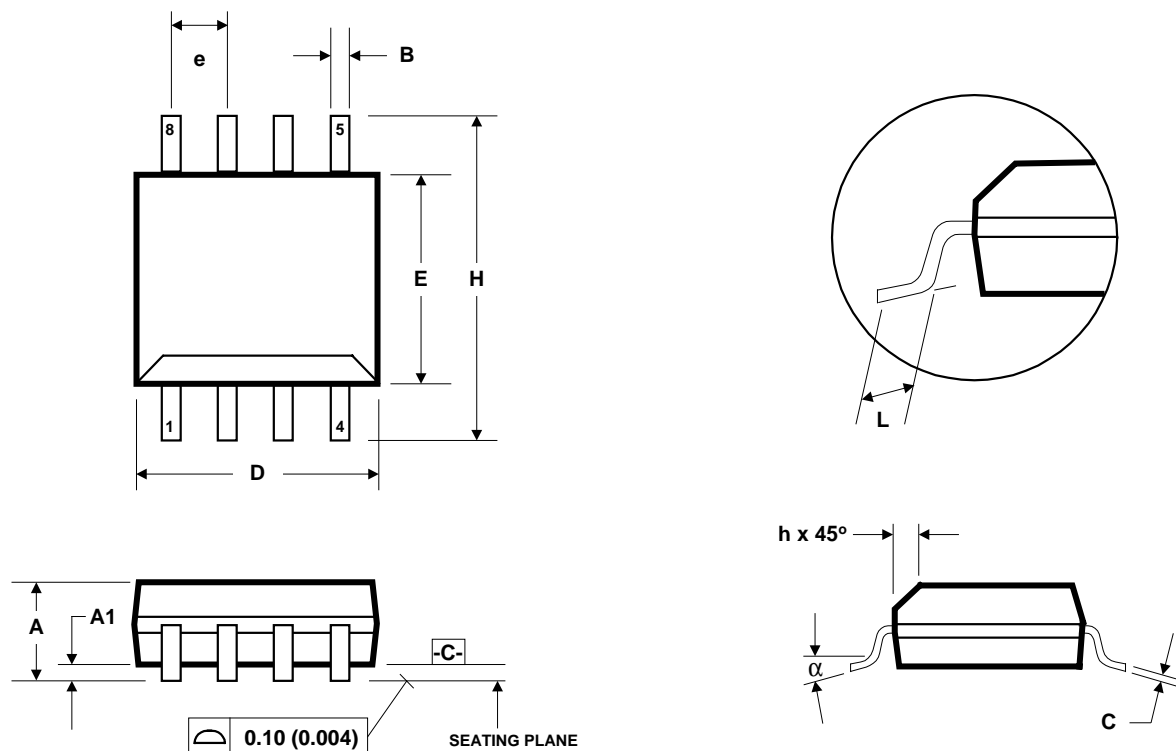
Printed circuit boards with separate analogue and digital ground planes deliver the best system performance. The two ground planes should be connected together at the low impedance power supply source. Ground currents should be managed so as to minimise voltage drops across the ground planes.

A 0.1 $\mu$ F decoupling capacitor should be connected between the positive supply and ground pins of the DAC, with short leads as close as possible to the device. Use of ferrite beads may further isolate the system analogue supply from the digital supply.

## PACKAGE DIMENSIONS

D: 8 PIN SOIC 3.9mm Wide Body

DM009.B



Symbols	Dimensions (mm)		Dimensions (Inches)	
	MIN	MAX	MIN	MAX
<b>A</b>	1.35	1.75	0.0532	0.0688
<b>A<sub>1</sub></b>	0.10	0.25	0.0040	0.0098
<b>B</b>	0.33	0.51	0.0130	0.0200
<b>C</b>	0.19	0.25	0.0075	0.0098
<b>D</b>	4.80	5.00	0.1890	0.1968
<b>e</b>	1.27 BSC		0.050 BSC	
<b>E</b>	3.80	4.00	0.1497	0.1574
<b>h</b>	0.25	0.50	0.0099	0.0196
<b>H</b>	5.80	6.20	0.2284	0.2440
<b>L</b>	0.40	1.27	0.0160	0.0500
$\alpha$	0°	8°	0°	8°
REF: JEDEC.95, MS-012				

## NOTES:

- A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS (INCHES).  
 B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.  
 C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.25MM (0.010IN).  
 D. MEETS JEDEC.95 MS-012, VARIATION = AA. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.