



WM2639

12-Bit Parallel Input Voltage Output DAC with Internal Reference

Production Data, July 1999, Rev 1.0

FEATURES

- 12-bit voltage output DAC
- Single supply 2.7V to 5.5V operation
- DNL ± 0.3 LSBs, INL ± 1.2 LSBs
- Internal programmable voltage reference
- Settling time $1\mu\text{s}$ typical
- 12-bit microprocessor compatible interface
- Power down mode 10nA

APPLICATIONS

- Battery powered test instruments
- Digital offset and gain adjustment
- Battery operated/remote industrial controls
- Machine and motion control devices
- Wireless telephone and communication systems
- Speech synthesis
- Arbitrary waveform generation
- Mass storage devices

DESCRIPTION

The WM2639 is a 12-bit voltage output, resistor string, digital-to-analogue converter. A hardware controlled power down mode is provided that reduces current consumption to 10nA. The device has been designed to interface efficiently to industry standard microprocessors and DSPs.

The WM2639 features an internal programmable voltage reference simplifying overall system design. The reference voltage can also be supplied externally.

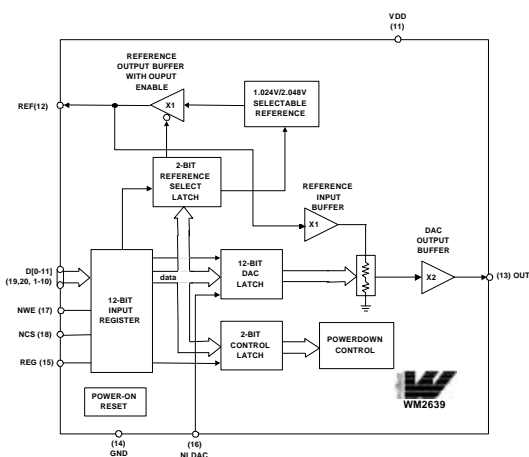
Excellent performance is delivered with a typical DNL of 0.3 LSBs and typical INL of 1.2 LSBs. The output stage is buffered by a x2 gain near rail-to-rail amplifier, which features a Class A output stage (slow mode, Class AB). The 12 data bits are double buffered enabling the output to be asynchronously updated under hardware control. The settling time of the DAC is software programmable to allow the designer to optimise speed versus power dissipation.

The device is available in a 20-pin TSSOP package. Commercial temperature (0° to 70°C) and Industrial temperature (-40° to 85°C) variants are supported.

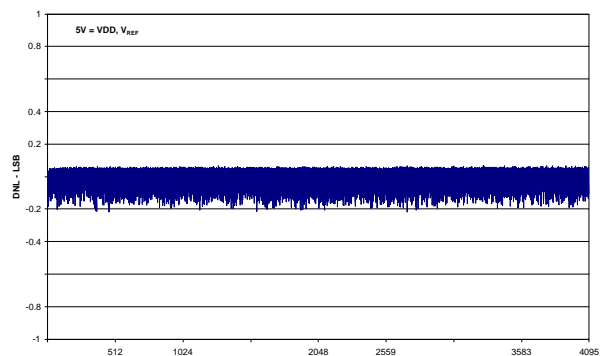
ORDERING INFORMATION

| DEVICE | TEMP. RANGE | PACKAGE |
|-----------|---------------------------------------|--------------|
| WM2639CDT | 0° to 70°C | 20-pin TSSOP |
| WM2639IDT | -40° to 85°C | 20-pin TSSOP |

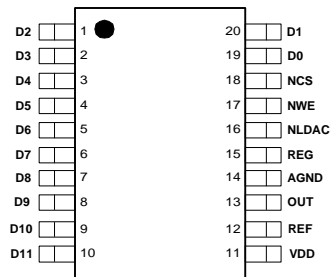
BLOCK DIAGRAM



TYPICAL PERFORMANCE



PIN CONFIGURATION



PIN DESCRIPTION

| PIN NO | NAME | TYPE | DESCRIPTION |
|--------|-------|-----------------|---|
| 1 | D2 | Digital input | Data input. |
| 2 | D3 | Digital input | Data input. |
| 3 | D4 | Digital input | Data input. |
| 4 | D5 | Digital input | Data input. |
| 5 | D6 | Digital input | Data input. |
| 6 | D7 | Digital input | Data input. |
| 7 | D8 | Digital input | Data input. |
| 8 | D9 | Digital input | Data input. |
| 9 | D10 | Digital input | Data input. |
| 10 | D11 | Digital input | Data input.(MSB) |
| 11 | VDD | Supply | Positive power supply. |
| 12 | REF | Analogue I/O | Analogue reference voltage input/output. |
| 13 | OUT | Analogue output | DAC analogue voltage output. |
| 14 | AGND | Supply | Analogue Ground. |
| 15 | REG | Digital input | Register select. Digital input used to access control register. |
| 16 | NLDAC | Digital input | Load DAC. Digital input active low. NLDAC must be taken low to update the DAC latch from the holding latches. |
| 17 | NWE | Digital input | Write enable. Digital input active low. |
| 18 | NCS | Digital input | Chip select. Digital input active low. |
| 19 | D0 | Digital input | Data input. (LSB) |
| 20 | D1 | Digital input | Data input. |

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified



ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

| CONDITION | | MIN | MAX |
|---|-----------|-------|------------|
| Digital supply voltages, VDD to GND | | | 7V |
| Reference input voltage | | -0.3V | VDD + 0.3V |
| Digital input voltage range to GND | | -0.3V | VDD + 0.3V |
| Operating temperature range, T _A | WM2639CDT | 0°C | 70°C |
| | WM2639IDT | -40°C | 85°C |
| Storage temperature | | -65°C | 150°C |
| Lead temperature 1.6mm (1/16 inch) soldering for 10 seconds | | | 260°C |

RECOMMENDED OPERATING CONDITIONS

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------------------|------------------|--------------------|-----|-----|-----------|------|
| Supply voltage | VDD | | 2.7 | | 5.5 | V |
| High-level digital input voltage | V _{IH} | VDD = 2.7V to 5.5V | 2 | | | V |
| Low-level digital input voltage | V _{IL} | VDD = 2.7V to 5.5V | | | 0.8 | V |
| Reference voltage to REF | V _{REF} | See Note | | | VDD - 1.5 | V |
| Load resistance | R _L | | 2 | | | kΩ |
| Load capacitance | C _L | | | | 100 | pF |
| Operating free-air temperature | T _A | WM2639CDT | 0 | | 70 | °C |
| | | WM2639IDT | -40 | | 85 | °C |

Note: Reference voltages greater than VDD/2 will cause output saturation for large DAC codes.

ELECTRICAL CHARACTERISTICS

Test Conditions:

$R_L = 10k\Omega$, $C_L = 100pF$. $V_{DD} = 5V \pm 10\%$, $V_{REF} = 2.048V$ and $V_{DD} = 3V \pm 10\%$, $V_{REF} = 1.024V$ over recommended operating free-air temperature range (unless noted otherwise)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|----------|--|------------|--|--|--|
| Static DAC Specifications | | | | | | |
| Resolution | | | 12 | | | bits |
| Integral non-linearity | INL | See Note 1 | | ± 1.2 | ± 3 | LSB |
| Differential non-linearity | DNL | See Note 2 | | ± 0.3 | ± 0.5 | LSB |
| Zero code error | ZCE | See Note 3 | | 3 | ± 20 | mV |
| Gain error | GE | See Note 4 | | | ± 0.3 | % FSR |
| d.c. power supply rejection ratio | DC PSRR | See Note 5 | | 0.5 | | mV/V |
| Zero code error temperature coefficient | | See Note 6 | | 20 | | ppm/ $^{\circ}C$ |
| Gain error temperature coefficient | | See Note 6 | | 20 | | ppm/ $^{\circ}C$ |
| DAC Output Specifications | | | | | | |
| Output voltage range | | | 0 | | $V_{DD} - 0.4$ | V |
| Output load regulation | | 2k Ω to 10k Ω load See Note 7 | | 0.1 | 0.3 | % |
| Power Supplies | | | | | | |
| Active supply current | I_{DD} | No load, $V_{IH} = V_{DD}$, $V_{IL} = 0V$ $V_{DD} = 5V$, $V_{REF} = 2.048V$, Internal Slow Fast $V_{DD} = 5V$, $V_{REF} = 2.048V$, External Slow Fast $V_{DD} = 3V$, $V_{REF} = 1.024V$, Internal Slow Fast $V_{DD} = 3V$, $V_{REF} = 1.024V$, External Slow Fast See Note 8 | | 1.3 2.3 0.9 1.9 1.2 2.1 0.9 1.8 | 1.6 2.8 1.2 2.4 1.5 2.6 1.1 2.3 | mA mA mA mA mA mA mA mA |
| Power down supply current | | No load, all inputs 0V or VDD See Note 9 | | 0.01 | 1 | μA |
| Dynamic DAC Specifications | | | | | | |
| Slew rate | | DAC code 32-4095, 10%-90% Slow Fast See Note 10 | 1.2 6.0 | 1.7 10 | | V/ μs V/ μs |
| Settling time | | DAC code 32-4095 Slow Fast See Note 11 | | 3.5 1 | | μs μs |
| Glitch energy | | Code 2047 to 2048 | | 5 | | nV-s |

Test Conditions:

$R_L = 10k\Omega$, $C_L = 100pF$. $V_{DD} = 5V \pm 10\%$, $V_{REF} = 2.048V$ and $V_{DD} = 3V \pm 10\%$, $V_{REF} = 1.024V$ over recommended operating free-air temperature range (unless noted otherwise)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------------------|---------------|---|-------|------------|-------|------------|
| Signal to noise ratio | SNR | $f_s = 480ksp/s$, $f_{OUT} = 1kHz$, $BW = 20kHz$, $T_A = 25^\circ C$ See Note 12 | 73 | 78 | | dB |
| Signal to noise and distortion ratio | SNRD | $f_s = 480ksp/s$, $f_{OUT} = 1kHz$, $BW = 20kHz$, $T_A = 25^\circ C$ See Note 12 | 61 | 67 | | dB |
| Total harmonic distortion | THD | $f_s = 480ksp/s$, $f_{OUT} = 1kHz$, $BW = 20kHz$, $T_A = 25^\circ C$ See Note 12 | | -69 | -62 | dB |
| Spurious free dynamic range | SPFDR | $f_s = 480ksp/s$, $f_{OUT} = 1kHz$, $BW = 20kHz$, $T_A = 25^\circ C$ See Note 12 | 63 | 74 | | dB |
| Reference configured as input | | | | | | |
| Reference input resistance | R_{REFIN} | | | 10 | | $M\Omega$ |
| Reference input capacitance | C_{REFIN} | | | 55 | | pF |
| Reference feedthrough | | $V_{REF} = 1V_{PP}$ at 1kHz + 1.024Vdc, DAC code 0 | | -60 | | dB |
| Reference input bandwidth | | $V_{REF} = 0.2V_{PP} + 1.024V$ d.c. DAC code 2048 Slow Fast | | 500 900 | | kHz kHz |
| Reference configured as output | | | | | | |
| Low reference voltage | $V_{REFOUTL}$ | | 1.003 | 1.024 | 1.045 | V |
| High reference voltage | $V_{REFOUTH}$ | $V_{DD} > 4.75V$ | 2.027 | 2.048 | 2.069 | V |
| Output source current | I_{REFSRC} | | | | 1 | mA |
| Output sink current | I_{REFSNK} | | -1 | | | mA |
| Load Capacitance | | | | | 100 | pF |
| PSRR | | | | -48 | | dB |
| Digital Inputs | | | | | | |
| High level input current | I_{IH} | Input voltage = V_{DD} | | | 1 | μA |
| Low level input current | I_{IL} | Input voltage = 0V | | | -1 | μA |
| Input capacitance | C_I | | | 8 | | pF |

Notes:

- Integral non-linearity (INL)** is the maximum deviation of the output from the line between zero and full scale (excluding the effects of zero code and full scale errors).
- Differential non-linearity (DNL)** is the difference between the measured and ideal 1LSB amplitude change of any adjacent two codes. A guarantee of monotonicity means the output voltage changes in the same direction (or remains constant) as a change in digital input code.
- Zero code error** is the voltage output when the DAC input code is zero.
- Gain error** is the deviation from the ideal full scale output excluding the effects of zero code error.
- Power supply rejection ratio** is measured by varying V_{DD} from 4.5V to 5.5V and measuring the proportion of this signal imposed on the zero code error and the gain error.
- Zero code error** and **Gain error** temperature coefficients are normalised to full scale voltage.
- Output load regulation** is the difference between the output voltage at full scale with a 10k Ω load and 2k Ω load. It is expressed as a percentage of the full scale output voltage with a 10k Ω load.
- I_{DD} is measured while continuously writing code 2048 to the DAC. For $V_{IH} < V_{DD} - 0.7V$ and $V_{IL} > 0.7V$ supply current will increase.
- Typical supply current** in power down mode is 10nA. Production test limits are wider for speed of test.
- Slew rate** results are for the lower value of the rising and falling edge slew rates.
- Settling time** is the time taken for the signal to settle to within 0.5LSB of the final measured value for both rising and falling edges. Limits are ensured by design and characterisation, but are not production tested.

12. **SNR**, **SNRD**, **THD** and **SPFDR** are measured on a synthesised sine wave at frequency f_{OUT} generated with a sampling frequency f_s .

SERIAL INTERFACE

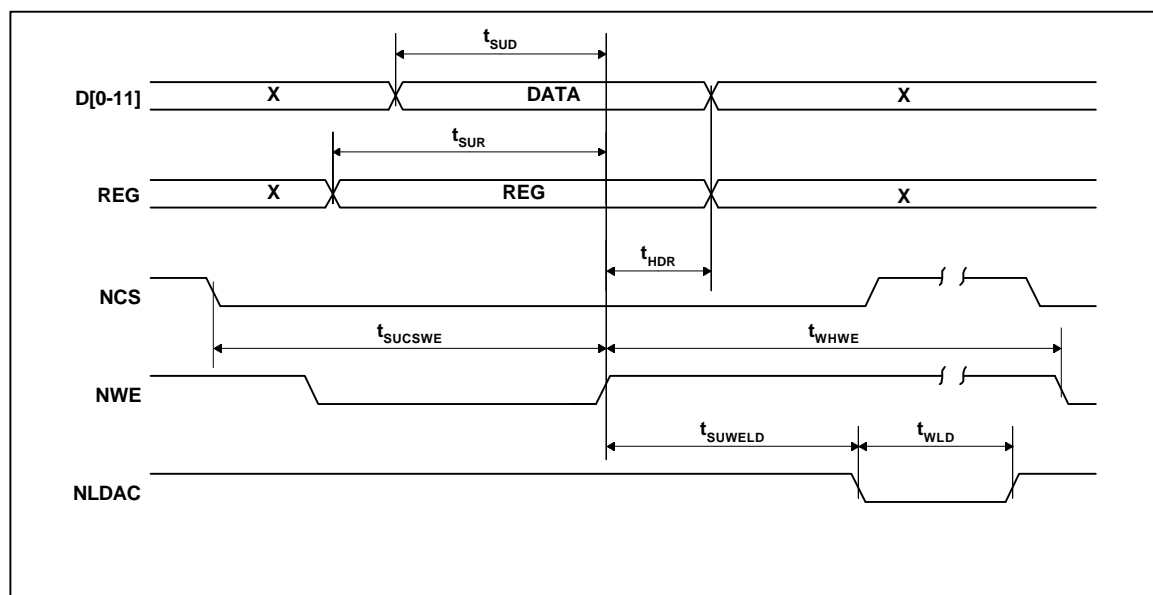


Figure 1 Timing Diagram

Test Conditions:

$R_L = 10k\Omega$, $C_L = 100pF$. $V_{DD} = 5V \pm 10\%$, $V_{REF} = 2.048V$ and $V_{DD} = 3V \pm 10\%$, $V_{REF} = 1.024V$ over recommended operating free-air temperature range (unless noted otherwise)

| SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------|--|-----|-----|-----|------|
| t_{SUCSWE} | Setup time NCS low before positive NWE edge | 15 | | | ns |
| t_{SUD} | Setup time data ready before positive NWE edge | 10 | | | ns |
| t_{SUR} | Setup time REG ready before positive NWE edge | 20 | | | ns |
| t_{HDR} | Data and REG hold after positive NWE edge | 5 | | | ns |
| t_{SUWELD} | Setup time NWE high before NLDAC low | 5 | | | ns |
| t_{WHWE} | High pulse width of NWE | 20 | | | ns |
| t_{WLD} | Low pulse width of NLDAC | 23 | | | ns |

TYPICAL PERFORMANCE GRAPHS

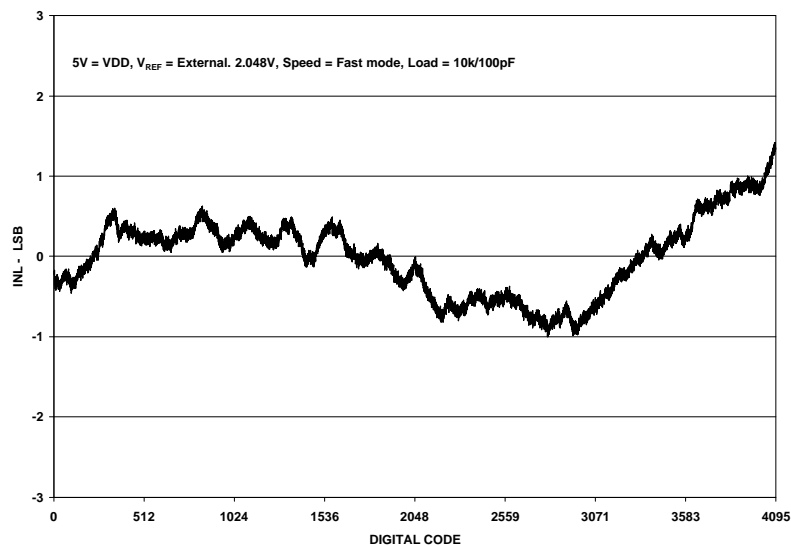


Figure 2 Integral Non-Linearity

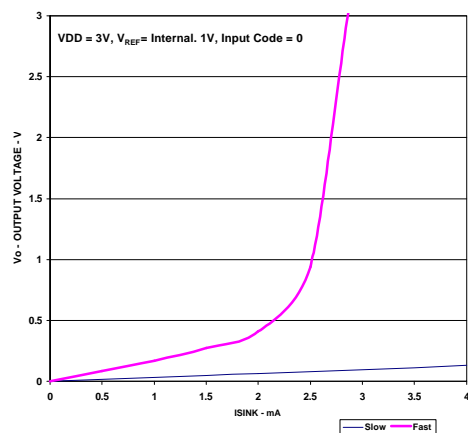


Figure 3 Sink Current VDD = 3V

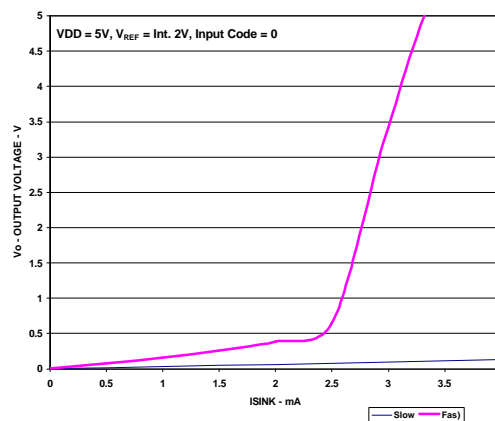


Figure 4 Sink Current VDD = 5V

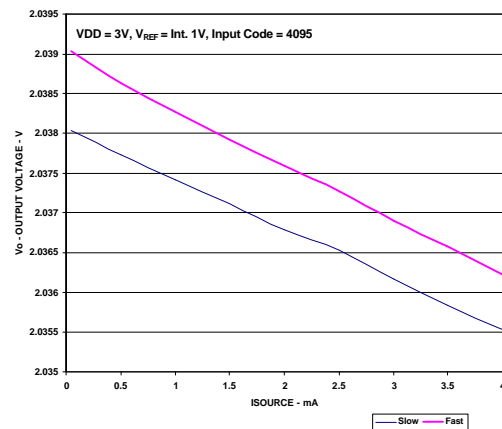


Figure 5 Source Current VDD = 3V

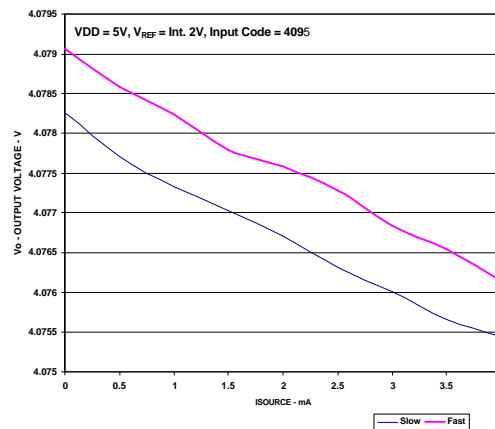


Figure 6 Source Current VDD = 5V

DEVICE DESCRIPTION

GENERAL FUNCTION

The device uses a resistor string network buffered with an op amp to convert 12-bit digital data to analogue voltage levels (see Block Diagram). The output voltage is determined by the reference input voltage and the input code according to the following relationship:

$$\text{Output voltage} = 2(V_{\text{REF}}) \frac{\text{CODE}}{4096}$$

| INPUT | | | OUTPUT |
|-------|------|------|--|
| 1111 | 1111 | 1111 | $2(V_{\text{REF}}) \frac{4095}{4096}$ |
| | : | | : |
| 1000 | 0000 | 0001 | $2(V_{\text{REF}}) \frac{2049}{4096}$ |
| 1000 | 0000 | 0000 | $2(V_{\text{REF}}) \frac{2048}{4096} = V_{\text{REF}}$ |
| 0111 | 1111 | 1111 | $2(V_{\text{REF}}) \frac{2047}{4096}$ |
| | : | | : |
| 0000 | 0000 | 0001 | $2(V_{\text{REF}}) \frac{1}{4096}$ |
| 0000 | 0000 | 0000 | 0V |

Table 1 Binary Code Table (0V to 2V_{REF} Output), Gain = 2

POWER ON RESET

An internal power-on-reset circuit resets the DAC register to all 0s on power-up.

BUFFER AMPLIFIER

The output buffer has a near rail-to-rail output with short circuit protection and can reliably drive a 2kΩ load with a 100pF load capacitance.

HARDWARE CONFIGURATION OPTIONS

The WM2639 has one configuration option that is controlled by a device pin.

DAC UPDATE

The NLDAC pin (Pin 16) can be held high to prevent word writes from updating the DAC latch. By writing the new value to the DAC then pulling NLDAC low, the new DAC code is loaded into the DAC latch.

PARALLEL INTERFACE

The device registers data on the positive edge of NWE (Pin 17). It must be enabled with NCS (Pin 18) low. Whether the data is written to the DAC holding latch or the control register, depends on the state of input pin REG (Pin 15). REG = 0 selects the DAC holding latch, REG = 1 selects the control register.

SOFTWARE CONFIGURATION OPTIONS

DATA FORMAT

The WM2639 writes data either to the DAC holding latch or to the control register depending on the state of input pin REG.

| REG (PIN 15) | DATA DESTINATION |
|-----------------|-------------------|
| 0 | DAC holding latch |
| 1 | Control register |

| D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----|-----|----|----|----|----|----|------|------|----|-----|-----|
| X | X | X | X | X | X | X | REF1 | REF0 | X | PWR | SPD |

Table 1 Register Bits

PROGRAMMABLE SETTling TIME

Settling time is a software selectable 3.5 μ s or 1 μ s, typical to within ± 0.5 LSB of final value. This is controlled by the value of SPD – Bit D0. A ONE defines a settling time of 1 μ s, a ZERO (default) defines a settling time of 3.5 μ s.

PROGRAMMABLE POWER DOWN

The power down function can be controlled by PWR. A ZERO configures the device as active, or fully powered up, a ONE configures the device into power down mode. When the power down function is released the device reverts to the DAC code set prior to power down.

PROGRAMMABLE INTERNAL REFERENCE

The reference can be sourced internally or externally under software control. If an external reference voltage is applied to the REF pin, the device must be configured to accept this.

If an external reference is selected, the reference voltage input is buffered which makes the DAC input resistance independent of code. The REF pin has an input resistance of 10M Ω and an input capacitance of typically 55pF. The reference voltage determines the DAC full-scale output.

If an internal reference is selected, a voltage of 1.024V or 2.048 is available. The internal reference can source up to 1mA and can therefore be used as an external system reference.

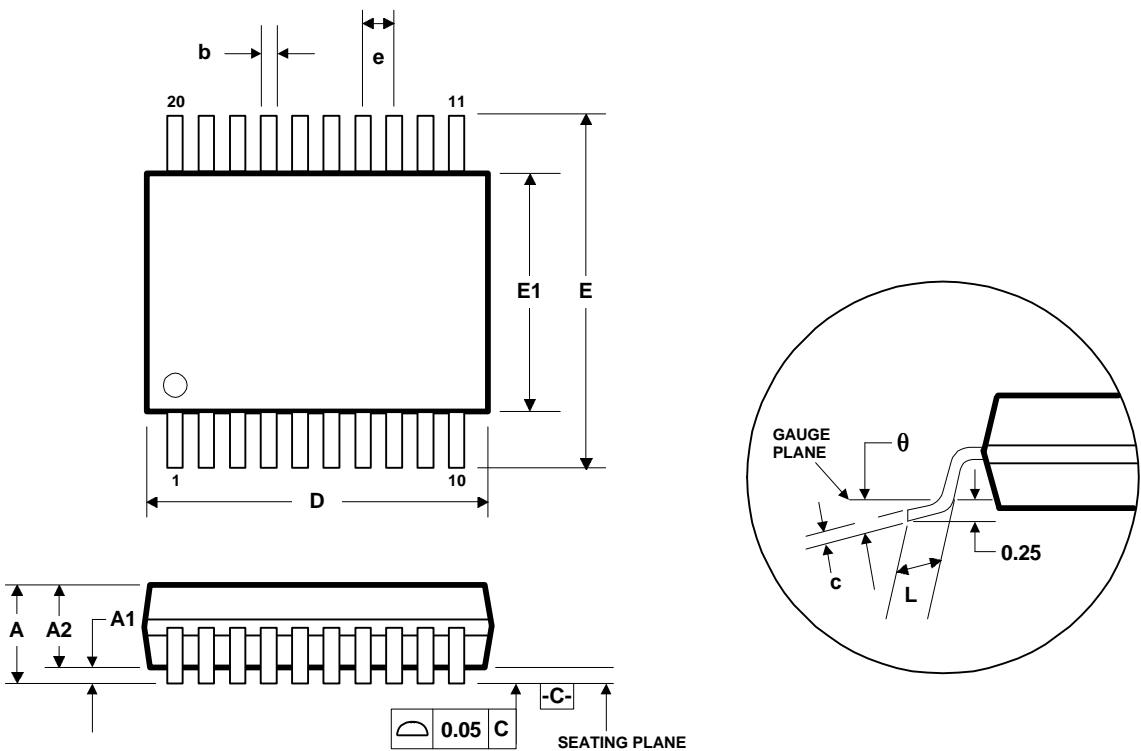
| REF1 | REF0 | REFERENCE |
|------|------|--------------------|
| 0 | 0 | External (default) |
| 0 | 1 | 1.024V |
| 1 | 0 | 2.048V |
| 1 | 1 | External |

Table 2 Programmable Internal Reference

PACKAGE DIMENSIONS

DT: 20 PIN TSSOP (6.5 x 4.4 x 1.0 mm)

DM008.C



| Symbols | Dimensions (mm) | | |
|----------------|-----------------|-------|------|
| | MIN | NOM | MAX |
| A | ----- | ----- | 1.20 |
| A ₁ | 0.05 | ----- | 0.15 |
| A ₂ | 0.80 | 1.00 | 1.05 |
| b | 0.19 | ----- | 0.30 |
| c | 0.09 | ----- | 0.20 |
| D | 6.40 | 6.50 | 6.60 |
| e | 0.65 BSC | | |
| E | 6.4 BSC | | |
| E ₁ | 4.30 | 4.40 | 4.50 |
| L | 0.45 | 0.60 | 0.75 |
| θ | 0° | | 8 |
| REF: | | | |

NOTES:
A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.
B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.25MM.
D. MEETS JEDEC.95 MO-153, VARIATION = AC. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.