Z86U18

USB DEVICE CONTROLLER WITH CMOS Z86K15 MCU

FEATURES

Device	ROM (KB)	RAM (Bytes)	I/O Lines	Speed (MHz)
Z86U18	4	188	32	6

- USB Serial Interface Engine, Transceiver, and MCU Intergrated for USB Function Controller
- +4.0V to +5.5V Operating Range
- Low Power Consumption: 60 mW @ 6 MHz
- Digital Inputs CMOS Levels with Internal Pull-Up Resistors
- Four Direct Connect LED Drive Ports
- Power-On Reset (POR), Hardware Watch-Dog Timer (WDT)
- Intergrated USB Transceiver @ 1.5 Mb/sec
- For Use In A Variety of Applications Including Keyboards and Game Controllers
- Programmable 8-Bit Counter/Timer, with 6-Bit Programmable Prescaler
- Five Vectored, Priority Interrupts from Five Different Sources
- On-Chip Oscillator, Which Accepts A Crystal, Ceramic Resonator, LC or External Clock Drive (all clock speeds @ 6 MHz)
- Low System EMI Emission
- HALT/STOP Modes

GENERAL DESCRIPTION

The Z86U18 USB Controller is a member of the Z8® MCU family. The Z86U18 is characterized by a flexible I/O scheme, an efficient register architecture, and a number of ancillary features. It contains a dedicated USB interface (transceiver and SIE).

For applications demanding powerful I/O capabilities, the Z86U18 (40- and 44-pin versions) provides 32 pins dedicated to application input and output. These lines are grouped into four ports, each port consists of eight lines and are configurable under software control to provide timing, status signals, and serial or parallel I/O ports. It also has 2 pins to connect directly to the USB cable.

To unburden the system from coping with real-time tasks, such as counting/timing and I/O data communications, the Z86U18 offers an on-chip counter/timer with a large number of user-selectable modes.

The Z86U18 achieves low EMI by means of several circuit implementations in the output drivers and clock circuitry of the device.

With fast execution, efficient use of memory, sophisticated interrupt, input/output bit-manipulation capabilities, and easy hardware/software system expansion, along with low cost and low power consumption, the Z86U18 meets the needs of a variety of sophisticated applications (Figure 1: Functional Block Diagram)

Notes: All signals with a preceding front slash, "/", are active Low. For example, B//W (WORD is active Low); /B/W (BYTE is active Low, only).

GENERAL DESCRIPTION (Continued)

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

This device is based on the Z86K15 device with the following changes or modifications:

1. **Power-On Reset** (POR): POR timing is a function of the system clock.

   $POR = (3^2 * 2^{16})/f = .098$

   POR is in seconds and frequency in Hz. It may need a programmable timer for warm reset (USB reset).

2. **Watch-Dog Timer** (WDT): WDT is also driven by the system clock and subject to same tolerance. The WDT can be programmed for time out value of:

   WDT = POR/2

3. **EMI, 801-2 and 801-4 Compliance**: When used with good engineering practice, this device should meet Class B FCC with at least 10 dB of margin and comply with the 801-2 group 4 air discharge. It shall meet 801-4 EFT requirements in a system.

4. **XTAL**: Drive to 3-pin ceramic resonator (@ 6 MHz).

5. **XTAL In**: From ceramic resonator or crystal.

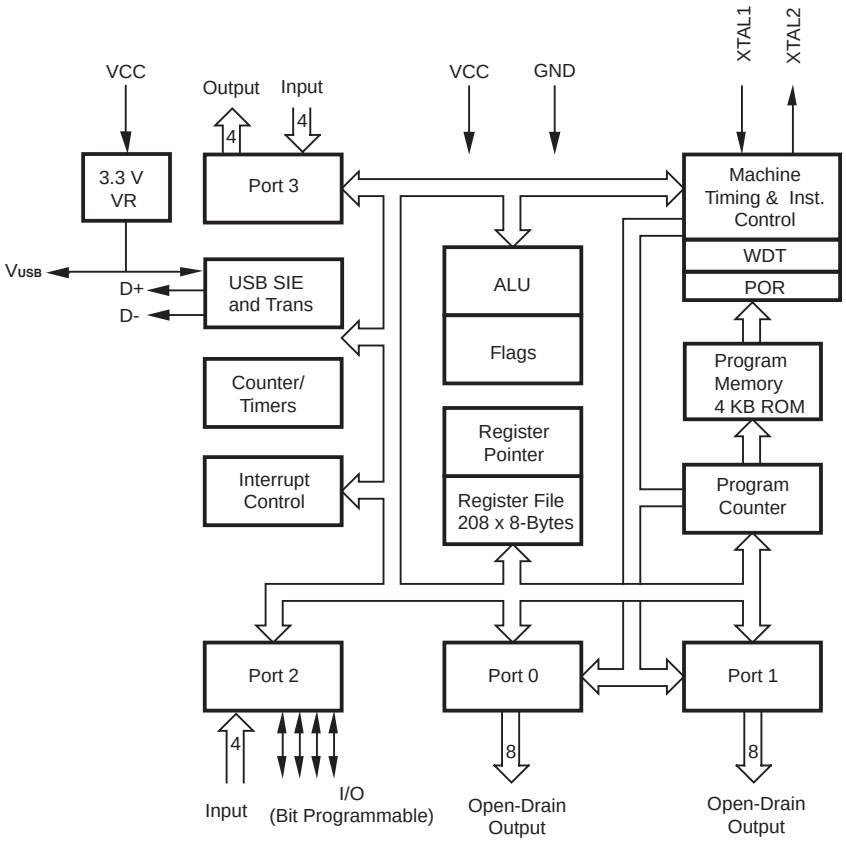


Figure 1. Z86U18 Functional Block Diagram

USB FUNCTIONAL BLOCK DESCRIPTION

The USB portion of the chip is divided into two areas, the transceiver and the Serial Interface Engine (SIE). The transceiver handles incoming differential signals and "single ended zero" (SE0). It also converts output data in digital form to differential drive at the proper levels.

The SIE does all other processing on incoming and out going data. This includes signal recovery timing, bit stuffing, validity checking, data sequencing, and handshaking to the host. Data flow into and out of the MCU portions is processed through eight registers mapped into Expanded Register File Memory at locations 010 to 017.

The USB SIE handles two endpoints (control at Endpoint 0 and data into the host from Endpoint 1). All communications are at the 1.5 Mb/sec HID class data rate. Future devices will handle the full 12 Mb/sec data rate.

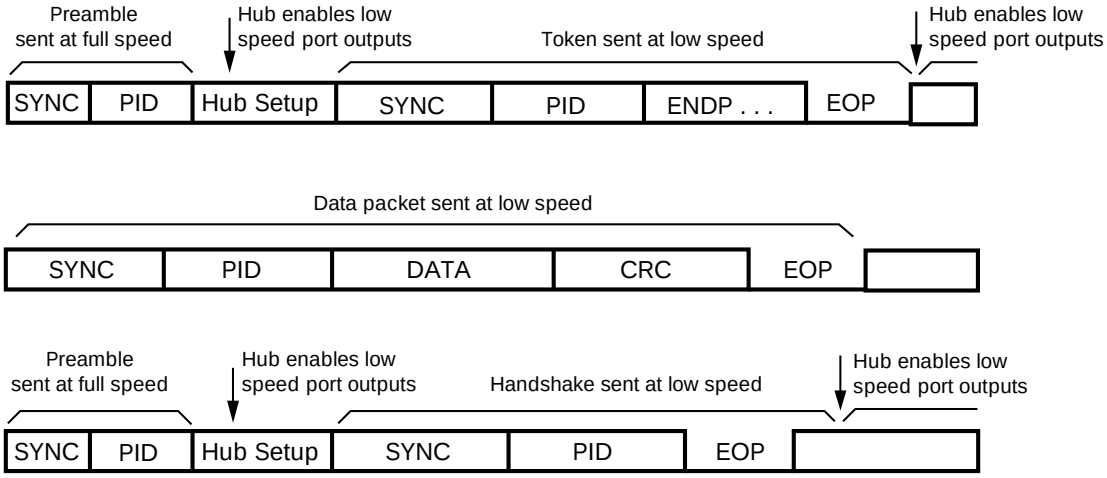


Figure 2. Data To/From K86U18

USB SUSPEND/RESUME FUNCTIONALITY

Suspend is intitiated by the host only, when it stops sending start of frame signaling or start of frame keep alive pulse.

When SIE detects the absence of start of frame signaling from the host for more than 3 miliseconds, it sets the Suspend bit in Reg7 and the Supspend Interrupt bit in Reg6 which interrupts the microcontroller. There is also an internal Suspend node that reflects the state of the Suspend bit in Reg7. This Suspend node is used to put the tranceiver in Suspend mode. When the microcontroller gets the Suspend Interrupt, it stops all the clocks.

Resume can be initiated by host or by UC. Host initiates Resume by sending J to K transition on D+ and D- pins. Upon detecting J to K transition, the GFI makes Resumeout signal active, which is used to wake the UC. Once the UC is up, it clears the suspend bit in Reg7. UC can initiate Resume by writing 1 to Send Resume bit in Reg7 for longer than 10mSec. This makes GFI to send J to K transition on D+ and D- pins which indicates to the host the Resume state. After 10 msec UC also clears the Suspend bit in Reg7.

U18 EMULATIONS AND CODE DEVELOPMENT

An existing ICEBOX™ Emulator has been modified by the addition of an adaptor board. This board includes a FPGA with the logic of the SIE, a commercial USB transceiver, and a voltage regulator. These three functions adapt our Z86C15/K15 to the USB world allowing the customer to develop code to be placed into the ROM of U18s.

The ICEBOX has complete functional equivalence to the final part including pin out to the application board. This begins with the 40-pin DIP and covers the other pin configurations. Once code has been verified, it can be released to Zilog and placed into the ROM of the Z86U18.

PIN IDENTIFICATION

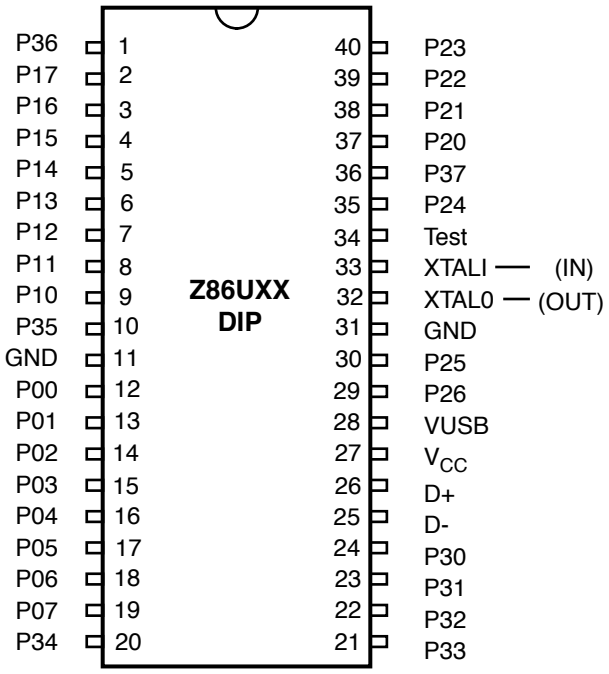
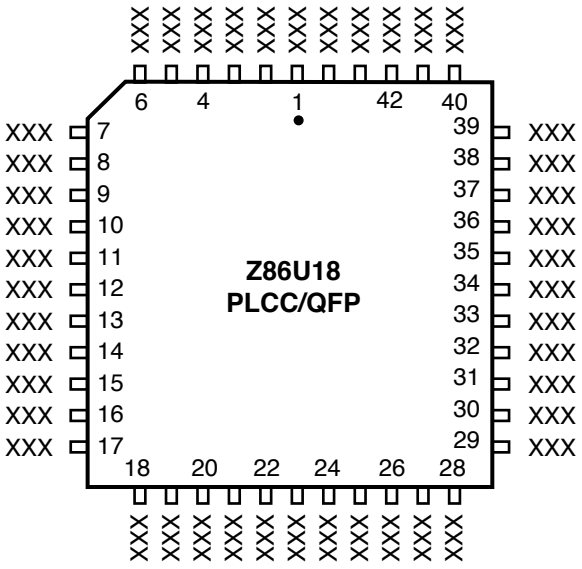
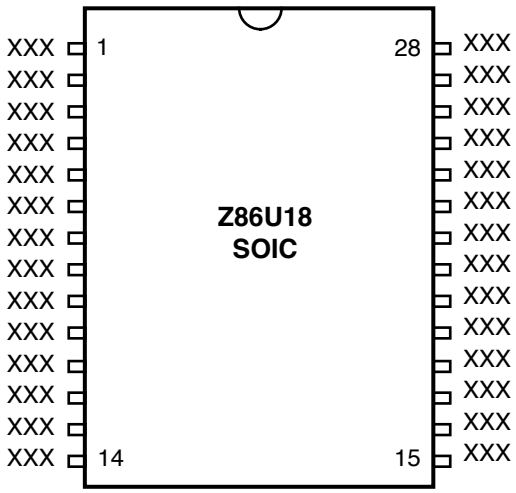


Figure 3. 40-Pin DIP Pin Configuration



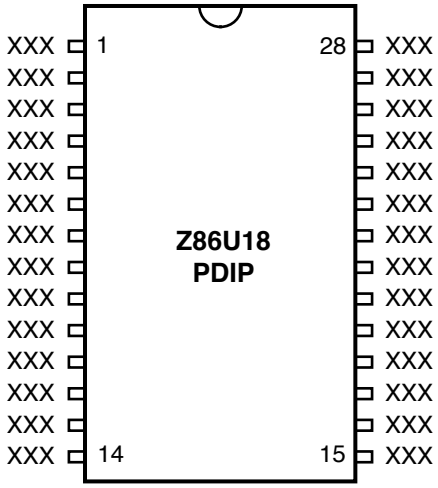
Pin assignments to be determined.

Figure 4. 44-Pin PLCC and QFP Pin Assignments



Pin assignments to be determined.

Figure 5. 28-pin SOIC Assignments



Pin assignments to be determined.

Figure 6. 28-pin PDIP Assignments

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage*	–0.3	+7.0	V
T_{STG}	Storage Temp	–65	+150	°C
T_A	Oper Ambient Temp	0	+105	°C

Note: * Voltage on all pins with respect to GND.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed here apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Figure 7).

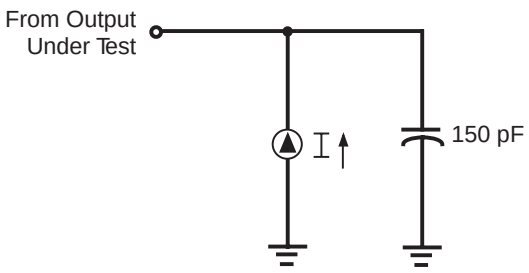


Figure 7. Test Load Diagram

CAPACITANCE

T_A = 25°C; V_{CC} = GND = 0V; f = 1.0 MHz; unmeasured pins returned to GND.

Parameter	Max
Input Capacitance	12 pF
Output Capacitance	12 pF
I/O Capacitance	12 pF

Note: Frequency tolerance ±10%

DC CHARACTERISTICS

V_{CC} = 4.0V to 5.5V @ 0°C to +70°C

Sym	Parameter	Min	Max	Unit	Condition
V_{CH}	Clock Input High Voltage	0.7 V_{CC}	V_{CC} + 0.3V	V	Driven by External Clock Generator
V_{CL}	Clock Input Low Voltage	GND –0.3	0.2 V_{CC}	V	Driven by External Clock Generator
V_{IH}	Input High Voltage	0.7 V_{CC}	V_{CC} + 0.3	V	
V_{IL}	Input Low Voltage	GND –0.3	0.2 V_{CC}	V	
V_{OH}	Output High Voltage	V_{CC} –0.4		V	I_{OH} = –2.0 mA
V_{OH}	Output High Voltage	V_{CC} –0.6		V	I_{OH} = –2.0 mA (see note 1 below.)
V_{OL}	Output Low Voltage		.4	V	I_{OL}= 4 mA
V_{OL}	Output Low Voltage		.8	V	I_{OL}= 4 mA (see note 1 below.)
I_{OL}	Output Low	10	20	mA	V_{OL}= V_{CC} –2.2 V (see note 1 below.)
I_{OL}	Output Leakage	–1	1	µA	V_{IN} = 0V, 5.25V
I_{CC}	V_{CC} Supply Current		12	mA	@ 6.0 MHz
I_{CC1}	Halt Mode Current		TBD	mA	@ 6.0 MHz
I_{CC2}	Stop Mode Current		10	µA	
R_p	Pull Up Resistor	6.76	14.04	K ohm	
R_p	Pull Up Resistor (P26-P25)	1.8	3	K ohm	
V_{USB}	Voltage Regulator Output	3.0	3.6	V	
D+,D-	Differential Signaling	D- > D+	D+ > D-	mV	@ > 200mV Difference (see note 2 below)

Notes:

1. Ports P37-P34. These may be used for LEDs or as general-purpose outputs requiring high sink current.
2. Except for SE0 for EOP and RESET (See 7.1.4 of USB Specification).

AC ELECTRICAL CHARACTERISTICS

Additional Timing Diagram

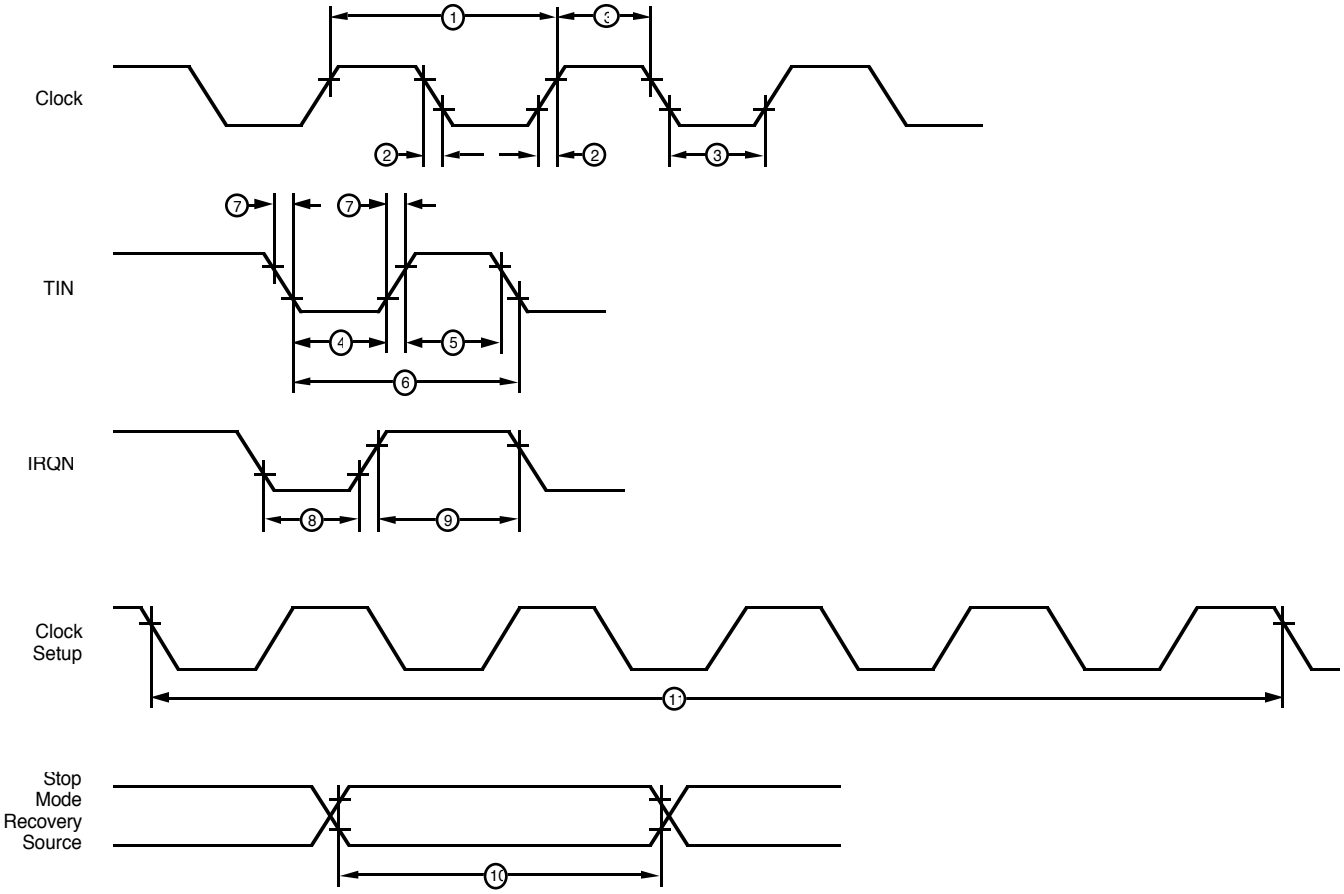


Figure 8. Additional Timing

AC ELECTRICAL CHARACTERISTICS

Additional Timing Table

			T_A=0°C to +70°C 5.0V, 6 MHz			
No	**Symbol**	**Parameter**	**Min**	**Max**	**Units**	**Notes**
1	TpC	Input Clock Period	150	250	ns	1
2	TrC,TfC	Clock Input Rise & Fall Times		25	ns	1
3	TwC	Input Clock Width	37		ns	1
4	TwTinL	Timer Input Low Width	70		ns	1
5	TwTinH	Timer Input High Width	2.5TpC			1
6	TpTin	Timer Input Period	4TpC			1
7	TrTin	Timer Input Rise & Fall Timer		100	ns	1
8	TwIL	Int. Request Low Time	70		ns	1,2
9	TwIH	Int. Request Input High Time	3TpC			1,2
10	Twsm	Stop-Mode Recovery Width Spec	5TpC		ns	
11	Tost	Oscillator Start-up Time		5TpC	ns	
12	Twdt	Watch-Dog Timer	3,0		ms	
13	D+, D-	Differential Rise and Fall Times	70	300	nS	3

Notes:

1. Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.
2. Interrupt request through Port 3 (P33-P31)
3. See USB Specification 7.1.1.2

PIN FUNCTIONS

XTAL 1,2 for ceramic resonator operation (6 MHz)**.**

Port 0 (P07-P00) and **Port 1** (P17-P10). Port 0 and Port 1 are 8-bit open drain output (Figure 9).

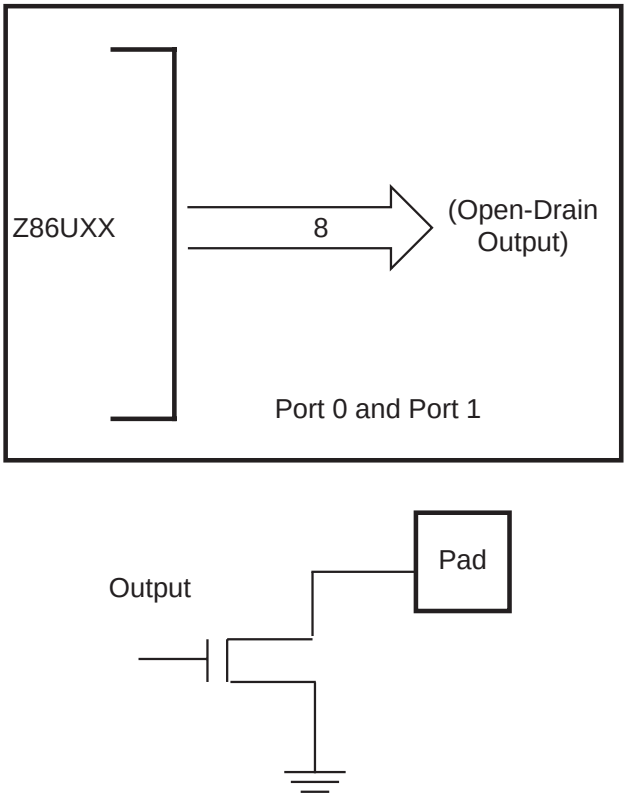


Figure 9. Port 0 and Port 1 Configuration

Port 2 (P27-P20). Port 2 is an 8-bit CMOS-compatible Port with 4-bit input, 4-bit programmable I/O (Figure 10). P20-P24 have 10.4 K (±35 percent) pull-up resistors. P25 and P26 have 2.4 K (±25 percent) pull-up resistor.

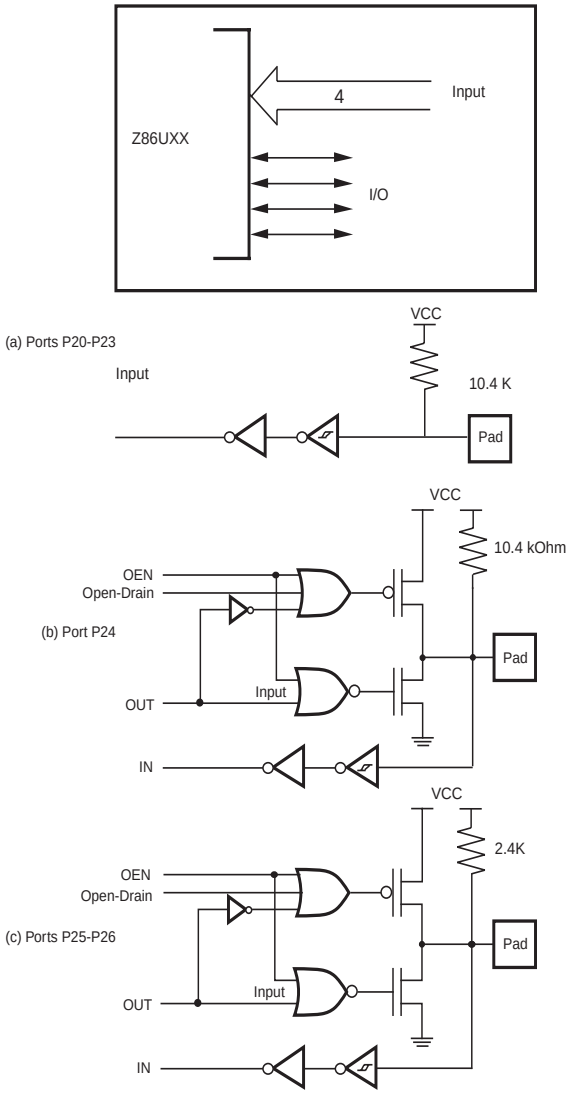


Figure 10. Port 2 Configuration

PIN FUNCTIONS (Continued)

Port 3 (P37-P30). Port 3 is an 8-bit, CMOS-compatible four-fixed-input (P33-P30) and four-fixed-output (P37-P34) I/O port. Port 3 inputs have 10.4 Kohm pull-up resistors and outputs are capable of directly driving LED.

Port 3 is configured under software control to provide the following control functions: three external interrupt request signals (IRQ0-IRQ2)..

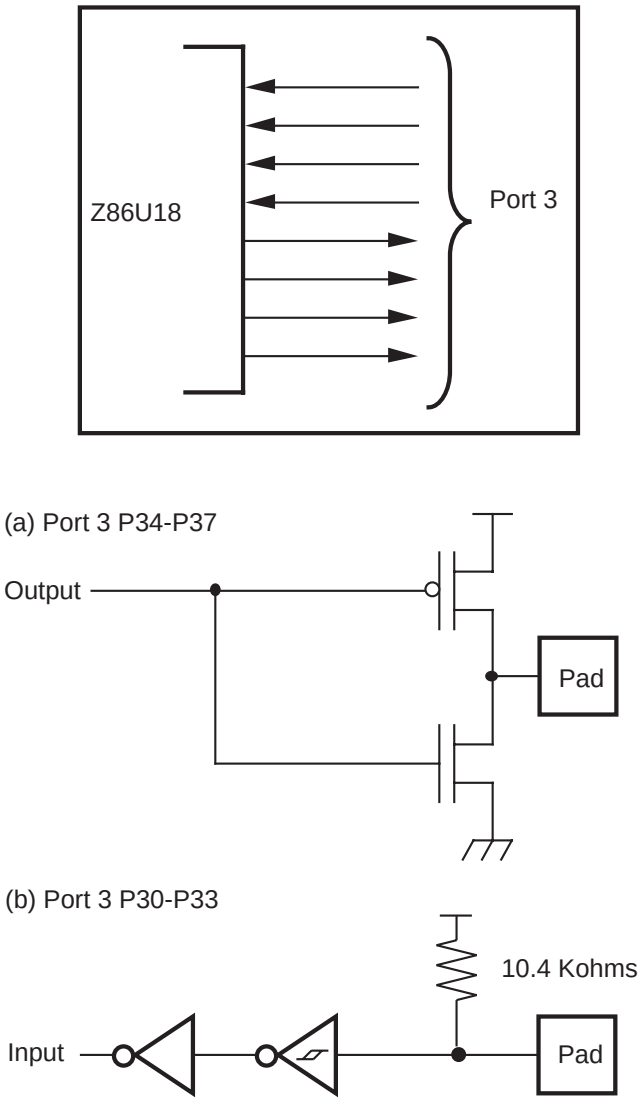


Figure 11. Port 3 Configuration

FUNCTIONAL DESCRIPTION

Program Memory. The 16-bit program counter addresses 4 KB of program memory space at internal locations (Figure 12).

The first 12 bytes of program memory are reserved for the interrupt vectors. These locations have five 16-bit vectors that correspond to the six available interrupts.

Byte 12 to byte 4095 consists of on-chip, mask programmed ROM. Addresses 4096 and greater are reserved. The 4 KB program memory is mask programmable.

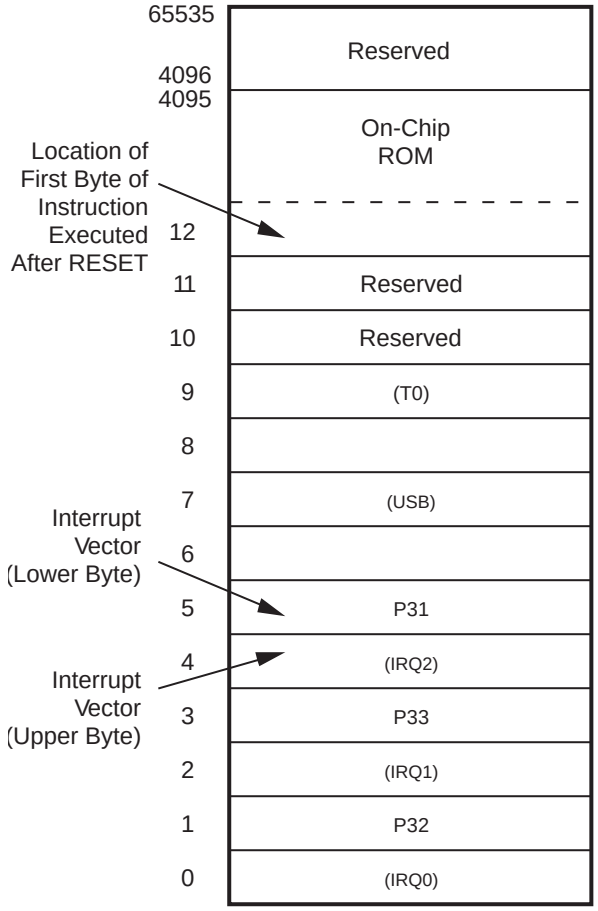


Figure 12. Program Memory Map

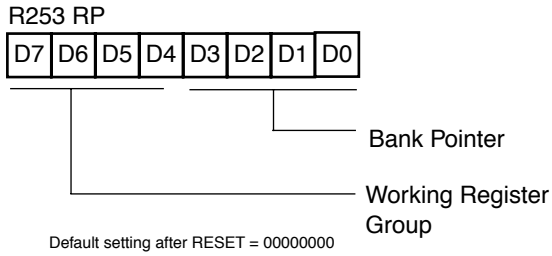


Figure 13. Register Pointer Register

Register File. The register file consists of four I/O port registers, 188 general-purpose registers and 11 control and status registers (R3-R0, R4-191, and R255-R240, respectively). The instructions can access registers directly or indirectly through an 8-bit address field. This allows short, 4-bit register addressing using the Register Pointer (Figure 13). In the 4-bit mode, the register file is divided into12 working-register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group.

Note: To use the Bank Pointer: The instruction SRP 01 must be used to access the USB registers in the Expanded Register File Space. These 8 registers (as defined on pp. 21-24) are available along with those registers from 10h to BFh. Setting SRP 0 will allow access to the register locations 0 to BFh, including the I/O port registers at 0-3.

FUNCTIONAL DESCRIPTION (Continued)

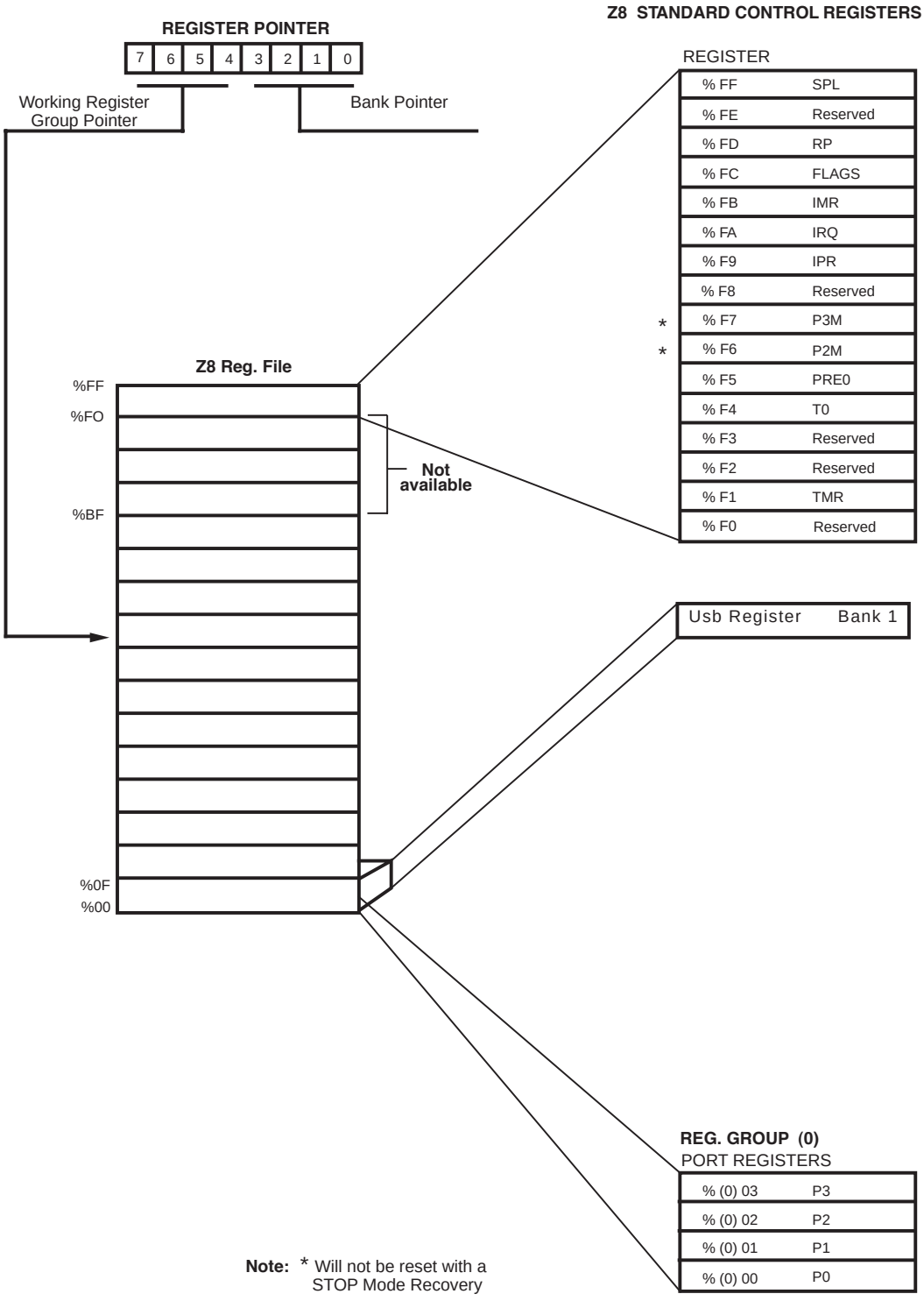


Figure 14. Register File Architecture

Counter/Timers. There is an 8-bit programmable counter/timer (T0) driven by its own 6-bit programmable prescaler (Figure 15).

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. The prescaler drives the counter, which decrements the counter value (1 to 256) on the prescaler overflow. When both the counter and prescaler reach the end of count, a timer interrupt request, IRQ4, is generated.

The counter can be programmed to start, stop, restart to continue, or restart from the initial value. The counter can also be programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode) The counter, but not the prescaler, is read at any time without disturbing its value or count mode.

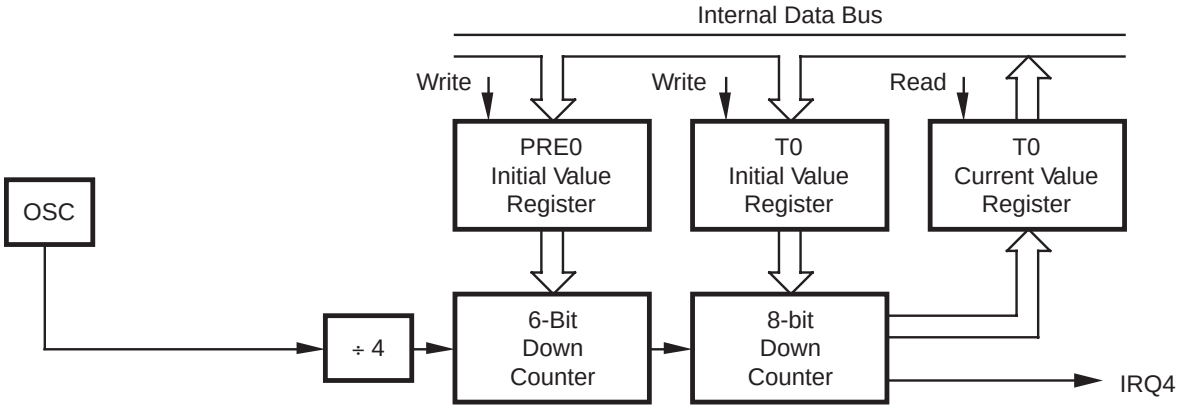


Figure 15. Counter/Timers Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

Watch-Dog Timer. The Watch-Dog Timer is activated automatically by power-on

WDT Hot bit. Bit 7 of the Interrupt Request register (IRQ register FAH) determines whether a hot start or cold start occurred. A cold start is defined as reset occurring from the power-up of the Z86U18 (the default upon power-up is 0). A hot start occurs when a WDT time-out has occurred (bit 7 is set to 1). Bit 7 of the IRQ register is read-only and is automatically reset to 0 when accessed.

Watch-Dog Timer Mode Register (WDTMR). The WDTMR is: WDT (ms) ≈ 50 ms.

WDT During HALT (D5-R250)**.** This bit determines whether or not the WDT is active during HALT Mode. The default is 1, and a 1 indicates active during HALT.

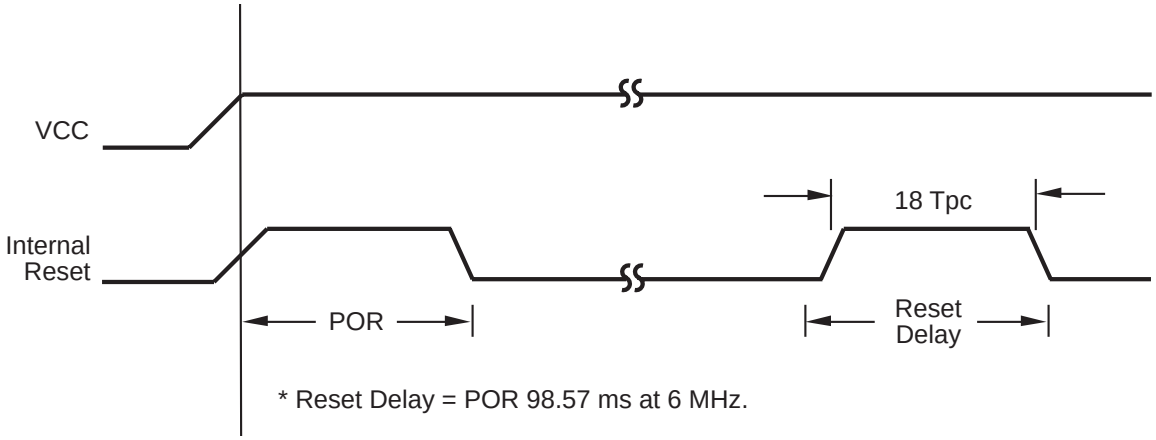


Figure 16. WDT Turn-On Timing After Reset

Interrupts. The Z86U18 has five different interrupts from three different groups. These interrupts are maskable and prioritized (Figure 17). The five sources are divided as follows: three sources are claimed by Port 3 lines P33-P31, one is claimed by the counter/timer, and the other is claimed by the USB interface. The Interrupt Masked Register globally or individually enables or disables the six interrupts requests.

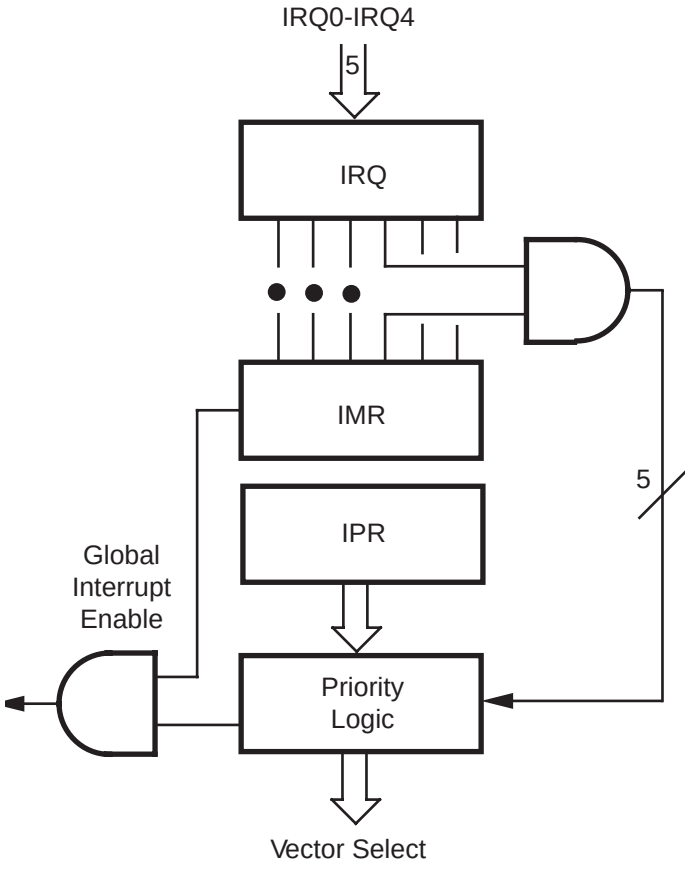


Figure 17. Interrupt Block Diagram

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All interrupts are vectored through locations in the program memory. When an interrupt machine cycle is activated an interrupt request is granted. Thus, this disables all of the subsequent interrupts, saves the Program Counter and status flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt request needs service.

EMI. Lower EMI on the Z86U18 is achieved through circuit modifications. The internal divide-by-two circuit has been removed to further reduce EMI.

The Z86U18 also accepts external clock from Pin 33 (40-Pin DIP).

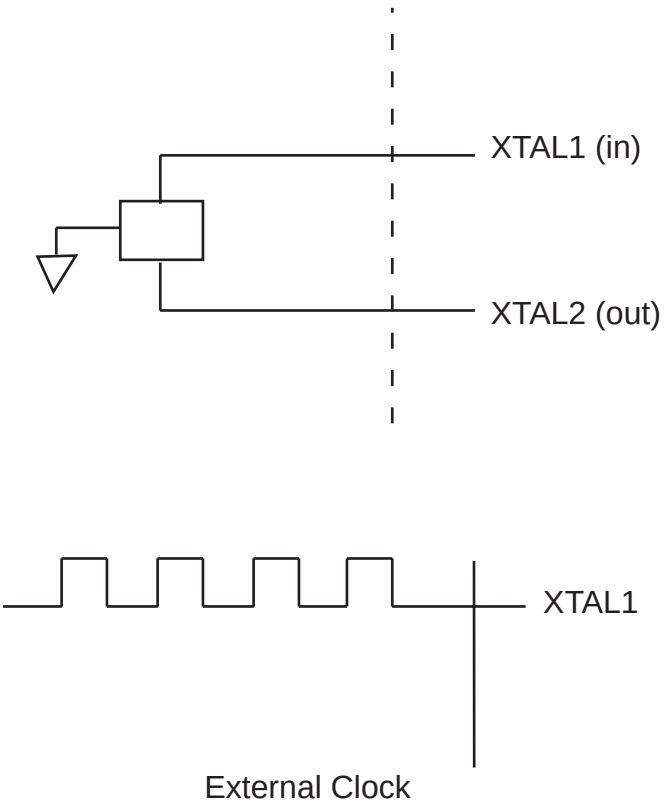


Figure 18. Oscillator Configuration

FUNCTIONAL DESCRIPTION (Continued)

Power-On-Reset (POR)**.** A timer circuit is triggered by the system oscillator and is used for the Power-On Reset (POR) timer function. The POR time allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins. POR period is defined as:

POR (ms) = 98 ms

The POR timer circuit is a one-shot timer triggered by lower fail to Power OK status. The POR time is a nominal 100 ms at 6 MHz. The POR time is bypassed after Stop-Mode Recovery.

HALT. HALT turns off the internal CPU clock, but not the oscillator. The counter/timer and external interrupts IRQ0, IRQ1, IRQ2, and IRQ3 remain active. The Z86U18 recovers by interrupts, either externally or internally.

USB Reset. Detection by the SIE of a reset from the Host will cause the chip to reset. The reset will be remembered so that the program can decide the source of the reset. The USB Reset will act even if the chip is in the STOP mode.

STOP. This instruction turns off the internal clock and external crystal oscillation. It reduces the standby current to less than 10 μA. The STOP Mode is terminated by an interrupt. An interrupt from any of the active (enabled) interrupts will remove the chip from the STOP Mode (Ports 31-33 and the USB reset). The timer can not do this as the clock is stopped. This causes the processor to restart the application program at the address or the vector of the interrupt and continue the program at the end of the interrupt service routine. In order to enter STOP (or HALT) Mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (opcode=FFH) immediately before the appropriate sleep instruction, such as:

```
FF      NOP     ; clear the pipeline
6F      STOP    ; enter STOP Mode
                or
FF      NOP     ; clear the pipeline
7F      HALT    ; enter HALT Mode
```

Z8 CONTROL REGISTER DIAGRAMS

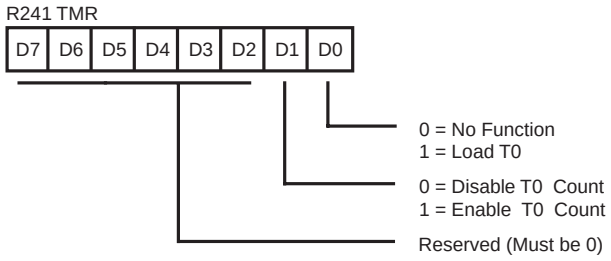


Figure 19. Timer Mode Register ($F1_H$: Read/Write)

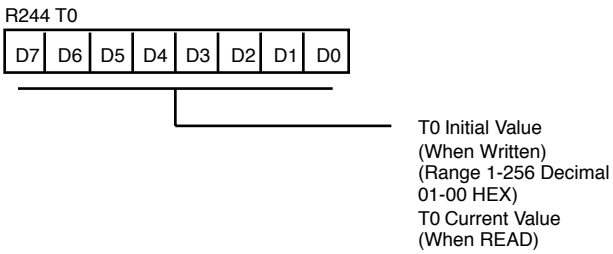


Figure 20. Counter/Timer 0 Register ($F4_H$: Read/Write)

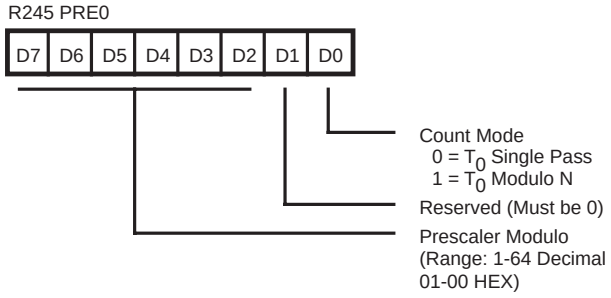


Figure 21. Prescaler 0 Register ($F5_H$: Write Only)

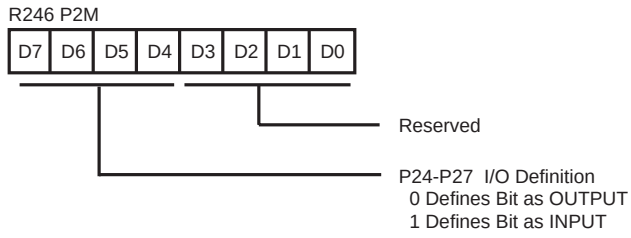


Figure 22. Port 2 Mode Register ($F6_H$: Write Only)

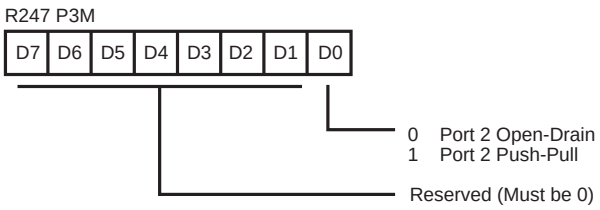


Figure 23. Port 2 Open Drain Register ($F7_H$: Write Only)

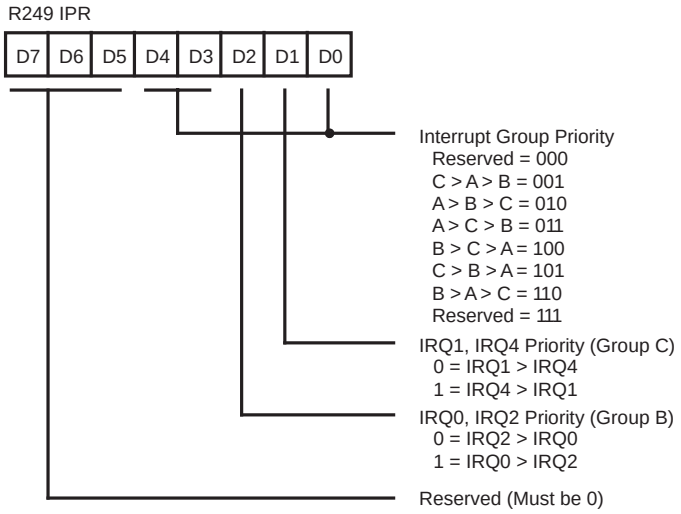


Figure 24. Interrupt Priority Register ($F9_H$: Write Only)

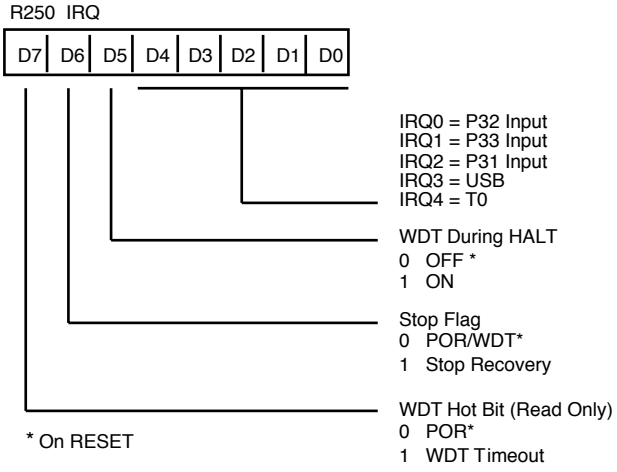


Figure 25. Interrupt Request Register (FA_H: Read/Write)

Z8 CONTROL REGISTER DIAGRAMS (Continued)

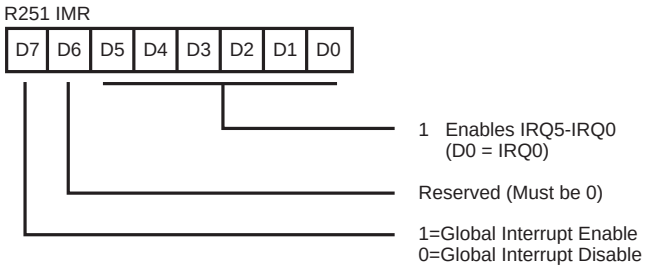


Figure 26. Interrupt Mask Register (FB_H: Read/Write)

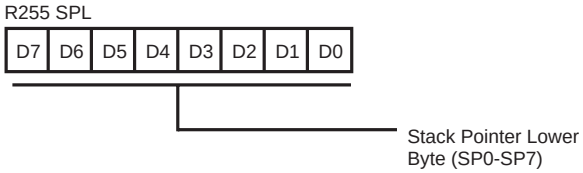


Figure 29. Stack Pointer (FF_H: Read/Write)

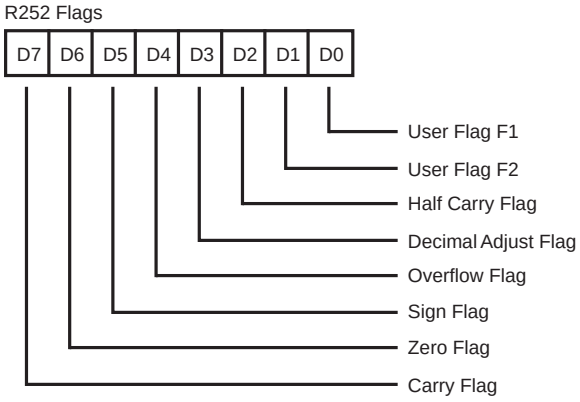


Figure 27. Flag Register (FC_H: Read/Write)

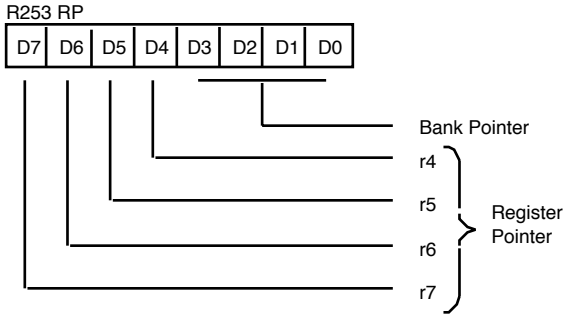


Figure 28. Register Pointer (FD_H: Read/Write)

USB REGISTERS

Table 1. Address Offset Located @ 01 in Expanded Register Space

Register	Address	Reset Value
Function Address	0	00
Endpoint 0 CSR	1	00
Endpoint 0 Write Count	2	00
Endpoint FIFO	3	00
IN CSR	4	40
IN FIFO	5	00
Interrupt Register	6	00
Miscellaneous Register	7	00

REGISTER DESCRIPTIONS

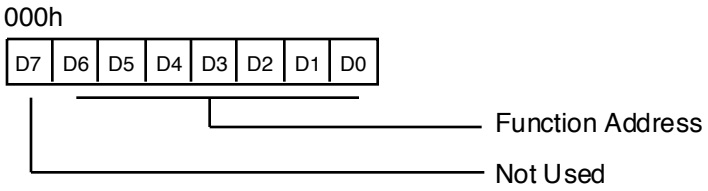


Figure 30. Function Address Register

Bit	µC	SIE	Description
6:0	R/W	R	Upon receiving a SET_Address descriptor, the microcontroller writes this register with the address received from the host.

REGISTER DESCRIPTIONS (Continued)

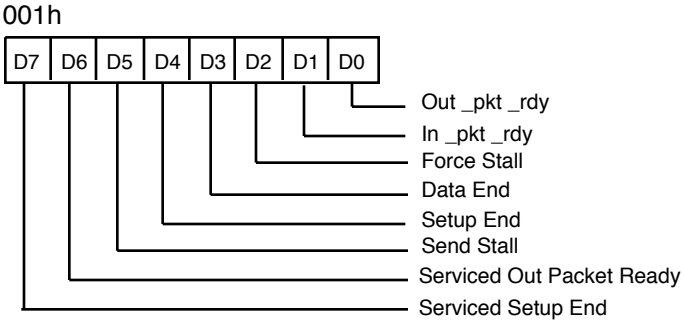


Figure 31. Endpoint 0 CS Register

Bit No	Bit Description	μC	SIE	Description
7	Serviced Setup End	W	R	The microcontroller writes a 1 to this register to clear setup end bit.
6	Serviced Outpacket Ready	W	R	The microcontroller writes a 1 to this register to clear out packet ready bit.
5	Send STALL	W	R	If the microcontroller decodes an invalid descriptor, it writes a 1 to this register before clearing out_pkt_rdy bit or when microcontroller decodes a set feature or clear feature USB command from the host.
4	Setup End	R	W	If the function receives a new setup transaction before the previous one is complete (entire length of data is transferred), this bit is set. Upon seeing this bit set, the microcontroller should abort the current set operation.
3	Data End	W	R	During the data phase of a control transfer after the microcontroller has received/sent the last data as specified in the setup phase, it sets this bit.
2	Force STALL	R	W	The SIE writes to this register, when it encounters a protocol violation, and issues a STALL handshake to the current control transfer.
1	In Packet Ready	W	R	During the data phase, after the microcontroller has filled the data, it sets this bit. It is cleared by SIE upon successful transmittion of data.
0	Out Packet Ready	R	W	The SIE sets this bit after writing data to the FIFO. The microcontroller clears this bit by writing it to Serviced Out Packet Ready bit.

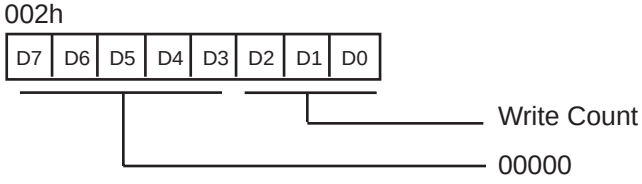


Figure 32. Endpoint 0 Write Count Register

Bit	μC	SIE	Description
2:0	R	W	The contents indicates the number of bytes in the FIFO.

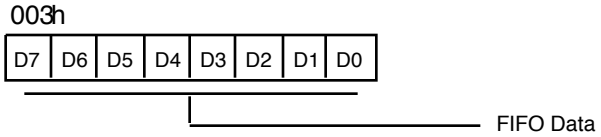


Figure 33. Endpoint 0 FIFO Register

Bit	μC	SIE	Description
7:0	R/W	R/W	This is the Endpoint 0 FIFO data register.

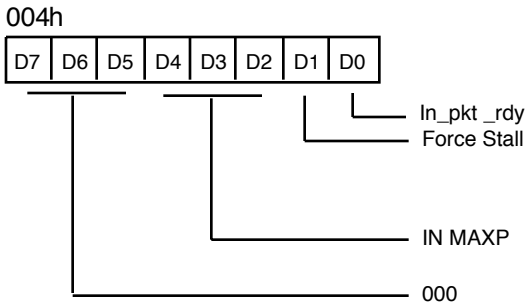


Figure 34. IN CS Register

/Bit No	Bit Description	μC	SIE	Description
4:2	IN MAXP	W	R	Before setting in_pkt_rdy, the microcontroller writes the maximum packet size to these bits. The default value = 8 Bytes.
1	Force STALL	R/W	W	The SIE writes this register, when it encounters a protocol violation, and issues a STALL handshake to the current transfer. The microcontroller sets this bit, when it receives a SET_FEATURE (ENDPOINT_STALL), and clears it, when it receives a CLEAR_FEATURE (ENDPOINT_STALL).
0	In Packet Ready	W	R	After the microcontroller has filled the data, it sets this bit. It is cleared by SIE upon successful transmission of data.

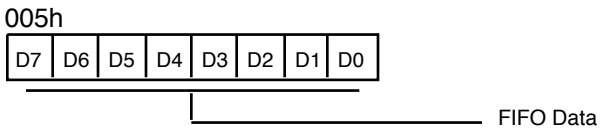


Figure 35. IN FIFO Register

Bit	μC	SIE	Description
7:0	W	R	The microcontroller writes IN data to this register.

REGISTER DESCRIPTIONS (Continued)

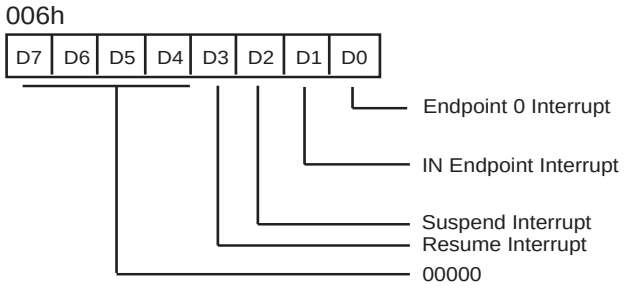


Figure 36. Interrupt Register

Bit No	Bit Description	μC	SIE	Description
3	Resume Interupt	R	W	The flag is sent on the Host signal to resume operations.
2	Suspend Interrupt	R	W	The bit is set when theSuspend signaling is received from the host.
1	IN Endpoint Interrupt	R	W	This bit is set upon: 1) clearing in_pkt_ rdy 2) setting Force STALL.
0	Endpoint 0 Interrupt	R	W	This bit set by SIE upon: 1) setting out_pkt_rdy 2) clearing in_pkt_rdy 3) setting Force STALL 4) clearing data_end 5) setting data_end

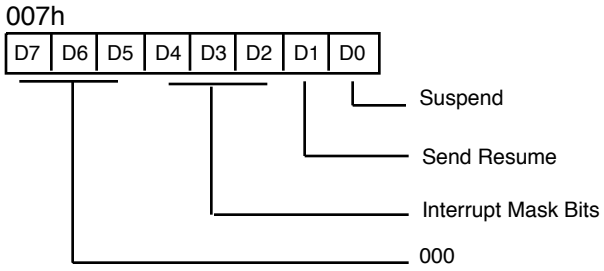
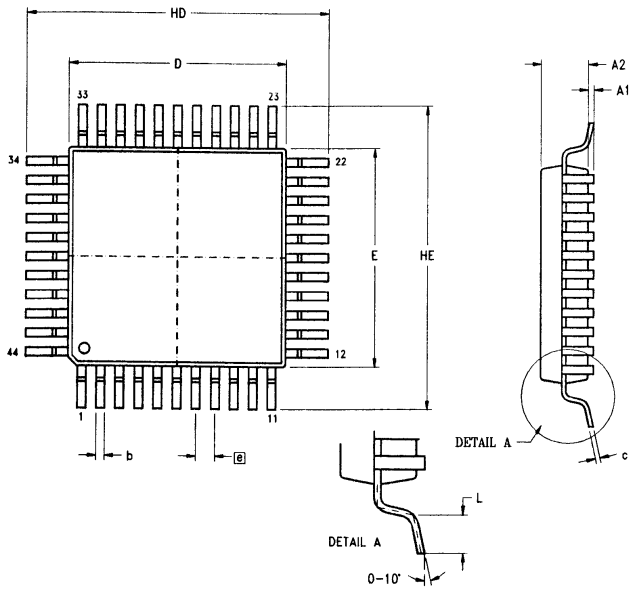


Figure 37. Misc. Register

Bit No	Bit Description	μC	SIE	Description
4:2	Interrupt Mask Bits	R/W	R	This has bit correspondence to the interrupt register. A value of 1, implies that particular interrupt is disabled.
1	Send Resume	W	R	The microcontroller writes a 1 to this bit, while in suspend mode, and wants to start a resume sequence after the clocks are running. This bit is set high for a duration of at least 10 ms by microcontroller.
0	Suspend	R/W	W	This bit is set by the SIE when, the microcontroller is to enter suspend mode. The microcontroller clears this bit after finishing resume signaling, or after it receives a resume out interrupt, and the clocks have started.

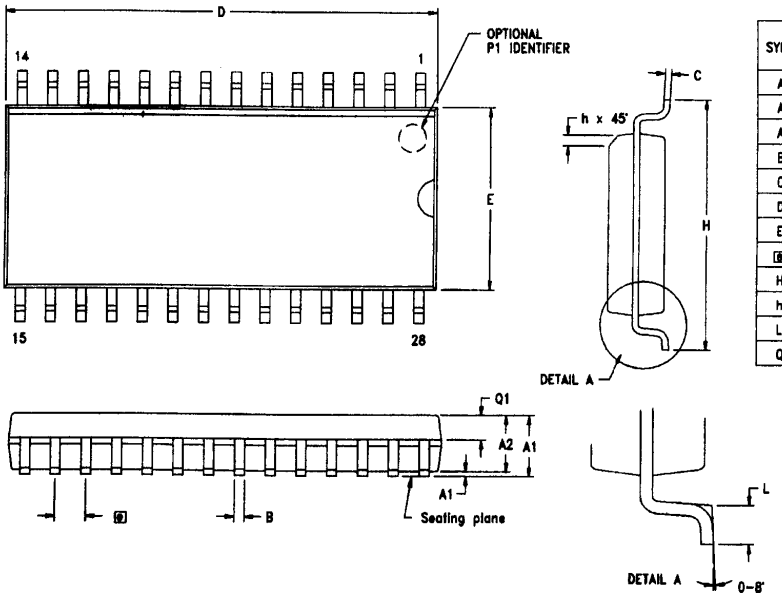
PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.05	0.25	.002	.010
A2	2.00	2.25	.078	.089
b	0.25	0.45	.010	.018
c	0.13	0.20	.005	.008
HD	13.70	14.15	.539	.557
D	9.90	10.10	.390	.398
HE	13.70	14.15	.539	.557
E	9.90	10.10	.390	.398
e	0.80 TYP		.0315 TYP	
L	0.60	1.20	.024	.047

NOTES:
1. CONTROLLING DIMENSIONS : MILLIMETER
2. LEAD COPLANARITY : MAX .10 (.004")

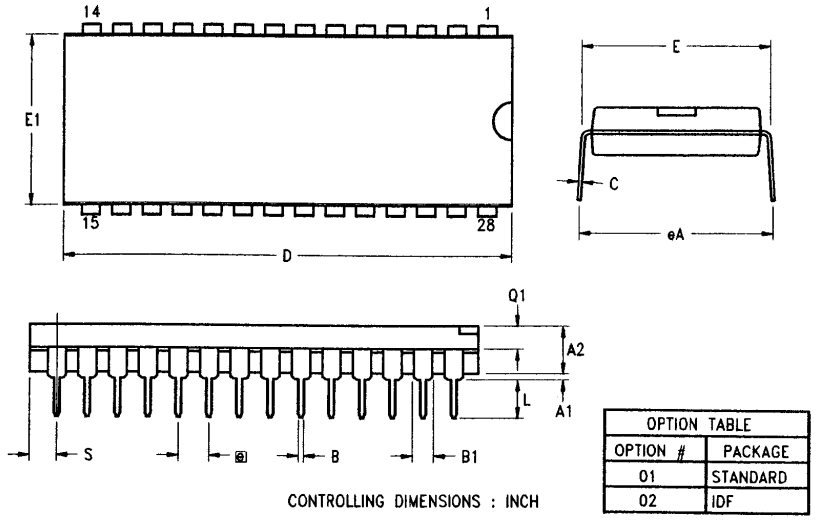
Figure 38. 44-Pin QFP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.64	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	17.78	18.00	.700	.710
E	7.40	7.60	.291	.299
e	1.27 typ		.050 typ	
H	10.00	10.65	.394	.419
h	0.30	0.71	.012	.028
L	0.61	1.00	.024	.039
Q1	0.97	1.07	.038	.042

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

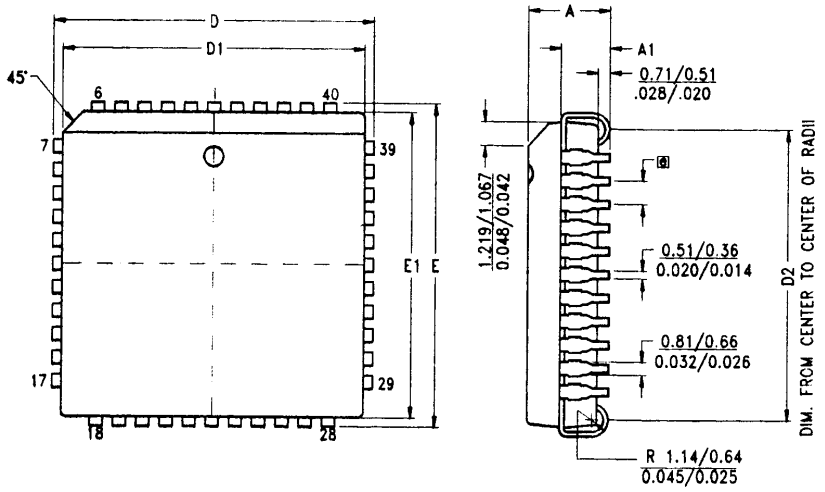
Figure 39. 28-Pin SOIC



OPTION TABLE	
OPTION #	PACKAGE
01	STANDARD
02	IDF

SYMBOL	OPT #	MILLIMETER		INCH	
		MIN	MAX	MIN	MAX
A1		0.51	1.02	.020	.040
A2		3.18	3.94	.125	.155
B		0.38	0.53	.015	.021
B1	01	1.40	1.65	.055	.065
	02	1.14	1.40	.045	.055
C		0.23	0.38	.009	.015
D	01	36.58	37.34	1.440	1.470
	02	35.31	35.94	1.390	1.415
E		15.24	15.75	.600	.620
E1	01	13.59	14.10	.535	.555
	02	12.83	13.08	.505	.515
e		2.54 TYP		.100 TYP	
eA		15.49	16.76	.610	.660
L		3.05	3.81	.120	.150
Q1	01	1.52	1.91	.060	.075
	02	1.52	1.78	.060	.070
S	01	1.52	2.29	.060	.090
	02	1.02	1.52	.040	.060

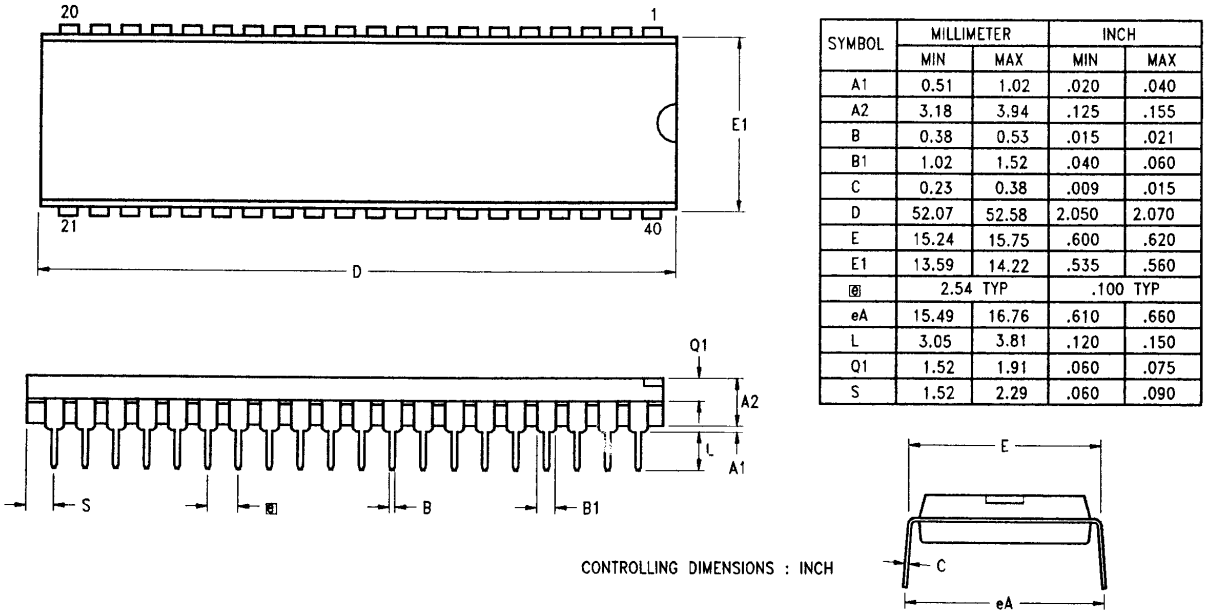
Figure 40. 28-Pin PDIP



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.27	4.57	0.168	0.180
A1	2.41	2.92	0.095	0.115
D/E	17.40	17.65	0.685	0.695
D1/E1	16.51	16.66	0.650	0.656
D2	15.24	16.00	0.600	0.630
e	1.27 TYP		0.050 TYP	

NOTES:
1. CONTROLLING DIMENSION : INCH
2. LEADS ARE COPLANAR WITHIN 0.004".
3. DIMENSION : MM / INCH

Figure 41. 44-Pin PLCC



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	1.02	.020	.040
A2	3.18	3.94	.125	.155
B	0.38	0.53	.015	.021
B1	1.02	1.52	.040	.060
C	0.23	0.38	.009	.015
D	52.07	52.58	2.050	2.070
E	15.24	15.75	.600	.620
E1	13.59	14.22	.535	.560
e	2.54 TYP		.100 TYP	
eA	15.49	16.76	.610	.660
L	3.05	3.81	.120	.150
Q1	1.52	1.91	.060	.075
S	1.52	2.29	.060	.090

Figure 42. 40-Pin DIP

ORDERING INFORMATION

6 MHz	6 MHz	6 MHz	6 MHz	6 MHz
40-Pin DIP	**44-Pin PLCC**	**44-PIN QFP**	**28-Pin DIP**	**28-Pin SOIC**
Z86U18PSC	Z86U18VSC	Z86U18FSC	Z86U18PSC	Z86U18SSC

For fast results, contact your Zilog sales office for assistance in ordering the part desired.

CODES

Package
P = Plastic DIP
V = Plastic Leaded Chip Carrier
F = Quad Flat Pack

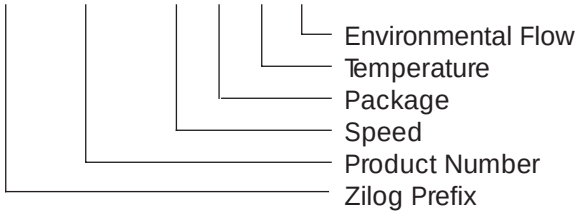
Speed
06 = 6 MHz

Environment
C = Plastic Standard

Temperature
S = 0°C to +70°C

Example:

Z 86U18 05 P S C is a Z86U18, 6 MHz, DIP, 0°C to +70°C, Plastic Standard Flow



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