

Z90365

DIGITAL TELEVISION CONTROLLER

FEATURES

Device	ROM (KW)	RAM* (Words)	PWM (8-Bit)	Voltage Range
Z90365	32	640	8	4.5 to 5.5V

Note: *General-Purpose

- 42-Pin SDIP
- 0°C to +70°C Temperature Range
- Fully Customized Character Set

- Character-Control and Closed-Caption Modes
- Keypad User Control
- TV Tuner Serial Interface
- Direct Video Signals
- Supports Violence Blocking
- Speed: 12 MHz

GENERAL DESCRIPTION

The Z90365 Digital Television Controller is designed to provide complete audio and video control of television receivers, video recorders, and advanced on-screen display facilities. The television controller features a Z89C00 RISC processor core that controls the on-board peripheral functions and registers using the standard processor instruction set.

Character attributes can be controlled through two modes: the on-screen display Character-Control Mode and the Closed-Caption Mode. The Character-Control Mode provides access to the full set of attribute controls, allowing the modification of attributes on a character-by-character basis. The insertion of control characters permits direction of other character attributes. Closed-caption text can be decoded directly from the composite video signal and displayed on-screen with the assistance of the processor's digital signal processing (DSP) capabilities.

The fully customized 512 character set, formatted in two 256 character banks, can be displayed with a host of display attributes that include underlining, italics, blinking, eight foreground/background colors, character position offset delay, and background transparency.

Serial interfacing with the television tuner is provided through the tuner serial port. Other serial devices, such as digital channel tuning adjustments, may be accessed through the industry-standard I²C port.

User control can be monitored through the keypad scanning port, or the 16-bit remote control capture register. Receiver functions such as color and volume can be directly controlled by eight 8-bit pulse width modulated ports.

Notes: All Signals with a preceding front slash, "/", are active Low. For example, B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V _{CC}	V _{DD}
Ground	GND	V _{SS}

The block diagram illustrates the internal architecture of the TMS320C49 DSP. The components and their connections are as follows:

- Capture IRIN:** Receives an external input and connects to the **ADC**.
- ADC:** Contains **ADC0**, **ADC1**, **ADC2**, **ADC3**, and **ADC4**. It receives inputs from **Port 17** and **Port 00** and connects to the **Port 0** and **Port 1** blocks.
- Port 0:** A 16-bit parallel port with pins **Port 00** through **Port 0F**. It connects to the **ADC**, **Control**, and **CPU** blocks.
- Port 1:** A 16-bit parallel port with pins **Port 10** through **Port 18**. It connects to the **ADC**, **Port 0**, and **Port 0F**.
- PWM:** Contains **PWM1**, **PWM2**, **PWM3**, **PWM4**, **PWM5**, **PWM9**, and **PWM10**. It connects to the **Port 0** and **Port 1** blocks.
- Control:** Contains **XTAL1**, **XTAL2**, **LPF**, **HSYNC**, **VSYNC**, and **/Reset**. It connects to the **Port 0** and **CPU** blocks.
- CPU:** The central processing unit, connected to **RAM**, **ROM**, **OSD**, and the **Port** blocks. It has **Register Addr/Data** and **ROM Addr** outputs.
- RAM (640 x 16):** Provides **Address** and **Data** buses to the **CPU**.
- ROM (32K x 16):** Provides **ROM Data** to the **CPU**.
- OSD:** Contains **V1**, **V2**, **V3**, **VBLANK**, and **HALFBLNK**. It connects to the **CPU** and **Port 0F**.

CP97TEL2800

PIN DESCRIPTION

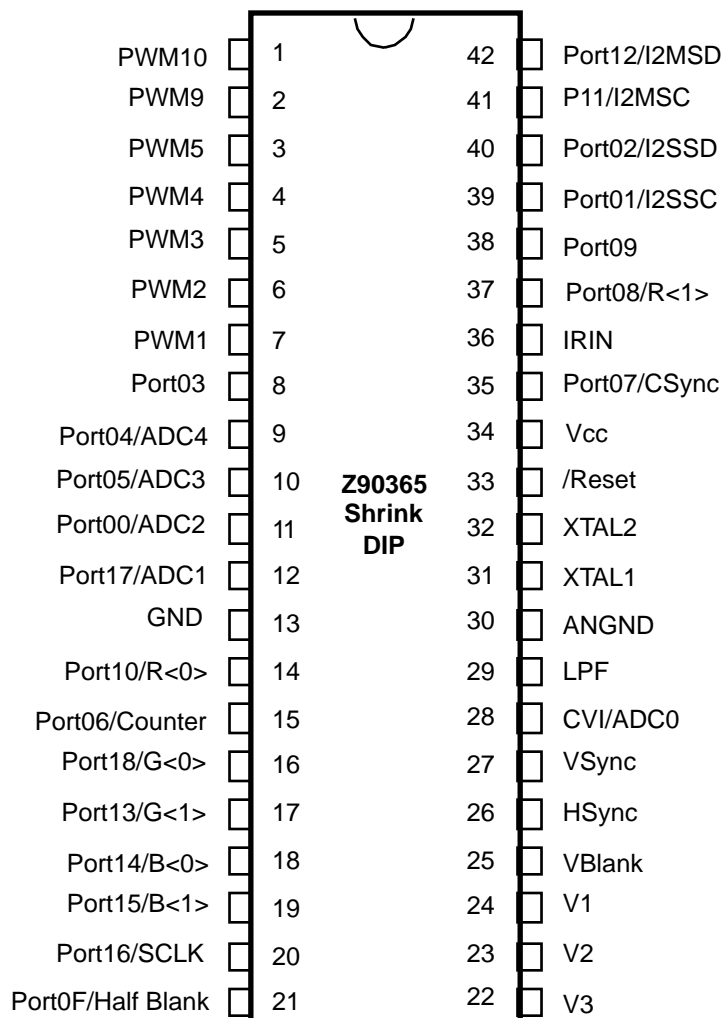


Figure 2. 42-Pin Shrink DIP

PIN DESCRIPTION (Continued)

Table 1. 42-Pin SDIP Pin Identification

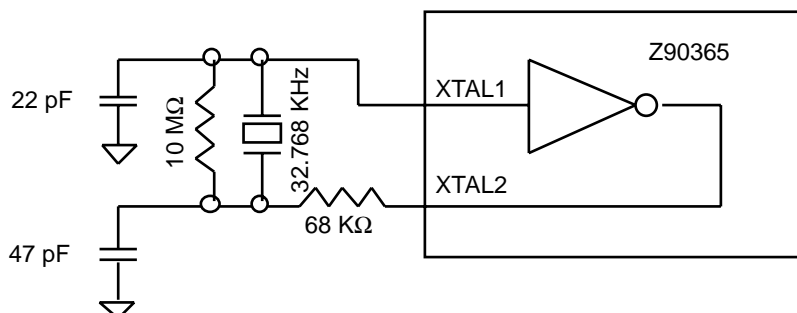
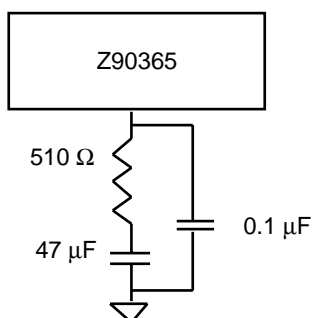
Name	Function	Z90365	Direction	Reset	Notes
V _{CC}	+ 5 Volts	34	PWR	–	
GND	0 Volts	13, 30	PWR	–	
IRIN	Infrared Remote Capture Input	36	I	I	
ADC[4:0]	4-Bit A/D Converter Input	9, 10, 11, 12, 28	AI	I	
PWM10, PWM9	14-Bit Pulse Width Modulator Output	1, 2	O	O	
PWM[5:1]	8-Bit Pulse Width Modulator Output	3, 4, 5, 6, 7	O	O	
Port0[F:0]	Bit Programmable Input/Output Ports	21, -, -, -, -, -, 38, 37, 35, -, -, 15, 8, 40, 39, 11	B	I	1
Port1[8:0]	Bit Programmable Input/Output Ports	16, 12, 20, 19, 18, 17, 42, 41, 14	B	I	
SCL	I ² C Clock I/O	39 or 41	BOD		2
SCD	I ² C Data I/O	40 or 42	BOD		3
XTAL1	Crystal Oscillator Input	31	AI	I	
XTAL2	Crystal Oscillator Output	32	AO	O	
LPF	Loop Filter	29	AB	O	
HSYNC	H_SYNC	26	B	I	
VSNC	V_SYNC	27	B	I	
/Reset	Device Reset	33	I	I	
V[3:1]	OSD Video Output Typically Drive B, G, and R Outputs	22, 23, 24	O	O	
Blank	OSD Blank Output	25	O	O	
HalfBlank	OSD HalfBlank Output	21	O		4
RGB Digital Outputs	R[1:0], G[1:0], and B[1:0] Outputs of the RGB Matrix	37, 14, 17, 16, 19, 18	O		5
SCLK	Internal Processor SCLK	20	O		6

Notes:

1. SCL I/O pin is shared with Port 0 or Port 11.
2. SCD I/O pin is shared with Port 02 or Port 12.
3. Half Blank output is a function shared with Port 0F.
4. Digital RGB outputs and the internal SCLK are shared with Port 1 [5:0].
5. Internal processor SCLK is shared with Port 16.
 PWM outputs are push/pull

V1, V2, V3 (R, G, B) ANALOG OUTPUT (PRELIMINARY) $T_A = 0^{\circ}\text{C}$ to 70°C

	Output Voltage (30 k Ω load)			Settling Time
	$V_{CC} = 4.75$	5.00V	5.25V	70% of DC level, 10pF load
data = 00	0.00v .. 0.65v	0.00v .. 0.70v	0.00v .. 0.75v	< 50 ns
data = 01	1.70v \pm 0.20v	1.80v \pm 0.20v	1.90v \pm 0.20v	
data = 10	2.80v \pm 0.25v	2.90v \pm 0.25v	3.00v \pm 0.25v	
data = 11	3.90v \pm 0.3v	4.0v \pm 0.30v	4.10v \pm 0.30v	

**Figure 3. 32 kHz Oscillator Recommended Circuit****Figure 4. Recommended Low Pass Filter Circuit**

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Units	Conditions
V_{CC}	Power Supply Voltage	0	7	V	
V_{ID}	Input Voltage	-0.3	$V_{CC} + 0.3$	V	Digital Inputs
V_{IA}	Input Voltage	-0.3	$V_{CC} + 0.3$	V	Analog Inputs (A/D0...A/D4)
V_O	Output Voltage	-0.3	$V_{CC} + 0.3$	V	All Push-Pull Digital Output
V_O	Output Voltage	-0.3	$V_{CC} + 0.3$	V	Push/Pull PWM Outputs (PWM1...PMW8)
I_{OH}	Output Current High		-10	mA	One Pin
I_{OH}	Output Current High		-100	mA	All Pins
I_{OL}	Output Current Low		20	mA	One Pin
I_{OL}	Output Current Low		200	mA	All Pins
T_A	Operating Temperature	0	70	°C	
T_A	Storage Temperature	-65	150	°C	

DC CHARACTERISTICS

$T_A = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$; $V_{CC} = 4.5\text{V}$ to $+5.5\text{V}$; $F_{OSC} = 32.768\text{ kHz}$

Symbol	Parameter	Min	Max	Typical	Units	Conditions
V_{IL}	Input Voltage Low	0	$0.2 V_{CC}$	0.4	V	
V_{IH}	Input Voltage High	$0.7 V_{CC}$	V_{CC}	3.6	V	
V_{PU}	Max. Pull-Up Voltage		$V_{CC} + 0.3$		V	All Pins
V_{OL}	Output Voltage Low		0.4	0.16	V	@ $I_{OL} = 1\text{ mA}$
V_{OH}	Output Voltage High	$V_{CC} - 0.4$		4.75	V	@ $I_{OL} = 0.75\text{ mA}$
V_{XL}	Input Voltage XTAL1 Low		$0.3 V_{CC}$	1.0	V	External Clock
V_{XH}	Input Voltage XTAL1 High	$V_{CC} - 2.0$		3.5	V	Generator Driven
V_{HY}	Schmitt Hysteresis	3.0	0.75	0.5	V	On XTAL1 Input Pin
I_{IR}	Reset Input Current		150	90	μA	$V_{RL} = 0\text{V}$
I_{IL}	Input Leakage	-3.0	3.0	0.01	μA	@ 0V and V_{CC}
I_{CC}	Supply Current		100	60	mA	
I_{ADC}	Input Current		10		μA	

Notes:

1. The Z90365 should not be operated for extended periods with the crystal oscillator disconnected, except in the defined power-down modes. In the event that the Z90365 is operated with the oscillator disconnected, the device may draw higher than typical current.
2. Each line of the on-screen display can consist of any number of characters, up to a maximum of 30 characters.

AC CHARACTERISTICS

$T_A = 0^{\circ}\text{C}$ to 70°C ; $V_{CC} = 4.5\text{V}$ to 5.25V ; $F_{OSC} = 32.768\text{ kHz}$

Symbol	Parameter	Min	Typical	Max	Units
T_{PC}	Input Clock Period	16	32	100	μS
T_{RC}, T_{FC}	Clock Input Rise and Fall		12		nS
TD_{POR}	Power-On Reset Delay	0.8	1.2		S
TW_{RES}	Power-On Reset Minimum Width			5 TPC	μS
TD_{HS}	H-SYNC Incoming Signal Width	1	10	15	μS
TD_{VS}	V-SyYNC Incoming Signal Width	1	200	10,000	μS
TD_{ES}	Time Delay Between Leading Edge of V-SYNC and H-SYNC in EVEN Field	-12	0	+12	μS
TD_{OS}	Time Delay Between Leading Edge of H-SYNC in ODD Field	20	32	44	μS
TW_{HVS}	H_Sync/V_Sync Edge Width		0.5	2.0	μS

Note: All timing of the I²C bus interface are defined by related specifications of the I²C bus interface.

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